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Electrical and Electronics Systems Research Division

Oak Ridge National Laboratory Annual Progress Report for the Power Electronics and Electric Motors Program

John M. Miller, Program Manager

November 2013

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US Department of Energy
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Oak Ridge National Laboratory Annual Progress Report for the Power Electronics and Electric Motors Program

Prepared by:

Oak Ridge National Laboratory

John M. Miller, Program Manager

Submitted to:

Energy Efficiency and Renewable Energy
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Susan A. Rogers, Technology Development Manager

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ACRONYMS AND ABBREVIATIONS

3D	three dimensional
ac	alternating current
ACB	active current balancing
AEV	all electric vehicle
AGD	active gate driver
Al	aluminum
Alnico	(Al-Ni-Co-Fe; family of iron alloys)
ANL	Argonne National Laboratory
APEEM	Advanced Power Electronics and Electric Motors (program, DOE)
APEEM	Advanced Power Electronics and Electric Machinery (subprogram, ORNL)
AWG	American wire gauge
bemf	back electromotive force
BREM	Beyond Rare Earth Magnets
CAN	controller area network
CBC	current balancing controller
CDS	Combined Driving Schedule
CFD	computational fluid dynamics
CGD	conventional gate driver
CMOS	complementary metal-oxide semiconductor
CMR	common mode rejection
CT	current transducer
Cu	copper
CVD	chemical vapor deposition
DBC	direct bond copper
dc	direct current
DCR	dc resistance
DCT	differential current transformer
DOE	US Department of Energy
DSP	digital signal processing/processor
Dy	dysprosium
eGaN	enhancement mode gallium nitride
EM	electric machine
EMC	epoxy molding compound
EMI	electromagnetic interference
emf	electromotive force
EPA	Environmental Protection Agency
EPC	Efficient Power Conversion

ESR	equivalent series resistance
EV	electric vehicle
FEA	finite element analysis
FET	field effect transistor
FUL	fault under load
GaN	gallium nitride
GIR	gate impedance regulation
GPM	gallons per minute
GVC	gate voltage control
HEMT	high electron mobility transfer
HEV	hybrid electric vehicle
HIL	hardware in loop
HSF	hard switching fault
HSG	hybrid starter-generator
HV	high voltage
HWFET	Highway Fuel Economy Test
IC	integrated circuit
IGBT	insulated gate bipolar transistor
IM	induction motor/machine
IPM	interior permanent magnet
IR	insulation resistance
IR	International Rectifier
JBS	junction barrier Schottky
JFE	JFE Steel Corporation
JFET	junction field-effect transistor
K	thermal conductivity
K	degrees Kelvin
LA92	Los Angles 92 drive cycle
M/G	motor/generator
MIFP	multiple isolated flux path
MOSFET	metal oxide semiconductor field-effect transistor
Nd	neodymium
NREL	National Renewable Energy Laboratory (DOE)
OBC	onboard charger
OD	outer diameter
OEM	original equipment manufacturer

ORNL	Oak Ridge National Laboratory
PCB	printed circuit board
PCU	power converter unit
PD	power density (peak)
PE	power electronics
PEV	plug-in electric vehicle
PF	power factor
PFC	power factor correction
PM	permanent magnet
PSAT	Powertrain Systems Analysis Toolkit
PSIM	Powersim (circuit simulation software)
PWM	pulse width modulated/modulation
PwrSoC	power supply on chip
R&D	research and development
RC	resistor-capacitor
RL	inductor-resistor
RE	rare earth
RESS	regenerative energy storage system
rms	root mean square
SBD	Schottky barrier diode
SCC	switched capacitor converter
Si	silicon
SiC	silicon carbide
SJT	super junction transistor
SOA	state of the art
SOC	state of charge
SOI	silicon-on-insulator
SP	specific power
SPM	surface permanent magnet
SRM	switched reluctance motor
SSCB	solid state circuit breaker
TC	thermal conductivity
TDS	traction drive system
THD	total harmonic distortion
UC	ultracapacitor
U.S. DRIVE	Driving Research and Innovation for Vehicle efficiency and Energy sustainability (cooperative research effort between DOE and industry partners)

UDDS	Urban Dynamometer Driving Schedule
Vac	volts of alternating current
Vce	voltage across collector and emitter
Vdc	volts of direct current (operating voltage)
VGD	variable gate delay
VSATT	Vehicle Systems Analysis Technical Team
VSI	voltage source inverter
VTO	Vehicle Technologies Office (DOE)
WBG	wide bandgap
ZS	zero sequence

I. INTRODUCTION

The US Department of Energy (DOE) announced in May 2011 a new cooperative research effort comprising DOE, the US Council for Automotive Research (composed of automakers Ford Motor Company, General Motors Company, and Chrysler Group), Tesla Motors, and representatives of the electric utility and petroleum industries. Known as U.S. DRIVE (Driving Research and Innovation for Vehicle efficiency and Energy sustainability), it represents DOE's commitment to developing public–private partnerships to fund high-risk–high-reward research into advanced automotive technologies. The new partnership replaces and builds upon the partnership known as FreedomCAR (derived from "Freedom" and "Cooperative Automotive Research") that ran from 2002 through 2010 and the Partnership for a New Generation of Vehicles initiative that ran from 1993 through 2001.

Oak Ridge National Laboratory's (ORNL's) Advanced Power Electronics and Electric Motors (APEEM) subprogram within the DOE Vehicle Technologies Office (VTO) provides support and guidance for many cutting-edge automotive technologies now under development. Research is focused on developing revolutionary new power electronics (PE), electric motor, and traction drive system (TDS) technologies that will leapfrog current on-the-road technologies, leading to lower cost and better efficiency in transforming battery energy to useful work. The research and development (R&D) is also aimed at achieving a greater understanding of and improvements in the way the various new components of tomorrow's automobiles will function as a unified system to improve fuel efficiency through research in more efficient TDSs.

In supporting the development of advanced vehicle propulsion systems, the APEEM subprogram fosters the development of technologies that will significantly improve efficiency, costs, and fuel economy.

The APEEM subprogram supports the efforts of the U.S. DRIVE partnership through a three-phase approach intended to

- identify overall propulsion- and vehicle-related needs by analyzing programmatic goals and reviewing industry recommendations and requirements, and then develop, and deliver the appropriate technical targets for systems, subsystems, and component R&D activities
- develop, test, and validate individual subsystems and components, including electric motors and PE
- estimate how well the components and subsystems work together in a vehicle environment or as a complete propulsion system and whether the efficiency and performance targets at the vehicle level have been achieved

The research performed under this subprogram addresses the technical and cost barriers that currently inhibit the introduction of advanced propulsion technologies into hybrid electric vehicles (HEVs), plug-in HEVs (PEVs), all-electric vehicles (AEVs), and fuel-cell-powered automobiles that meet the goals set by USDRIVE.

A key element in making these advanced vehicles practical is providing an affordable electric TDS. This will require attaining weight, volume, efficiency, and cost targets for the PE and electric motor subsystems of the TDS. Areas of development include

- novel traction motor designs that result in increased power density and lower cost
- inverter technologies that incorporate advanced semiconductor devices to achieve higher efficiency while accommodating higher-temperature environments and delivering higher reliability
- converter concepts that leverage higher-switching-frequency semiconductors, nanocomposite magnetics, higher-temperature capacitors, and novel packaging techniques that integrate more functionality into reduced size, weight, and cost applications
- new onboard battery charging electronics that build from advances in converter architectures for decreased cost and size
- more compact and higher performing thermal controls achieved through novel thermal materials and innovative packaging technologies

- integrated motor-inverter TDS architectures that optimize technical strengths of the underlying PE and electric machine subsystems.

ORNL's APEEM research program conducts fundamental research, evaluates hardware, and assists in the technical direction of the VTO APEEM program and in setting national policy for future AEVs that addresses the overarching goal of petroleum and greenhouse gas reduction. In this role, ORNL serves on the U.S. DRIVE Electrical and Electronics Technical Team, evaluates proposals for DOE, and lends its technological expertise to the direction of projects and evaluation of developing technologies. ORNL also executes specific projects for DOE.

DOE's continuing R&D into advanced vehicle technologies supports the administration's goal to produce a five-passenger affordable AEV with a payback of less than five years and sufficient range and fast charging capability to enable average Americans everywhere to meet their daily transportation needs more conveniently and at lower cost by the year 2022.

Research Highlights

These highlights of the APEEM R&D efforts begin on page 3.

Task 2: Traction Drive Systems Research and Technology Development

Task 2.1 System Modeling, Efficiency Mapping, Identification of Research Gaps

- Modeled a baseline Nissan LEAF inverter and motor
- Identified the highest-energy-throughput areas for the Urban Dynamometer Driving Schedule and Combined Driving Schedule using the clustering and energy histogram methods
- Provided TDS operating targets to the PE and electric motors areas in the APEEM program
- Completed the TDS model in a circuit simulator

Task 2.2 Inverter Development and System Controls

- Acquired, tested, and characterized a gallium nitride switch, a silicon carbide (SiC) super junction transistor, and an SiC junction barrier Schottky diode
- Completed design, build, and testing of an all-SiC 10 kW inverter using a state-of-the-art commercial all-SiC module

Task 2.3 Benchmarking Competitive Technologies

- Conducted thorough teardown assessment and testing/evaluation of the 2013 Nissan LEAF 6.6 kW onboard charger
- Procured and disassembled 2013 Toyota Camry power converter unit and determined device characteristics
- Performed dynamometer testing of Remy induction motors (one with aluminum and one with copper rotor bars)
- Performed dynamometer testing of the 2012 Hyundai Sonata hybrid starter-generator

Task 2.4 System Integration and HIL Validation

- Completed design of universal control circuitry and board population
- Programmed and implemented a digital signal processor control board with driver circuitry and test setup
- Built, programmed, and assembled power analysis equipment
- Developed and successfully operated subscale dynamometer system
- Designed, fabricated, and assembled custom induction motor with GlidCop and aluminum rotor bars for subscale testing
- Procured battery emulator and ordered dynamometer

Task 3: Power Electronics Research and Technology Development

Task 3.1 Silicon to WBG Inverter Packaging

- Developed advanced power module packaging technologies, based on a directly integrated cold-base plate concept, that feature a 33% reduction in specific thermal resistivity compared with conventional technologies
- Fabricated a group of phase-leg power modules (50–100 A/1,200 V) with different combinations of power device (silicon, SiC) and thermal packages
- Performed comprehensive characterization and comparative system evaluation. Combining the attributes of the latest SiC power devices and advanced packaging enables an all-SiC power module with a 3× increase in current density and a 50% reduction in power losses compared with an all-silicon module

Task 3.2 WBG Gate Driver and Smart Power Module

- Developed and experimentally verified a highly integrated gate drive that operates successfully at 200°C
- Fabricated and verified the functionality of an isolation chip. Demonstrated an input pulse width modulation signal frequency of 5 MHz
- Designed and verified a common mode rejection test printed circuit board. The design allows for testing in excess of 30 kV/μs
- Completed the layout of the isolation chip
- Fabricated a power supply in package, consisting of a boost converter and on-chip inductor for characterization
- Designed an isolated power supply on chip schematic. Preliminary simulation results are encouraging. A plan for isolated feedback control to regulate the power supply has been established
- Fabricated the hardware prototype of the SiC metal oxide semiconductor field effect transistors (MOSFETs) with three overcurrent protection methods (solid state circuit breaker, desaturation technique, and fault current evaluation)
- Extensively evaluated the performance of the protection schemes under various conditions, considering variation of fault type, decoupling capacitance, and protection circuit parameters
- Proposed protection schemes capable of clearing a short-circuit fault within 200 ns, irrespective of the junction temperature variation of SiC MOSFETs
- Based on the testing results, compared each method to explore the benefits and drawbacks of each one and its potential applications
- Verified the active current balancing scheme by simulation and experiment, demonstrating the elimination of current unbalance for two parallel SiC MOSFETs
- Developed an active gate driver to eliminate cross talk for a phase leg using wide bandgap devices, and integrated the logic signal synthesis of the proposed gate auxiliary circuit with the latest version of a high-temperature gate driver integrated circuit
- Developed a board-level integrated power module and conducted the preliminary test for functionality verification

Task 3.3 WBG dc-dc and On-Board-Charger

- Completed a modeling, analysis, and simulation study for several isolation converter architectures and down-selected one for prototype development
- Developed a control strategy for the isolation converter to reduce the battery ripple current of twice the ac main frequency that is inherent in single-phase ac-dc converters. Simulation results show the control strategy enables a 60% reduction in the ripple current and thereby a significant size reduction in the bulky dc link capacitor in the front ac-dc converter

- Completed a direct bond copper substrate design for wide bandgap switch phase-leg modules for Cree SiC MOSFETs and Schottky diodes
  - Direct bond copper cards based on the design were fabricated.
  - Several SiC MOSFET phase-leg modules using the direct bond copper cards were assembled.
- Conducted testing and evaluation of Efficient Power Conversion low-voltage (<200 V) enhancement mode gallium nitride switches for possible use in the 14 V dc-dc converter
- Conducted testing and evaluation of International Rectifier 600 V gallium nitride switches packaged by Delphi for use in high-voltage converters
- Completed a design for a 6.6 kW isolation converter using ORNL-designed SiC phase-leg modules and planar ferrite cores
- Completed tests of a baseline 5 kW Si-based integrated charger, using the selected isolation converter candidate, that demonstrated an isolation converter peak efficiency of 98% and a charger system peak efficiency of 93%

Task 3.4 Power Electronics and Regenerative Energy Storage Systems Matching

- Reviewed, modeled, and simulated bi-directional dc-dc converter architectures that interface the regenerative energy storage system with the traction drive inverter and created a summary review report discussing the operating principles, controls, advantages, and drawbacks of these converter architectures
- Reviewed and analyzed hybrid regenerative energy storage system architectures and created a summary report based on the advantages, drawbacks, control systems, performance, number of components, and other characteristics
- Reviewed, analyzed, modeled, and simulated four battery/ultracapacitor hybridization strategies
- Built simulation models of the battery and ultracapacitor
- Modeled hybridization architectures
- Simulated a representative portion of the Urban Dynamometer Driving Schedule that includes acceleration, braking, and idling conditions for t = [690, 760] for these hybridization architectures
- Collected data and compared the simulation results
- Created a comparison results table for the regenerative energy storage system hybridization architectures

Task 4: Electric Motor Research and Technology Development

Task 4.1 Traction Drive Electric Motor Development

- Completed identification of motor R&D candidates.
- Completed comparisons based on DOE 2020 targets for specific power, power density, specific cost, and efficiency.
  - Candidate designs include the induction motor, switched reluctance motor, and eventually synchronous reluctance motor.
  - Package-efficient (i.e., smaller) motor designs are more challenging thermally. This challenge prompted closer collaboration with the National Renewable Energy Laboratory, which was achieved in the complementary task 1.2.
- Developed a more package-efficient traction motor that analysis shows can meet DOE 2020 targets:
  - minimizes material content
  - benefits from low-loss, affordable electrical steels
  - promotes operation at higher continuous power using improved thermal management materials
- Completed mass and cost calculations that show the selected, and commercially available, baseline interior permanent magnet traction motor will be challenged to meet DOE 2020 targets because

  - Rare earth magnets are a small fraction of the total mass but a very large fraction of cost.
  - Interior permanent magnet designs are close to or at their rotor structural stress limits; therefore, moving to much higher speeds will be challenging.
- Achieved success in a new process for low-loss, potentially cost-effective electrical steel that is suitable for high-volume manufacturing.
  - In FY 2012, this project validated the performance benefits of low-loss electrical steel and demonstrated, in static testing, substantial improvement in core loss reduction in the baseline interior permanent magnet test motor (temperature rise at the same operating point was 22°C lower than in the comparator).
  - Subsequent dynamic testing of the same interior permanent magnet stators in FY 2013 validated earlier findings and showed core loss was reduced by 86% for commercial high-silicon steel at a 7,000 rpm test condition (speed at which the resultant electrical frequency matches that of the earlier static tests).
  - The new metallurgical process for 6.5% Si steel (Fe 6.5 wt. % Si-500 ppmB) with trace amounts of boron was successfully demonstrated at ORNL using successive strain softening during warm deformation that leads to ease of cold formation, i.e., rolling into thin sheets.
- Completed the design of a high-speed induction motor that analysis shows can meet DOE 2020 targets for performance and cost. Efficiency will be challenging and requires the use of low-loss steel.

Task 4.2 Electric Motor and Driveline Matching

- Prepared technical assessment report evaluating benchmarked TDSs and selected state-of-the-art starter motors for high-speed operation
  - 2012 Nissan LEAF®, 2004 and 2010 Prius, 2011 Sonata, 2007 Camry, 2008 Lexus
  - 2010 Camry starter, Dixie Electric starter, Denso starter (planetary gears, gear manufacturing)
- Performed finite element analysis modal analyses on several traction drive rotors, benchmarked units and ORNL concept rotors
  - 2012 LEAF
  - 2010 Prius
  - ORNL multiple isolated flux path switched reluctance motor
  - ORNL outer rotor generator
  - ORNL induction motor design
- Performed finite element analysis stress and thermal analysis for concept motors
- Designed gearing for ORNL concept motor(s)

In addition to the accomplishments discussed in the research highlights, ORNL entered into a license agreement with Arcimoto, Inc., for limited exclusive commercial use of patented ORNL technology. License PLA-1686 was awarded on March 18, 2013. The agreement combines three ORNL-developed PE technologies under one license.

II. RESEARCH AREAS

2.1 System Modeling, Efficiency Mapping, Identification of Research Gaps

Burak Ozpineci (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1467; Fax: 865-946-1262
Email: liangz@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 2013
Projected End Date: September 2014

Objectives

- Develop a baseline circuit simulation model—the 2012 Nissan LEAF traction drive
- Find the high-energy-throughput points of a 2012 Nissan LEAF traction drive over the Combined Driving Schedule (CDS) which is formed by adding five driving schedules in series (UDDS+US06+HWFET+LA92+UDDS)

Technical Barriers

- Optimum operation of the TDS, not the component
- More detailed simulation of the TDS in a vehicle simulation
- Improved cost and efficiency

Technical Targets

- The TDS
- Cost: $8/kW (2020 target)
- Efficiency > 94% (2020 target)

Accomplishments

- Modeled a baseline Nissan LEAF inverter and motor
- Identified the highest-energy-throughput areas for the Urban Dynamometer Driving Schedule (UDDS) and CDS using the clustering and energy histogram methods
- Provided TDS operating targets to the PE and electric motors areas in the APEEM program
- Completed the TDS model in a circuit simulator

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Introduction

It is imperative that a comprehensive understanding be attained of all the interactions between driveline road load and regenerative energy storage system (RESS) power flows at the TDS level, as they influence the traction motor operating points and its attendant power inverter real and reactive power flows. For this reason, collaboration with Argonne National Laboratory is advised to avoid duplication and expedite the understanding of full system requirements. The objective of this task is to map out where the traction motor and power inverter must deliver optimum efficiency and how different material choices could benefit the full drive system. Examples are the application of new electrical steels in the electric machine, different conductor designs for the electric motor stator, thermal potting compounds, and the novel winding designs and overall geometry needed for higher-speed operation, if that is determined to be the route to pursue. In the PE inverter stage, modeling and simulation will benefit a deeper understanding of where the crossover in cost is between silicon (Si) and wide bandgap (WBG) semiconductor devices, including their matching gate drivers. The results of this system simulation are passed along to Subtasks 3.0 and 4.0 to guide their development roadmaps. For example, suppose results show a TDS can best accommodate WBG devices in the power inverter stage when their pulse width modulation (PWM) frequency is held in the conventional range of 10–20 kHz but voltage is increased to 1,000 Vdc. In that case, PE module development must proceed with a dielectric material suited to this voltage, and electric motor insulation systems and winding designs must also accommodate high voltages. Constraints on insulation systems, such as temperature endurance and high potential standardized test limits, must also be satisfied.

Approach

Circuit and system simulation software is used to model and simulate a baseline EV. The same simulation system is also used to model and simulate new PE and electric machines designed by APEEM and compare them with the baseline. In running the system simulation on the Autonomie software, the following tasks were completed:

- Define and develop at least five highest-energy-throughput zones in the TDS for further action
- Correlate operating efficiency at these five or more zones in the current baseline interior permanent magnet (IPM) TDS with a representative higher-efficiency TDS
- Cascade the requirements to the PE and electric machines sub-thrusts

Results

The project used two approaches to modeling: a top-down approach that includes vehicle-level and circuit-level simulation. Vehicle-level simulation is used to determine the high-energy-throughput points of a 2012 Nissan LEAF model, and the circuit-level approach looks at the operation of the TDS in finer time resolution for more detailed analysis and modeling.

Vehicle-level simulation

A CDS was defined to represent different driving schedules an EV would face, including city, highway, fast acceleration, and stop-and-start-driving. The CDS consists of the Environmental Protection Agency's (EPA) UDDS, the Supplemental FTP Driving Schedule (US06), Highway Fuel Economy Test Driving Schedule (HWFET), Unified Dynamometer Driving Schedule (LA92), and UDDS in sequence. These driving schedules are defined and are available at http://www.epa.gov.

UDDS occurs at the beginning and end of CDS. To observe the high-energy-throughput areas, the 2012 Nissan LEAF baseline vehicle was simulated over UDDS and the motor speed was plotted vs. time in Figure 1. This plot is similar to the vehicle speed plot; since LEAF is an EV, the motor speed is expected to be a scaled version of the vehicle speed.

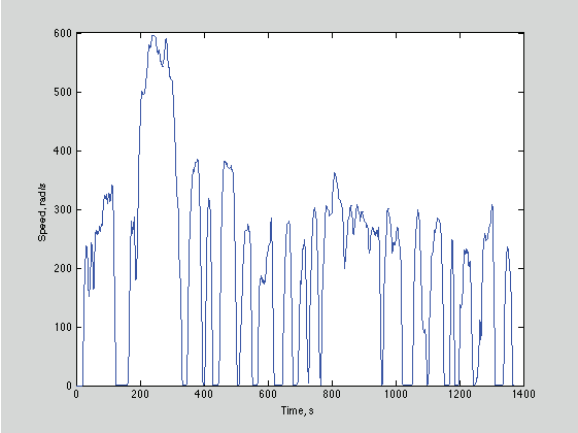


Figure 1: The motor speed profile of the 2012 Nissan LEAF simulated over UDDS on Autonomie.

The high-energy-throughput areas of the traction motor can be obtained from the torque speed curve of the vehicle over the UDDS cycle (Fig. 2). As seen in Fig. 2, if the motoring only region (i.e., first quadrant) is considered[dmc1], the motor is operated at high-torque, low-speed regions, as well as low-torque, medium- and high-speed regions.

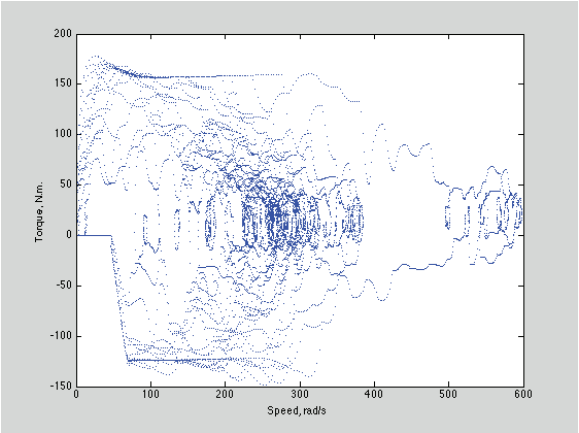


Figure 2: The torque speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

Two methods were used to determine the high-energy-throughput areas: energy histograms and clustering. For the energy histogram method, the torque and the speed values in the motoring region were divided into 40 bins each, forming 1,600 energy bins (40 torque bins × 40 speed bins = 1,600 energy bins). Figure 3 shows the energy bins, where the colors signify the density of operating points in those areas (red=most crowded, blue=least crowded. The red points validate the observation for the high-energy-throughput areas from the torque–speed curve.

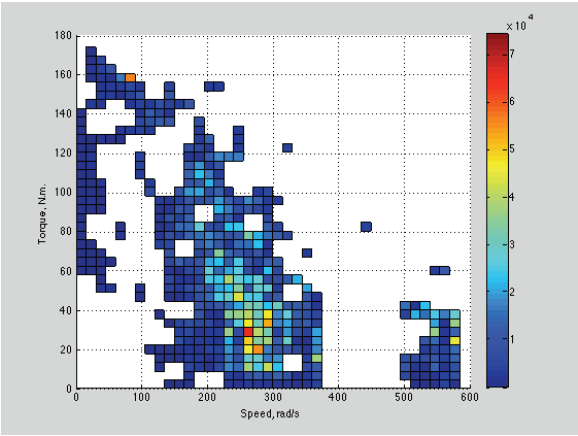


Figure 3: The energy bins obtained from the torque–speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

The clustering method uses the k-means clustering algorithm that forms a pre-specified number of clusters and their cluster centers by classifying each operating point according to its distance from the nearest cluster center. One by one, each operating point is assigned to a cluster in an iterative process. Figure 4 shows the results of this clustering process for three clusters; Table 1 lists the torque and speed values for the cluster centers. As can be seen, the centers of the green and blue clusters are close to the high-energy regions observed using the energy histogram method; but the center of the red cluster is at a much lower torque value compared with the earlier case.

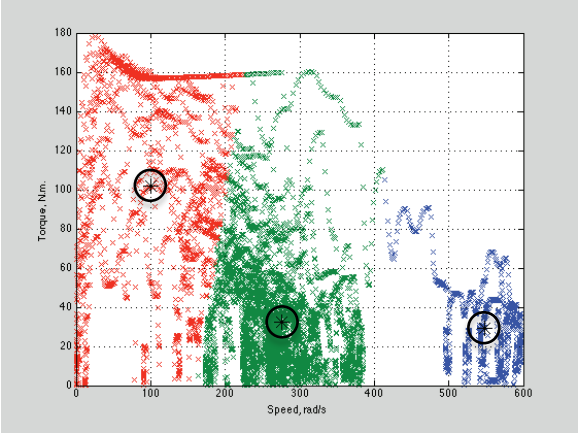


Figure 4: The clusters obtained from the torque–speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

Table 1: Cluster centers

Cluster	Speed (rad/s)	Torque (N.m.)
Blue	548	29.3
Green	275.4	32.4
Red	100.3	102

Figures 5 and 6 show the motor speed profile and the motor torque vs. speed plots of the 2012 Nissan LEAF simulated over CDS.

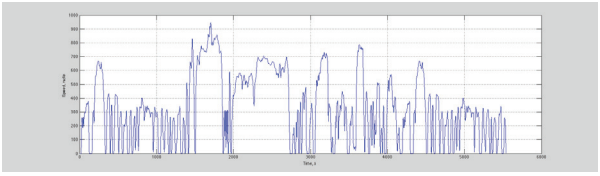


Figure 5: The motor speed profile of the 2012 Nissan LEAF simulated over CDS on Autonomie.

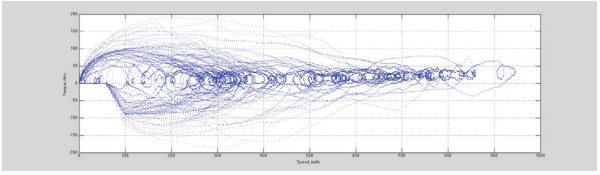


Figure 6: The torque speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

As seen in Fig. 6, there seem to be many areas of high energy throughput, some at the high-torque, low-speed regions but many along the speed axis, i.e. low-torque regions. To get a better understanding of these areas, the energy histogram and clustering methods were applied to the motoring region of the data in Fig. 6.

Figure 7 shows there are some high-energy areas for low-torque, medium-speed regions, but no distinct clusters can be identified.

Figure 8 shows the torque–speed curve with the clustering method applied for five clusters. The centers of the blue and green clusters are close to the high-energy points in Fig. 7. The other three cluster centers are not obvious from the figure. Table 2 lists the torque and speed values for the cluster centers.

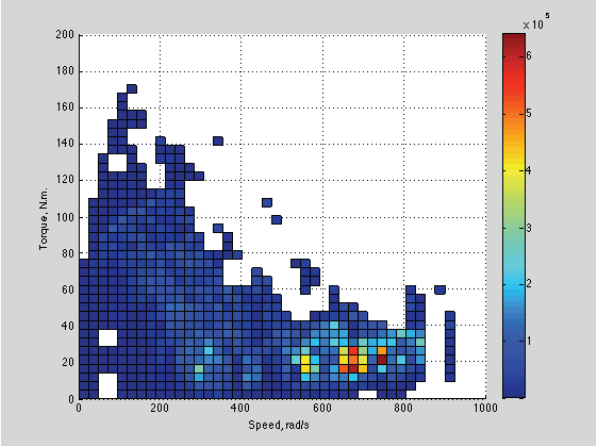


Figure 7: The energy bins obtained from the torque–speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

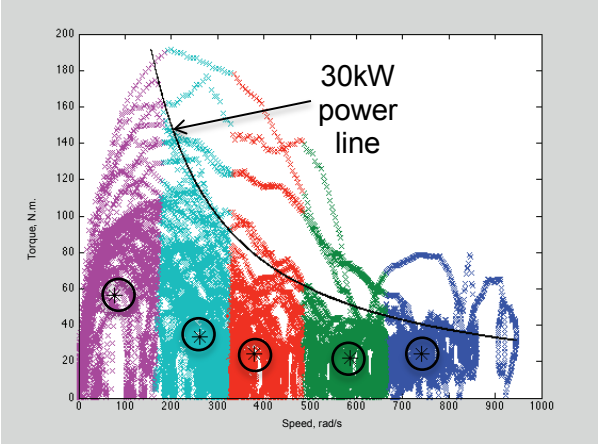


Figure 8: The clusters obtained from the torque–speed curve of the 2012 Nissan LEAF electric motor simulated over CDS on Autonomie.

Table 2: Cluster centers

Cluster	Speed (rad/s)	Torque (N.m.)
Blue	741.7	24.2
Green	586.5	21.8
Red	380.1	24
Cyan	262.2	33.7
Magenta	76.1	56.3

Since the high-energy areas are not obvious in Fig. 7, the figure is plotted in 3 dimensions (Fig. 9) to observe other possible peaks. This figure shows a concentration of high-energy-throughput peaks around the low-torque, high-speed and the low-speed, medium-torque regions, as expected. It is consistent with the results obtained from the clustering method.

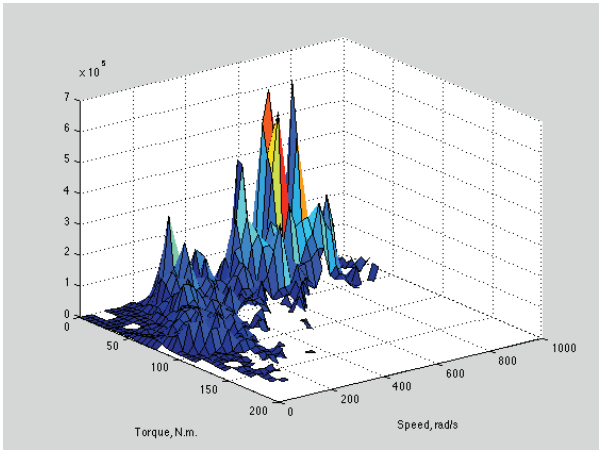


Figure 9: The 3D plot of the energy bins in Figure 7

Circuit-level simulation

Vehicle simulation is usually done at sampling times on the order of seconds or tenths of seconds. Those times would seem like an eternity for a power conversion simulation with device details, as the required sampling times for such conversions would be on the order of nanoseconds. A tradeoff on the level of detail is required. To evaluate the functionality and the performance of a power conversion circuit, sampling times on the order of microseconds would be sufficient. Vehicle-level simulation is conducted using Autonomie. It does not include circuit-level details, which would increase the Autonomie simulation time considerably. As a tradeoff, in this work, the PLECS software was selected for circuit-level simulation.

Figure 10 shows the circuit model of an inverter in PLECS. Figures 11 and 12 show the Nissan LEAF insulated gate bipolar transistor (IGBT) static characteristics and their implementation in PLECS; and Figures 13 and 14, respectively, show the same for the diode.

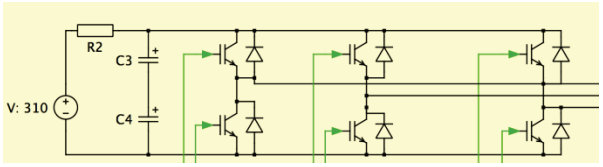


Figure 10: The circuit-level model of the 2012 Nissan LEAF inverter in PLECS.

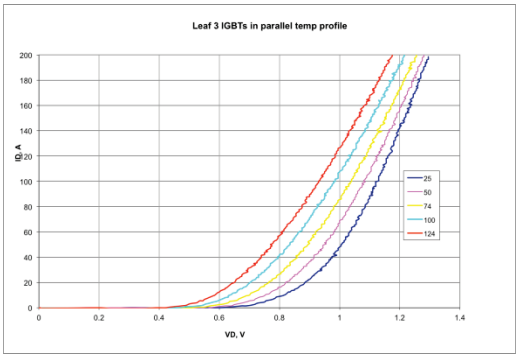


Figure 11: 2012 Nissan LEAF IGBT static characteristics.

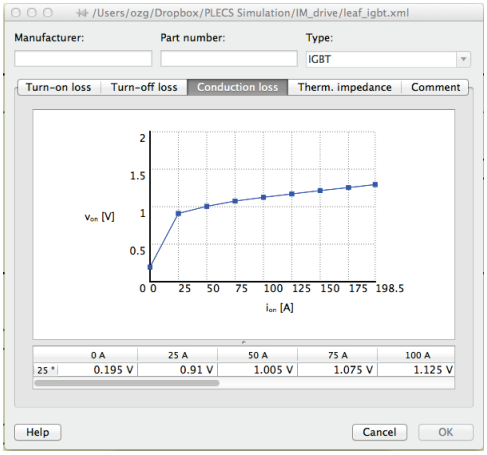


Figure 12: The model implementation of the 2012 Nissan LEAF IGBT static characteristics.

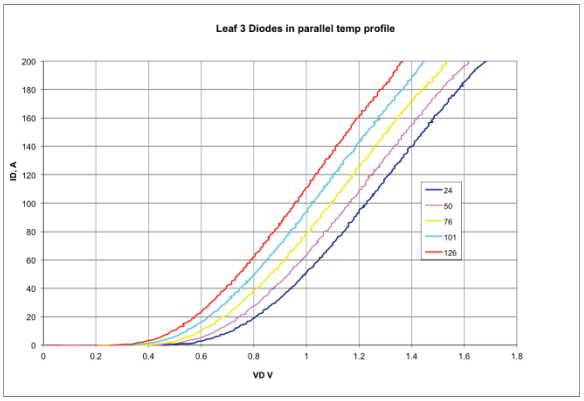


Figure 13: 2012 Nissan LEAF diode static characteristics.

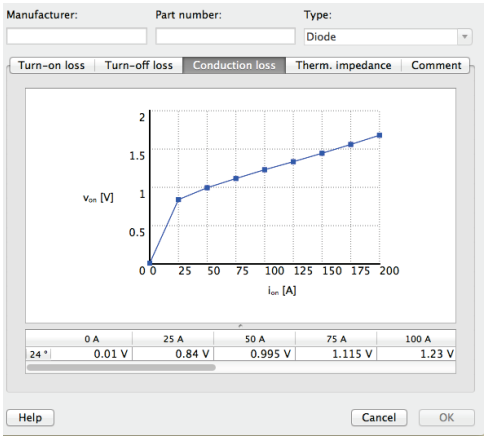


Figure 14: The model implementation of the 2012 Nissan LEAF diode static characteristics.

In addition to the devices and the inverter, the traction drive motor was modeled in PLECS. Figure 15 shows the 2012 Nissan LEAF traction motor model; Figures 16 and 17 show the torque and speed responses, respectively, for a given command profile.

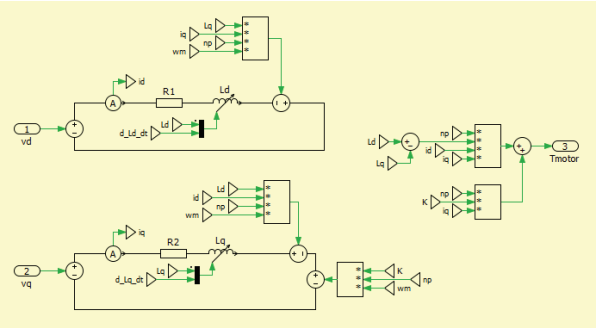


Figure 15: The 2012 Nissan LEAF traction motor model implementation.

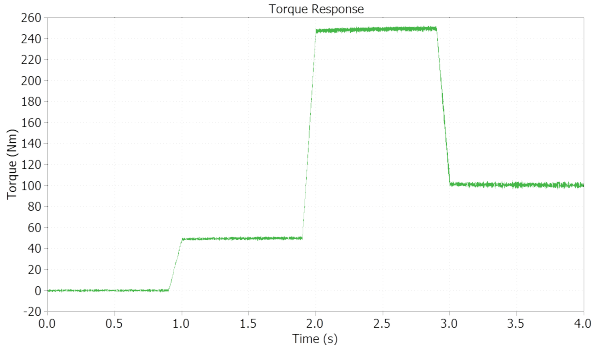


Figure 16: The 2012 Nissan LEAF traction motor model simulation response to a torque command profile.

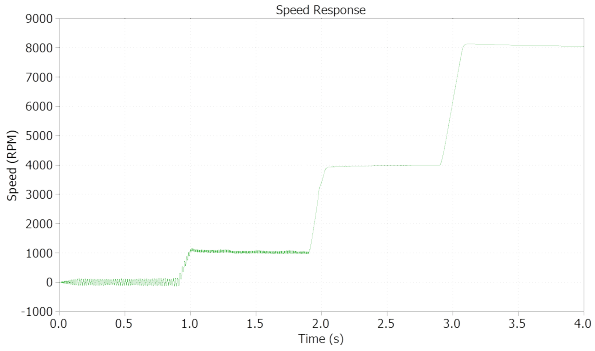


Figure 17: The 2012 Nissan LEAF traction motor model simulation response to a speed command profile.

High-speed induction machine

The purpose of the circuit-level modeling is also to form a platform for simulating converters, inverters, and motors of varying power levels under the same operating conditions and validating their responses. A high-speed induction machine that was developed under another task was modeled and simulated using PLECS to validate its operation. The PLECS model of this high-speed induction machine is shown in Fig. 18, and the machine parameters calculated during the design process are shown in Fig. 19.

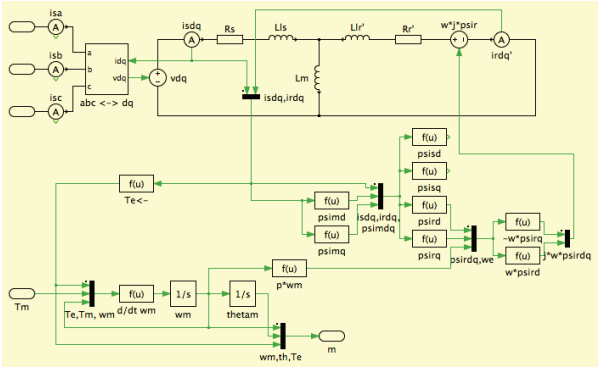


Figure 18: Induction machine model from PLECS.

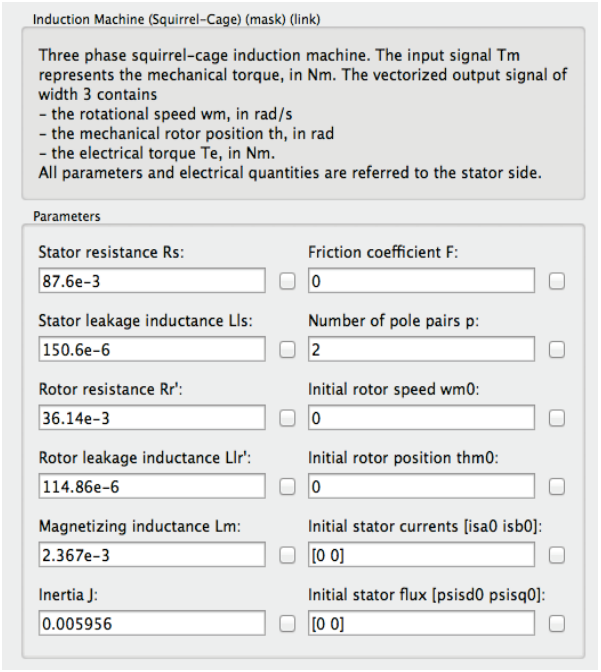


Figure 19: The parameters calculated during the high-speed induction machine design process.

Figure 20 shows the direct-on startup of the machine at no-load and its torque response to rated torque applied at 0.4 s. The torque oscillations observed during torque transitions occur because of the low-inertia design of the machine. Figure 21 shows the speed response corresponding to the startup and step torque response shown in Fig. 20. Figure 22 shows the torque vs. speed curve for this operation, and Fig. 23 shows the torque slip curve. As designed, at 200 Nm, the slip is at 6%.

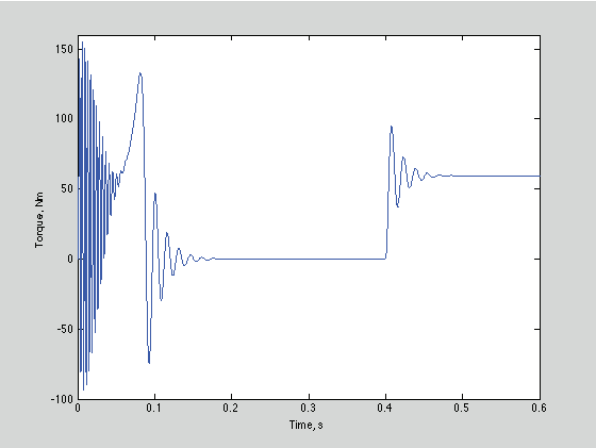


Figure 20: Torque response of the high-speed induction machine during startup and after a step load torque.

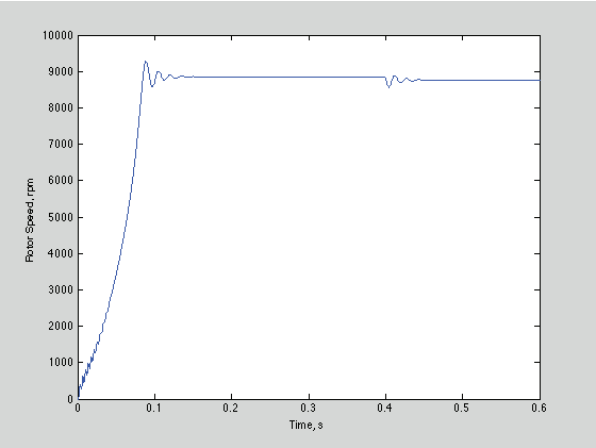


Figure 21: Speed response of the high-speed induction machine during startup and after a step load torque.

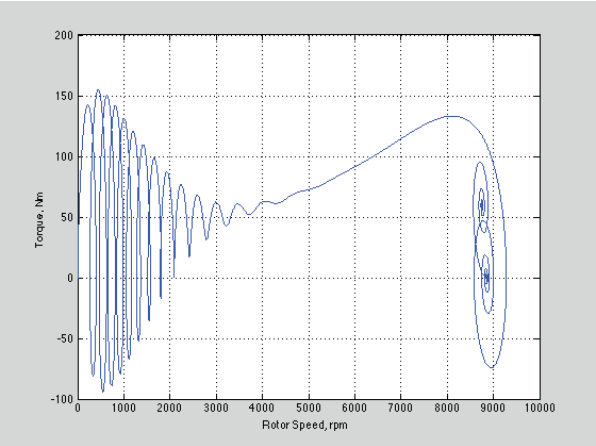


Figure 22: Torque vs. speed curve of the high-speed induction machine during startup and after a step load torque.

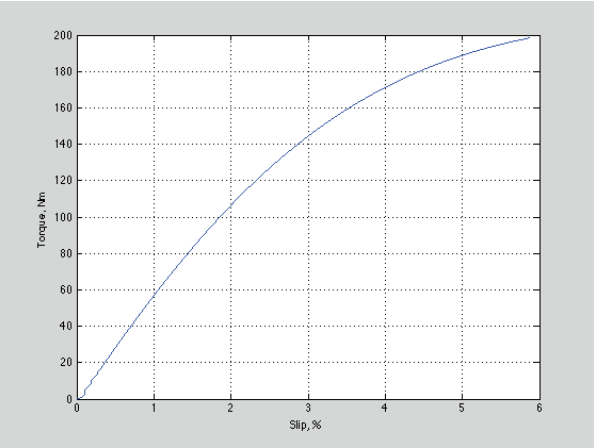


Figure 23: Torque slip curve of the high-speed induction machine

Conclusions and Future Directions

Typical electric motors and inverters are designed for rated power operation; however, they operate at very different operating points in EVs. The vehicle-level simulation results show the high-energy-throughput areas of a baseline EV, which should be used to design the TDSs. System simulations at the circuit and vehicle level can be used to show the operation of the components designed as a part of the program. Circuit-level simulations could be used as a software version of the dynamometers used in the lab to evaluate traction motors and inverters.

The system simulation work is proposed to be discontinued as an independent project during FY 2014. It will continue as a part of other projects.

FY 2013 Publications/Presentations

N/A

FY 2013 Patents

N/A

2.2 Inverter Development and System Controls

Madhu Chinthavali (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1467; Fax: 865-946-1262
Email: chinthavalim@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 2012
Projected End Date: September 2015

Objectives

Overall

- Develop and design a WBG 55 kW inverter using the WBG device attributes. Reduce the size, weight, and cost of the inverter to meet DOE's 2020 inverter targets.

FY 2013

- Design, build, and test a 10 kW WBG-based prototype using commercially available WBG modules.

Technical Targets

- Maintain cognizance of state-of-the-art WBG power devices and acquire, test, and characterize novel devices.
- Develop loss models and circuit models using the test data and discern the inverter benefits.
- Develop and build a single-phase test bed based on conventional mid-point converter architecture to evaluate WBG module performance.
- Design a 10 kW inverter using commercially available WBG devices/modules to demonstrate the performance targets scaled to 30 kW operation.
- Enhance the 10 kW inverter design using the high-temperature packages and the gate drivers developed at ORNL to show the feasibility of achieving 2020 targets.
- Scale the low-power inverter design to demonstrate the performance at 30 kW continuous and 55 kW peak power operation while meeting the 2020 targets.

Accomplishments

- Acquired, tested, and characterized a gallium nitride (GaN) switch, a silicon carbide (SiC) super junction transistor (SJT), and an SiC junction barrier Schottky (JBS) diode.
- Completed design, build, and testing of an all-SiC 10 kW inverter using a state-of-the-art commercial all-SiC module.

✧ ✧ ✧ ✧ ✧

Introduction

Problems associated with PE for advanced vehicle applications include

- cost, size, and weight of power converters and their cooling systems
- need for increased efficiency and reliability

It should be no surprise that none of the EV traction drive systems on the market can meet cost and efficiency goals. Efficiency is attained by using lower-loss devices and materials that tend to be expensive, even as quantities increase. A case in point is motor lamination steel, for which lower-loss grades are manufactured using novel processes that add cost. Table 1 summarizes the specific power and power density of the components in commercially available HEVs and EVs and their system-level metrics relative to DOE 2020 targets. Currently available commercial systems are subject to the following caveats:

- The LEAF motor has lower specific power since it is designed for continuous duty in an EV.
- The LEAF motor has 3 water–ethylene glycol coolant local loops in the stator housing, adding manufacturing complexity.
- All motors shown rely on IPMs containing rare earth (RE) materials that add cost.
- Induction motors (IMs) are less expensive, but are bigger, heavier, and less efficient
- All inverters shown are Si -based, the Prius at 250 A and the LEAF at 640 A.
- For comparison, the Tesla inverter is 800 A and contains more than three times as much Si as the Prius inverter.

Table 1. Commercial traction drive system benchmark summary

Metric	Units	2020 target	2010 Prius	2011 LEAF	2011 Sonata
Peak power	(kW)	55	60	80	30
Inverter	SP (kW/kg)	14.1	16.7 (5.9*)	4.94	6.9
	PD (kW/liter)	13.4	11.1 (6.9)	5.14	7.3
Motor	SP (kW/kg)	1.6	1.6	1.43	1.1
	PD (kW/liter)	5.7	4.8	4.21	3.0
System	SP (kW/kg)	1.44	1.46 (1.25)	1.1	0.95
	PD (kW/liter)	4.0	3.35 (2.8)	2.3	2.13
System efficiency	(peak %)	>94%	~95	~94	93

The goal of this research is to reduce the size and weight of power converters to meet the 2015 and 2020 inverter targets. The overall strategy for cost reduction is shown in Fig. 1. Cost reduction can be achieved by

- reducing the number of components by integrating functionality
- eliminating/reducing the existing liquid cooling loops
- cutting manufacturing costs by decreasing the part count and manufacturing steps
- minimizing high-cost materials, like copper (Cu), through bus bar optimization current reduction

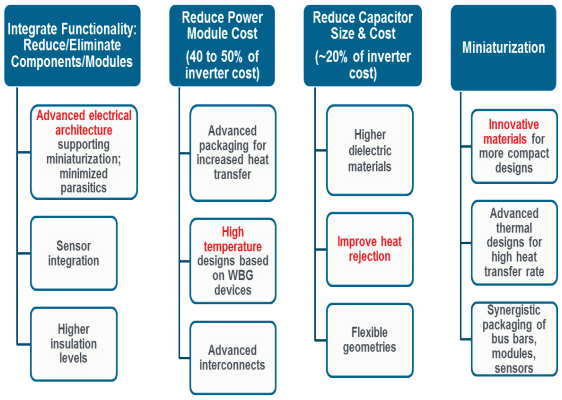


Figure 1. Strategy to reduce power electronics cost.

Approach

There is an increasing need for higher-temperature operation of PE in automotive applications. The ability of components to operate reliably at elevated temperatures can deliver cost and weight savings by reducing heat sinks and eliminating secondary cooling loops. Additionally, devices capable of higher-frequency operation can reduce requirements for passive components, leading to further reductions in cost, weight, and volume. WBG devices, specifically SiC and GaN semiconductors, are emerging technologies that enable higher-temperature and higher-frequency operation as well as efficiency and reliability improvements. The development of WBG devices is promising for helping achieve these goals and VTO targets. The WBG technology assessment performed under this project will help to determine when it is viable to introduce these devices to the market for automotive use. The independent assessment of such devices enables the automotive industry to monitor their progress and provides data readily when the need arises.

A pivotal point in the traction drive program is the PE stage showing single-phase electrical and thermal characterization and the point at which thermal management innovations are put into practice in a WBG-based module. The purpose of focusing on single-phase hardware characterization is that it affords development teams the opportunity to validate hardware at a much simpler stage than the full power inverter and to validate thermal performance.

Single-phase testing and characterization are performed at a bus voltage of up to 800 Vdc and are controlled to synthesize nominal electric machine phase current wave shape, amplitude, and base and switching frequency. The results will be used in subsequent electric motor tests.

Single-phase testing will be followed by multiphase testing under an electric motor equivalent R-L (inductor-resistor) loading. The overall objective of this project is to design and develop a high-voltage WBG 30 kW continuous-power, 55 kW peak-power inverter. WBG devices offer some distinct advantages over Si components. Their primary advantage is that they can operate at higher junction temperatures. This allows for hotter coolant and smaller heat sinks and can potentially help facilitate air-cooling without sacrificing performance.

Many of the typical components in a commercial inverter, e.g., capacitors and gate drivers, cannot withstand the desired operating temperatures of WBG devices. Thus the whole inverter must be considered in developing new high-temperature packages.

Design innovations in this project include the following.

- Layers of high-temperature thermal insulating material are used to separate low-temperature components from the high-temperature zone.
- The high-temperature operating capability of WBG devices enables air cooling, and newer fast-switching Si IGBTs are used for high-temperature liquid designs.
- The innovative heat sink design minimizes thermal resistance.
- There are new control and sensing techniques for system control and efficiency optimization.
- The design is optimized for the most frequently operated points.

These new concepts will increase the power density and decrease the volume and weight for EV traction drive inverters.

Results

1. Device Testing

The new WBG devices acquired this year are a 1200 V, 7 A SiC SJT; a 600 V, 5 A GaN field effect transistor (FET); and a 1200 V, 20 A normally-on junction field effect transistor (JFET). The devices were packaged differently, as shown in Fig. 2. On-

state characteristics and switching energy losses of the devices were obtained over a wide temperature range. The test results for these devices will be presented in the following sections. All the devices obtained were experimental samples.

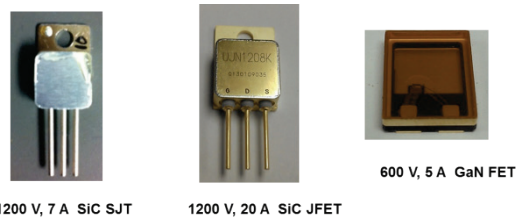


Figure 2. WBG devices tested in FY 2013.

1.1. SiC 1200 V, 7 A high-temperature package SJT

The static characteristics of the 1200 V, 7 A SiC SJT were obtained over a temperature range of 25 to 200°C at Ig= 200 mA for all the tests. The SiC SJT was tested at higher temperatures because it was packaged in a high-temperature metal package. The forward characteristics are shown in Fig. 3. The switching characteristics were obtained over a temperature range of 25 to 200°C at 400 V dc up to 7 A. The energy losses of the device for different currents are shown in Fig. 4.

Static characteristics of a 1200 V, 20 A normally-on SiC JFET for different operating temperatures are shown in Fig. 5. The forward characteristics were obtained for a gate voltage of +0 V. The forward voltage drop of the device at 15 A increased from 0.7 V at 25°C to 2.2 V at 175°C.

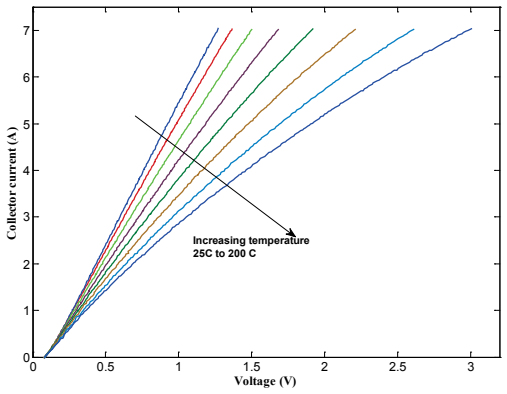


Figure 3. The i-v curves of a 1200V, 7 A SiC SJT.

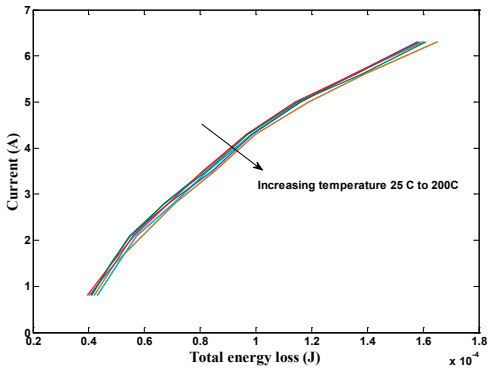


Figure 4. Total switching energy losses of a 1200 V, 7 A SiC SJT at 400 V.

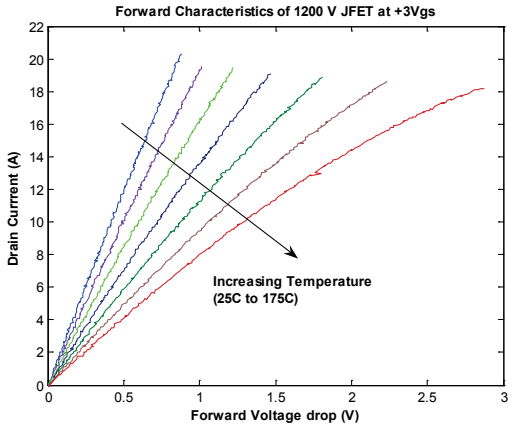


Figure 5. The i-v curves of a 1200 V, 20 A SiC JFET.

The turn-on and turn-off energy losses of the JFET were obtained using a double pulse circuit with a load inductance of 360 µH; a 1200 V, 30 A SiC JBS diode was used as the clamping diode in the circuit. The gate driver used for this testing was a commercial gate driver board, SGDR600P1. The device requires constant current for the device to remain switched on, and this features demands more power from the gate driver. The data were obtained at 600 V dc for various currents at 25 and 175°C. The total energy losses increase with an increase in current; however, the losses do not change much with increasing temperature (Fig. 6).

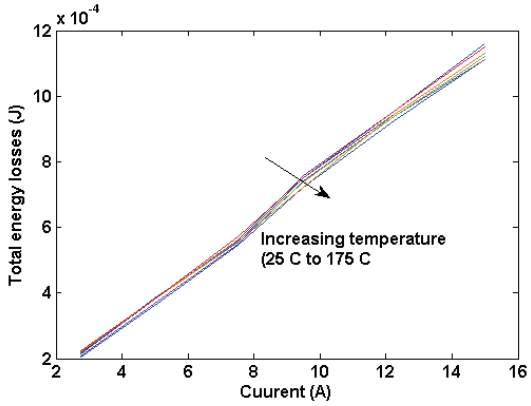


Figure 6. Total switching energy losses of 1200 V, 20 A SiC JFET at 600 V.

1.2. 600 V, 5 A GaN FET

This normally-on FET is the first GaN-based device tested under the DOE VTO program. The static characteristics of a 600 V, 5 A GaN FET were obtained over a temperature range of 25 to 150°C at Vgs = +2 V (Fig. 7). The test setup for the dynamic characterization is shown in Fig. 8. A special test setup was designed to test the device with the pc board. An airflow system with an electrical isolation pad was used to heat the device to just under test, and the rest of the board components were at room temperature. The switching characteristics were obtained at 25 and 50° C at 300 V dc up to 2 A. The switching test waveforms are shown in Fig. 9. The energy losses of the device at a measured temperature of 48.4°C were turn-on losses 17.9 µJ, turn-off losses 7.2 µJ, for total energy losses of 25.1 µJ at 300 V, 2 A, ± 2 V Vgs.

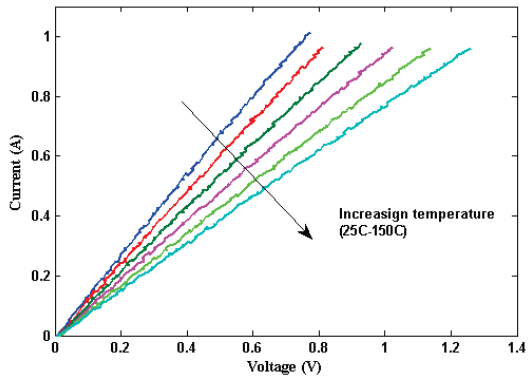


Figure 7. The i-v curves of a 600 V, 5 A GaN FET.

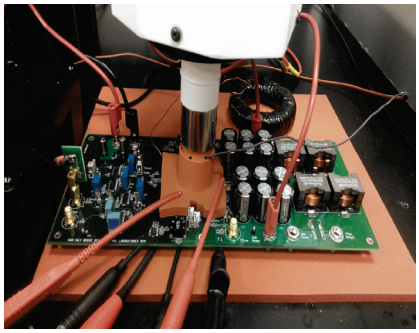


Fig. 8. Experimental setup for dynamic characterization of a 600 V, 5 A GaN FET.

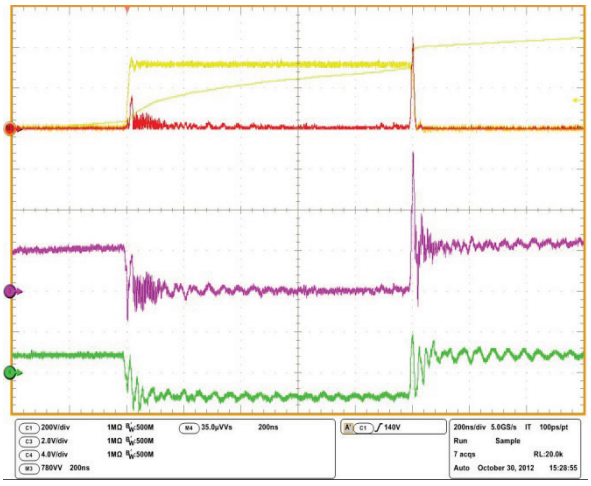


Figure 9. Switching waveforms for a 600V, 5 A GaN FET at 300 V,2 A.

1.3. 2012 Nissan LEAF silicon module

In addition to the WBG devices, a 2012 Nissan LEAF Si power module was evaluated during FY 2013. The test setup is shown in Fig. 10. The Si module was tested over a temperature range of 25 to 150°C at 365 V and up to 200 A. The forward and switching characteristics are shown in Figs. 11 and 12. The data obtained were used in the LEAF system simulation model by the APEEM team at ORNL. In the future, these data will be used to compare WBG devices with Si devices.

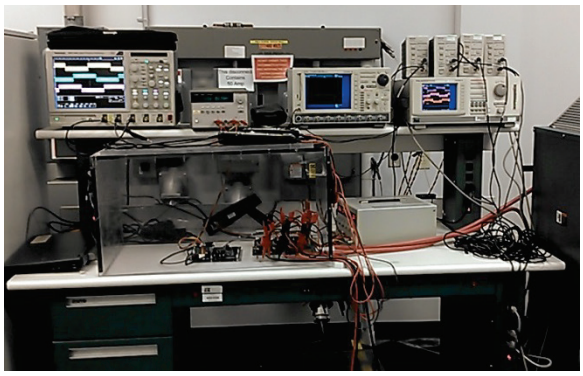


Figure 10. Continuous test bench test setup.

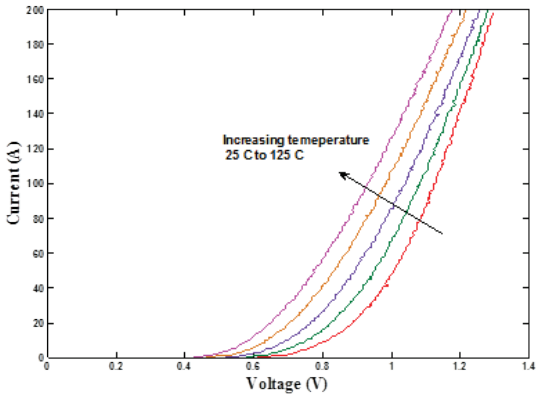


Figure 11. The i-v curves of a 600 V, 600 A Si IGBT.

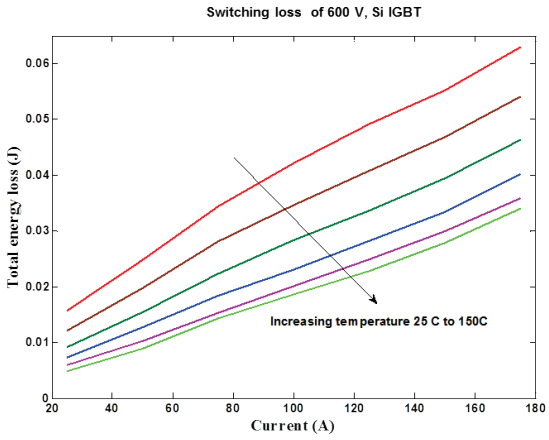


Figure 12. Total switching energy losses of 600 V, 600 A Si IGBT.

2. Continuous test bench for evaluation on WBG devices

Figure 13 illustrates a conceptual single-phase test based on a conventional midpoint converter architecture. As mentioned earlier, the continuous test bed was set up to evaluate the performance of modules and gate drive electronics before they are used in power converters, to ensure reliable operation of the converter. For the 10 kW all-SiC inverter, the 1200 V, 100 A SiC modules and the new gate driver boards were evaluated for functionality. The setup is shown in Fig. 10. The single-phase converter was tested with a resistive load. The waveforms obtained from the test bed are shown in Fig. 14.

3. WBG Inverter Design and Development

3.1 Commercial module–based inverter design

The 10 kW all-SiC inverter was designed using a commercially available 1200 V, 100 A SiC metal oxide semiconductor FET (MOSFET) –based module. The module is shown in Fig. 15 and the layout of the inverter in Fig. 16. The total inverter volume is 3.6 L (226 × 224 × 73 mm). Commercially available gate drivers from Rohm were used. The gate driver has galvanic isolation up to 3000 Vrms and integrated overcurrent protection, undervoltage lockout, and temperature feedback. The performance of the module was evaluated before the inverter was built. The cooling system for this prototype is a single-sided cooling commercially available heat sink. The modules were mounted on the heat sink, with thermal grease as the heat transfer medium from the lower side of the power modules. This prototype model will be packaged as shown in Fig. 16, with controls and capacitors packaged close to the heat sink. The capacitors used in this design are not a brick type but small individual capacitors in series to ensure better cooling and reduce costs.

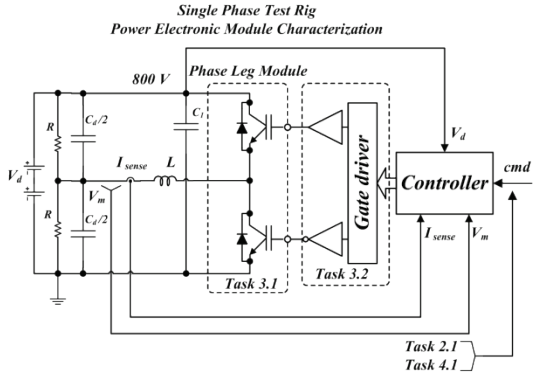


Figure 13. Power electronic single-phase characterization.

Figure 14. Single SiC H-bridge test waveforms obtained using the single-phase test bed. The tests were conducted at 250 V, 15 A continuous operation at 20 kHz.

Figure 15. 1200 V, 100 A SiC MOSFET commercial module.

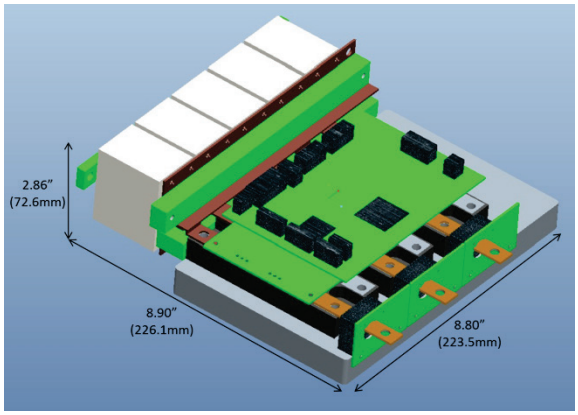


Figure 16. The 10 kW SiC inverter layout.

3.1.1. Characterization of the SiC module

Figure 17 shows forward characteristics of the (1200 V, 100 A) SiC MOSFET for operating temperatures from 25 to 150°C, in 25°C increments. SiC MOSFETs exhibit a linear relationship between voltage and current and have a positive temperature coefficient, which means their conduction losses will be higher at higher temperatures.

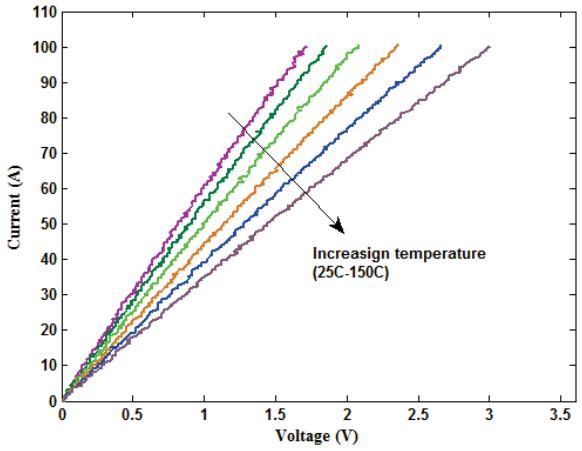


Figure 17. Forward characteristics of 1200 V, 100 A SiC MOSFET module.

A standard commercial driver integrated circuit (IC) from Rohm was used in the drive circuit for both devices. The driver can provide a peak output current of 5 A with a maximum output resistance of 1 Ω. The maximum rise time is 45 ns for a capacitive load of 10 nF with VCC=24 V, according to the data sheet specifications. This feature enables the driver to supply a high dynamic gate current to the SiC MOSFET with a short rise-time. Switching measurements (double pulse tests) were performed to characterize the SiC MOSFET dynamically. The actual test setup is shown in Fig. 18. A load inductance of 120 µH was used for all the tests. The equipment used was a Tektronix DPO 7104 1GHz, a TEK differential probe P5205 100 MHz bandwidth, and a Pearson current probe to 2877 MHZ bandwidth. The total energy losses of the devices were obtained at 600 V and at different currents of up to 100 A (Fig. 19).

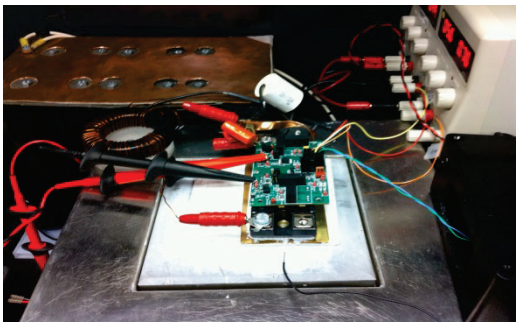


Figure 18. Test setup for the SiC MOSFET module with a gate driver.

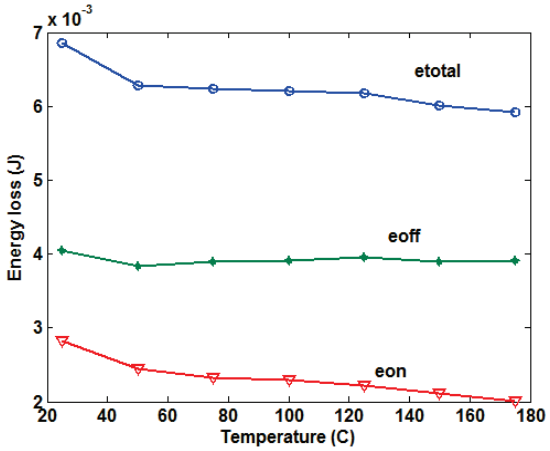


Figure 19. Turn-on and turn-off waveform of 1200 V, 100 A SiC MOSFET module at 800 V.

3.2. ORNL module-based inverter design

To take advantage of the high-temperature operating capability of WBG devices, device packages that can withstand high temperatures are required. Various organizations are working toward high-temperature packaging for high-temperature devices. Several high-temperature packages have been reported in recent years that include discrete device packages to power modules. This project focuses on the development of high-power-density power modules, which will enable size and volume reductions at the system level by integrating low-temperature components with high-temperature active devices and reducing the amount of material used to build the heat exchangers in inverters. This prototype uses single-sided cooling for the power modules, which are mounted using spring pressure. Thermal grease serves as the heat transfer medium from the lower side of the direct-bond copper (DBC) boards. This model of the prototype will be packaged as shown in Fig. 20, with controls and capacitors closely packaged to the heat sink.

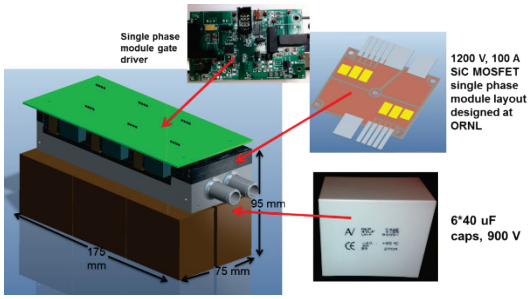


Figure 20. Layout of the 10-kW SiC inverter.

3.2.1. Power module development

An SiC MOSFET-based phase-leg module designed and developed in the internal packaging facility at ORNL is shown in Fig. 21. Figure 22 shows the layout of the die and interconnection pattern. The module includes four SiC MOSFETs and two SiC diodes, which form a totem pole or phase leg (half-bridge) configuration, a building block for an inverter. The package is designed to work at a temperature of at least 200ºC ambient. The electrical interconnection is achieved by bonding aluminum (Al) wires on top of the dies and soldering dies on the Cu traces of DBC substrates, which offer electrical insulation with their ceramic slice inside. The layout of multiple SiC dies on the DBC substrate and their interconnections has been optimized to reduce parasitic electric parameters.

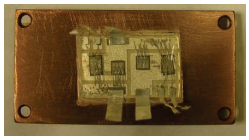


Figure 21. ORNL high-temperature SiC phase-leg module.

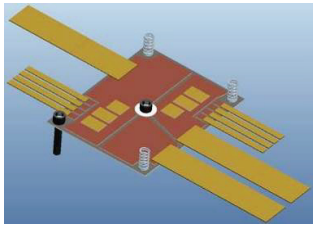


Figure 22. Power module layout design.

3.2.2. Characterization of the SiC module

Figure 23 shows forward characteristics of the (1200 V, 100 A) SiC MOSFET for different operating temperatures from 25 to 150°C in 25°C increments. SiC MOSFETs exhibit a linear relationship between the voltage and current and can be modeled as resistors.

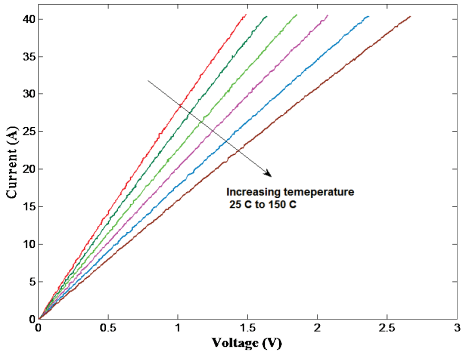


Figure 23. Forward characteristics of 1200 V, 50 A SiC module.

A standard commercial driver IC from IXYS, IXDN509, was used in the drive circuit for both devices. The driver can provide a peak output current of 9 A with a maximum output resistance of 1 Ω. The output stage of the drive includes resistor R2 and capacitor C1 for transient current and parallel resistor R1 for static current. The device turn-on and turn-off times are controlled by selecting the values of capacitor C1, and the resistor dampens the oscillation caused by C1 and the parasitic inductance of the circuit. A negative gate voltage of –5 V was chosen for the SiC MOSFET. The resistor R1 in the range of 9–15 Ω for Vcc of 20 V, the capacitor C2 in the range of 10–100 nF, and the resistor R2 in the range of 1–7 Ω were tried to achieve a high dynamic gate current during switching. A schematic of the gate drive circuit topology is shown in Fig. 24.

Switching measurements (double pulse tests) were performed to characterize the SiC MOSFET dynamically. The actual test setup is shown in Fig. 25. A load inductance of 120 uH and a 1200 V, 30 A SiC JBS freewheeling diode were used for all the tests. The total energy losses of the devices were obtained at 800 and 600 V and at different currents up to 35 A (Figs. 26 and 27).

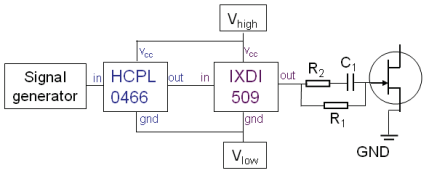


Figure 24. Schematic of the drive circuit.

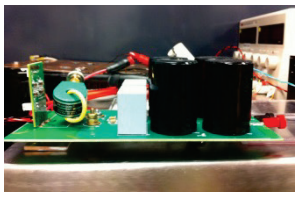


Figure 25. Experimental test setup for dynamic characterization of the 1200 V, 100 A SiC module.

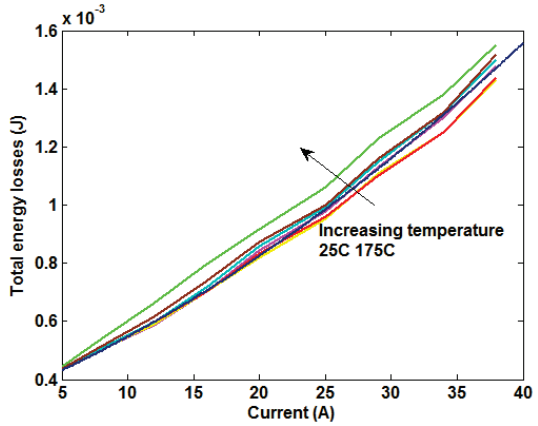


Figure 26. Total energy losses of the SiC MOSFET at 600 V.

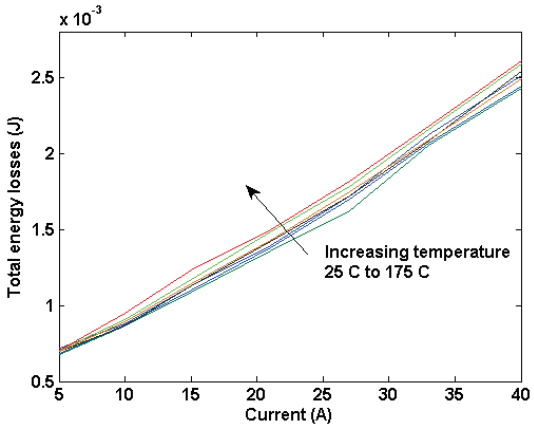


Figure 27. Total energy losses of the SiC MOSFET at 800 V.

4. Inverter Assembly and Testing

The final inverter assembly inverter is shown in Fig. 28. For this test, the dc-link voltage was fixed at nominal operating voltage (325 V) to the maximum bus voltage (450 V). The load resistance was set to the minimum value, and the current was controlled by changing the modulation index. The coolant was set at 20°C at a flow rate of 1.5 gpm. The open-loop frequency of operation and the PWM frequency were fixed and the current command was varied for a particular dc-link voltage. The command current was increased in steps without exceeding the power rating of the inverter or of the load. The coolant temperature was changed to 60ºC and data were recorded for a wide range of current and switching frequencies. The experimental waveforms for 325 and 450 V operation are shown in Fig. 29.

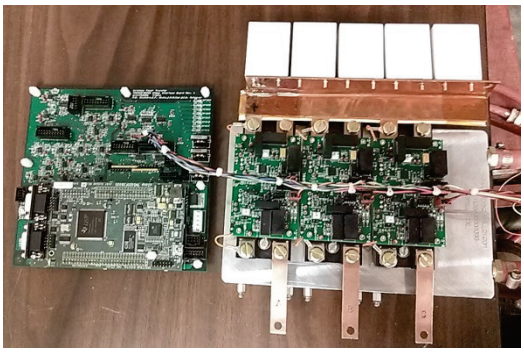
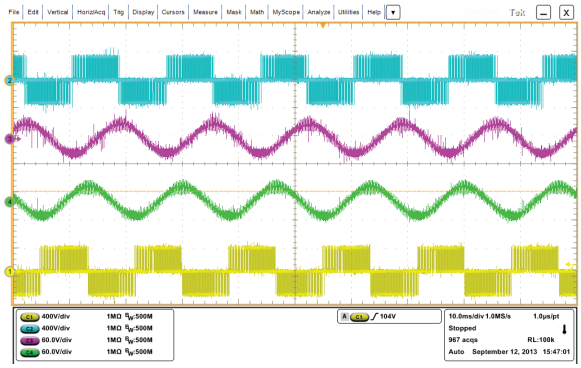
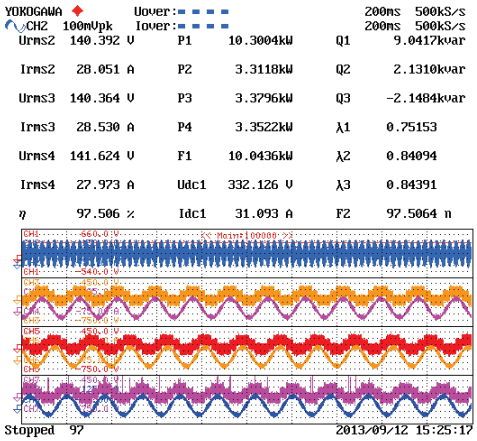


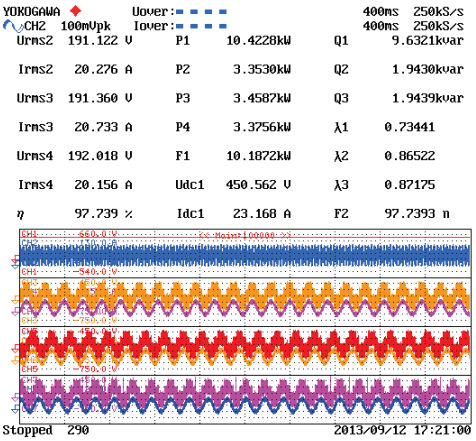
Figure 28. Final assembled inverter prototype.



(a)



(b)



(c)

Figure 29. Experimental waveforms of 10 kW SiC inverter. (a) 450 V dc-link voltage (b) screen shot of 325 V dc-link operation (c) screen shot of 450 V dc-link operation.

The efficiency versus output-power plot for several operating conditions, comparing efficiencies at different voltages, is shown in Fig. 30. Inverter efficiencies are higher at the 450 V than at the 325 V operating condition, as expected. Figure 31 shows that the inverter efficiency does not change much as the switching frequency increases. The overall inverter efficiency is ~98% for different operating conditions.

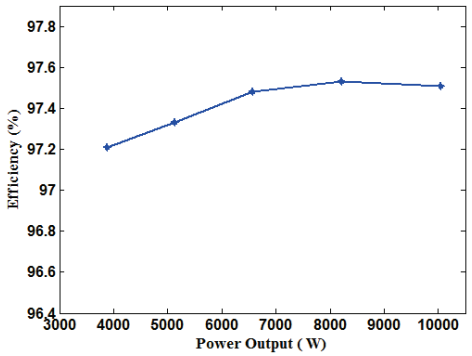


Figure 30. Inverter efficiency vs. output power.

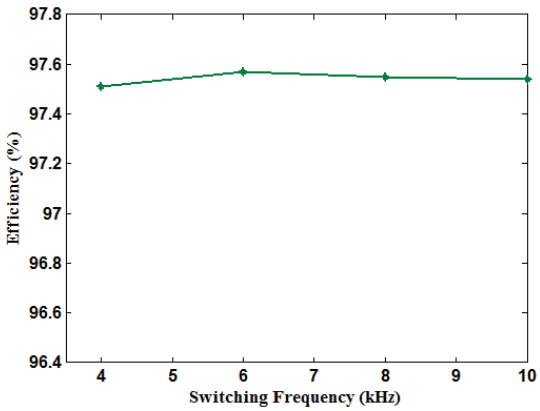


Figure 31. Inverter efficiency vs. switching frequency.

5. Air-Cooled inverter

ORNL has worked with the National Renewable Energy Laboratory (NREL) to develop an air-cooled inverter to further optimize the thermal design. The air-cooled inverter developed in FY 2011 was redesigned using thermal simulations from NREL. The initial inverter size was reduced by 33% through fin design optimization (Fig. 32). Balance-of-plant analysis is currently being conducted to establish the feasibility of air cooling at the system level.

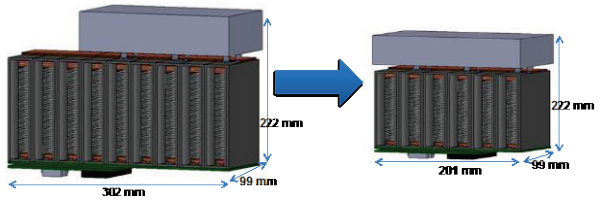


Figure 32. Air-cooled inverter design layout.

Conclusion and Future Directions

WBG device evaluation will continue until the technology transitions to industry. The inverter test results obtained this year will be used as a benchmark for a next-generation inverter to be built using ORNL PEEM's WBG package. The results obtained show that if the inverter is scaled to 30 kW, it will meet the 2020 VTO targets. They also show that WBG technology will aid in achieving U.S. DRIVE targets for volume, efficiency, power density, and system costs.

2.3 Benchmarking Competitive Technologies

Tim Burress (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1216; Fax: 865-946-1400
E-mail: burressta@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 2012
Projected End Date: Ongoing

Objectives

- Benchmark HEV/EV components
  - Assess design, packaging, and fabrication innovations in subsystems and components
    - Determine techniques used to improve specific power and power density and reduce cost.
    - Perform compositional analysis of key components.
  - Examine performance and operational characteristics during comprehensive tests and evaluations
    - Obtain peak torque and power capability
    - Identify detailed information regarding time-dependent and condition-dependent operation
  - Compile information from evaluations and assessments
    - Identify new areas of interest
    - Compare results with other EV/HEV technologies and DOE targets.

Technical Barriers

- Integrating custom ORNL inverter-motor-controller with original equipment manufacturer (OEM) components
  - Optimizing controls for nonlinear motors throughout operation range
- Intercepting, decoding, and overtaking OEM controller area network (CAN) signals
- Adapting nonstandard motor shaft and assembly to dynamometer and test fixture

Technical Targets

- This project helps with program planning and the establishment and verification of all DOE 2020 targets.

Accomplishments

- Overall: Conducted thorough benchmark assessments and reported on many HEV/EV technologies, including the following:
  - 2004 Prius, 2006 Accord, 2007 Camry, 2008 Lexus LS 600h, 2010 Prius, 2011 Hyundai Sonata motor, 2012 Nissan LEAF, 2012 Hyundai Sonata hybrid starter-generator (HSG)
- FY 2013
  - Conducted comprehensive teardown assessment and testing/evaluation of the 2013 Nissan LEAF 6.6 kW onboard charger
  - Procured and disassembled 2013 Toyota Camry power converter unit (PCU) and determined device characteristics
  - Performed dynamometer testing of Remy induction motors (IMs; one with Al and one with Cu rotor bars)
  - Performed dynamometer testing of the 2012 Hyundai Sonata HSG

✧ ✧ ✧ ✧ ✧

Introduction

Benchmarking plays an important role in program planning efforts by defining the current state of the art for components and subsystems, defining performance and design metrics for DOE's competitive R&D efforts, and identifying technology gaps to provide guidance on future research focus areas. To establish practical targets, baseline technological status must be obtained from subsystems currently in the marketplace. Therefore, benchmarking cutting-edge technologies in competitive global markets establishes a solid technology baseline for the DOE APEEM program. It also assists in determining if performance goals established for the program are realistically achievable and if they present sufficient challenge to warrant a robust program.

Benchmarking activities also ensure that the DOE APEEM program will not duplicate technical innovations found in commercially available technologies. They provide technical insight, allowing the DOE program to move more rapidly by maintaining awareness of current trends and technical innovations in advancing on-the-road technologies. Findings and results from the benchmarking efforts are detailed in reports and presentations. These publications are frequently cited in technical conference papers and have received high recognition from industry, academia, and car enthusiasts.

Approach

Appropriate HEV and EV components are selected by DOE based on information from the Internet, technical publications, published specifications, and feedback from automotive manufacturers and suppliers. Several components were evaluated in FY 2013 and each is discussed in the following sections.

2013 Nissan LEAF 6.6 kW charger

With the recent advent of the first mass-produced fully-EV, the Nissan LEAF, it is important to note that the onboard charger (OBC) is a critical component that impacts overall efficiency and the cost to operate the vehicle. The charger requires several power stages and many components, so there are significant associated cost and design requirements. The Nissan LEAF inverter and motor were benchmarked by ORNL in FY 2012 and the results published. The 2012 LEAF includes a 3.3 kW OBC, and the 2013 LEAF upgraded to a 6.6 kW charger, both of which accept ac power in standard forms (i.e., 120 and 240 V). A separate "fast-charging" port is available that accepts dc power from a large off-board charger.

The focus of DOE's APEEM program is on components and subsystems; therefore, the entire vehicle was not procured and used during analyses of the LEAF's OBC. Various standards (namely SAE J1772) are in place to regulate charger functionality and impact on grid power quality (IEEE 519). Since harmonic analysis for total harmonic distortion (THD) and other metrics related to standards requires the entire system, ORNL focused on obtaining design, functionality, and operational characteristics at a detailed subsystem level. This includes destructive teardown and invasive investigations to determine the layout and connectivity of all items in the charger. ORNL evaluated the operation of converter stages by implementing custom-developed control algorithms, and plans are being developed to compare the custom controls and ensure that they closely mimic OEM controls on a fully operational vehicle.

2013 Toyota Camry power converter unit

The 2013 Toyota Camry was selected for Stage 1 benchmarking assessments, which include disassembly for design, functionality, and volumetric assessments as well as device characterization. Although this does not include testing on a dynamometer, valuable information in regard to advancing on-the-road technology can be gained without devoting the resources required for full dynamometer testing. This facilitates the capability to obtain benchmark information on the components while components from other vehicle models are prepared for evaluation with a dynamometer.

Remy induction motor testing

The most common type of electric motor used in EV/HEVs is the permanent magnet (PM) motor with neodymium-iron-boron magnets. Recent R&D efforts involve the development of electric motors that do not use RE materials, which have a history of high and uncertain costs. The IM is a possible alternative, but in general, detailed operational characteristics (such as efficiency maps) are not readily available for induction motors. Remy offered to provide ORNL with two pre-production IMs, one with Cu rotor bars and one with Al rotor bars. ORNL designed and fabricated the appropriate high-precision shaft and alignment/support fixture. Additionally, ORNL implemented an inverter drive system and developed motor control algorithms to optimize motor operation with respect to efficiency.

2012 Hyundai Sonata hybrid starter-generator

The Hyundai Sonata HSG was chosen because it is seen as a component that can facilitate the hybridization of existing vehicle product lines. The HSG is slightly larger than a conventional alternator, yet it replaces not only the alternator but also the starter for the combustion engine. It is belt-driven by the engine crankshaft pulley, and it is more efficient than a conventional alternator since it operates at the hybrid battery voltage (270 V) as opposed to the conventional alternator/ battery system 12 V. The primary hybrid motor of the Hyundai Sonata is about the same size as the non-hybrid's automatic transmission torque converter, and it essentially replaces the torque converter. Therefore, this is a convenient approach to hybridizing an existing vehicle design without major modifications to the drivetrain components. The HSG was tested on a dynamometer in both motoring and regenerative mode. The primary drive motor was benchmarked in FY 2012 and the results were published.

Results

2013 Nissan LEAF 6.6 kW charger

Design and functionality assessments

The 2013 Nissan LEAF charger is shown on the upper left in Fig. 1. As received, the mass of the charger was about 16.3 kg, which includes the mass of the external off-white line filter and its support bracket weighing a total of 3.2 kg. The main charger assembly width and length are about 9.9 and 10.9 in., and the height varies from about 3 to 4.5 in., giving a volume of approximately 11.1 L. Using these metrics with a power rating of 6.6 kW, the specific power and power density are 0.4 kW/kg and 0.6 kW/L, respectively. These figures seem quite low, but it should be noted that the charger operates continuously at a power level of 6.6 kW, and isolation and power quality specifications required by standards ultimately require additional components.

The underside of the charger assembly is also shown in Fig. 1, where cast (then machined) Al channels for liquid cooling with a water ethylene-glycol mixture are visible. The internal compartment includes a control-communication circuit board, a driver and signal conditioning board, a black power module, large passive components for various charger stages, and many smaller devices and peripheral passive components. The control board includes a Renesas R5F71476FPV microcontroller, which is the type of microcontroller used for the Nissan LEAF motor controller.

The block diagram in Fig. 1 describes the various stages of the OBC and indicates where the associated devices are located in the power module. The corresponding circuit schematic is shown in Figs. 2 and 3. Note that the latter two figures are actually one schematic, but they are separated for image clarity. Also note there is only one 310 V, 1 μF and 420 V, 2,700 μF capacitor in the circuit, and it is duplicated in both figures as a reference item. After the external line filter, the ac input of the

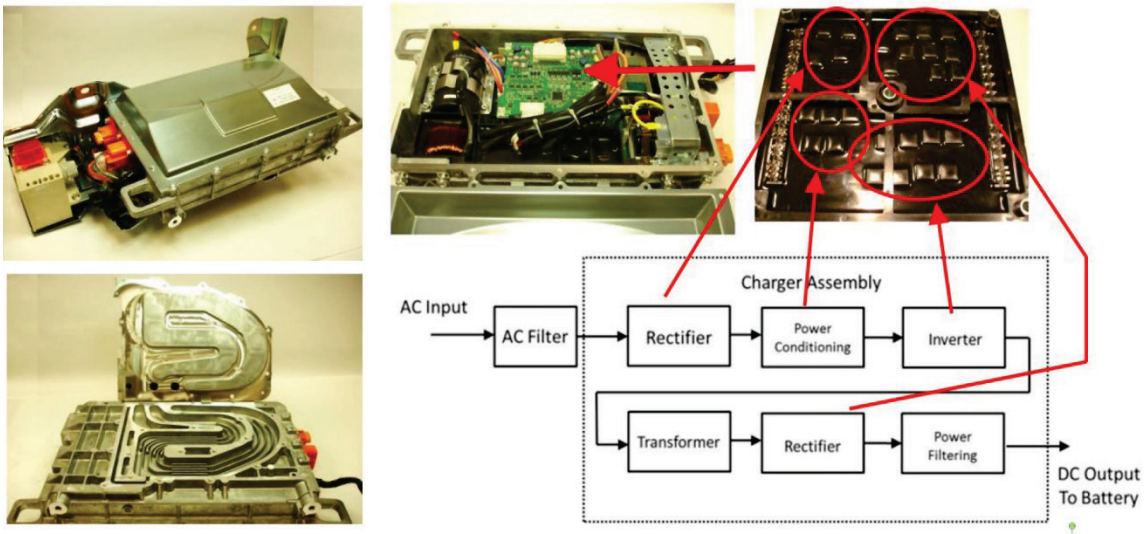


Figure 1: Nissan LEAF charger ac input and boost-PFC.

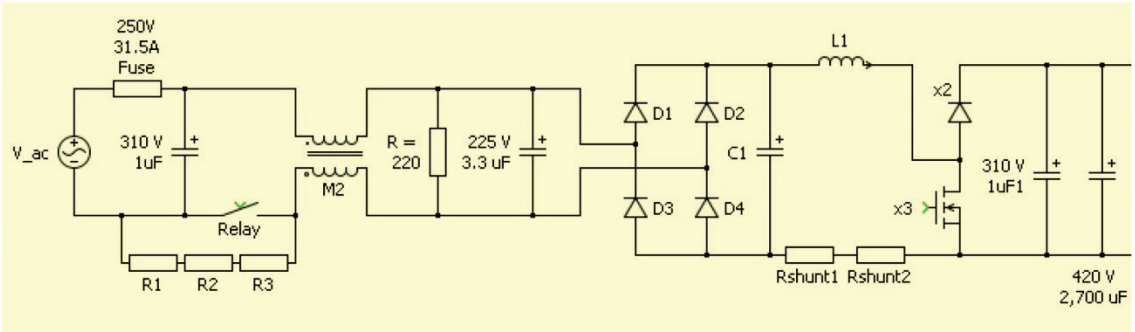


Figure 2: Nissan LEAF charger ac input and boost-PFC.

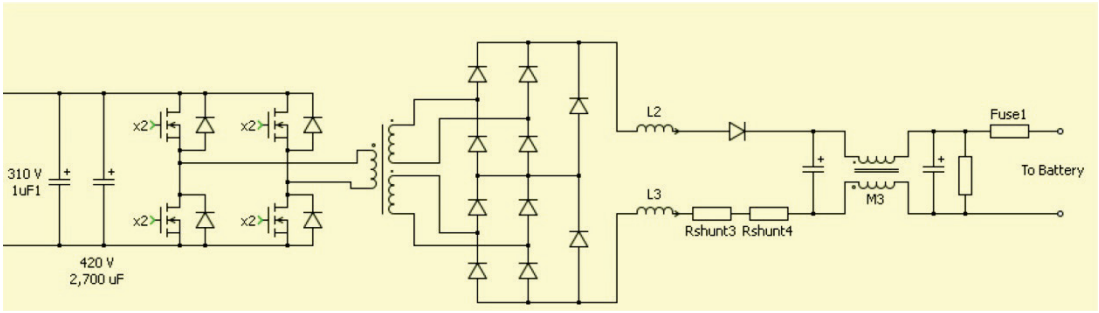


Figure 3: Nissan LEAF charger isolation and rectification stage.

charger is fused and additional filtering (including common mode) is applied with relatively small passive components. A relay remains open until ac voltage has been applied for a certain amount of time to avoid high in-rush currents by charging system capacitors through three resistors. The first conversion stage of the charger is a conventional rectifier with four diodes. The next stage is a boosting power factor correction (PFC) stage, which includes three MOSFETs in parallel for chopping action, and two diodes in parallel to prevent reverse current and to allow energy to be stored in the inductor as the MOSFETs are active. The boosted voltage is regulated to between about 360 and 400 V, and a large 420 V, 2,700 μF electrolytic capacitor is located at the boosted output.

The final stages of the charger, shown in Fig. 3, include an H-bridge inverter with two MOSFETS for each switch and one small anti-parallel diode for each switch. The inverter drives the primary coil of the large isolation transformer, which has two secondary windings. Output from the two secondary windings is fed to two full-bridge rectifiers, with outputs placed in series and balancing diodes in parallel with each rectifier. In total, ten diodes are located in the final rectification stage. The rectified output is fed through two large inductors, a diode (not located in the power module), a common mode filter, and

small passive filters before passing through the output connector that connects to the battery.

The battery voltage varies with the state of charge; therefore, the output voltage of the charger must have a fairly wide range to maintain a constant charging power level and avoid overcharging conditions. It can be roughly estimated that the charger output voltage is in the range of 300–400 V for normal charging conditions.

Testing and characterization

Since the operation of the charger is largely dependent on battery characteristics and OEM controls, as the charger is operating with the battery pack, ORNL performed basic operational tests to verify assessments made during functionality studies. ORNL is working to establish a collaboration with other organizations that perform full-vehicle assessments to verify and analyze in situ operational characteristics. However, the invasive efforts required to obtain this information create a difficulty: there is some risk of compromising vehicle integrity/value, and most test vehicles are borrowed or will be used in company fleets. Nonetheless, system-level efficiencies are easier to obtain. Argonne National Laboratory performed full-vehicle testing and reports that the 3.3 kW 2012 LEAF charger and EV service equipment have a total efficiency of about 86.3%, which is the efficiency from the ac receptacle to the dc power input to the battery.

In carrying out basic operational tests, it was discovered that the driver circuitry for the H-bridge inverter is unconventional, as the MOSFETs are controlled with only the power isolation transformer and no additional control signal isolation (i.e., optocoupler) is used. This is possible largely because the H-bridge is controlled with phase-shift control and therefore variable pulse width is not used. Additionally, it appears that the dead-time is generated on the output of the secondary with passive components.

2013 Toyota Camry power converter unit

Design and functionality assessments

The 2013 Toyota Camry PCU is manufactured by Denso and has a total mass of 15.3 kg and a volume of about 12.3 L. The PCU, shown in Fig. 4, serves functions similar to those of many Toyota PCUs, including motor inverter, generator inverter, bi-directional boost converter, and dc-dc converter to convert the hybrid battery voltage to 12 V for auxiliary loads. Note that the first-generation Camry PCU does not include the 12 V dc-dc converter. The boost converter boosts the hybrid battery voltage of about 244 V up to a maximum of 650 V. Sections of the PCU are labeled on the right side of Fig. 4. The uppermost portion of the PCU contains the control and driver circuitry, which is shown in Fig. 5. The upper middle section contains the power modules, cooling infrastructure, and boost inductor; and the lower middle section houses the large capacitor module. The bottom section contains the 12 V dc-dc converter, and the output terminal is labeled accordingly.

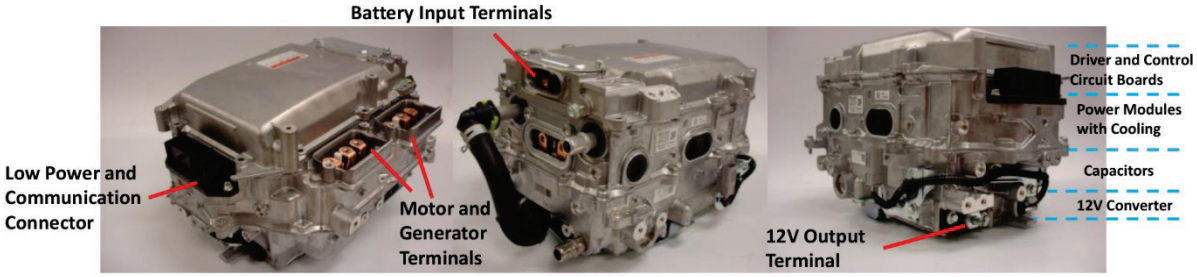


Figure 4: 2013 Toyota Camry power converter unit.

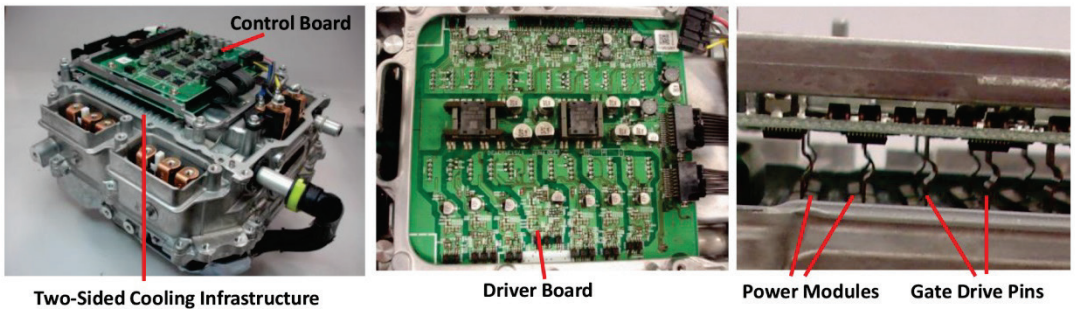


Figure 5: 2013 Toyota Camry circuit boards.

The mass and volume of the 12 V dc-dc converter are roughly 3.1 kg and 1.45 L, and the boost converter, motor inverter, and generator inverter account for about 12.2 kg and 10.9 L. The PE devices for the boost converter and both inverters are located together; they were in separate locations in previous Camry designs. This transition has been made in most recent Toyota/Lexus PCUs.

There are a total of 12 phase legs, three dedicated to the 3-phase generator inverter, six (two in parallel for each phase) used for the inverter, and three in parallel for the boost converter. Therefore, the motor inverter mass and volume can

be approximated to be about 6.1 kg and 5.5 L, respectively. Using the published motor power rating of 105 kW, the specific power of the motor inverter is 17.2 kW/kg and the power density is 19 kW/L.

The 105 kW power rating has not been verified during dynamometer testing. Also, a critical factor that yields improved power density and specific power is the high voltage enabled by the boost converter (and partially by regenerative power from the combustion engine via the generator). If the boost converter mass and volume are included with the motor inverter, the power density and specific power are 12.7 kW/L and 11.5 kW/kg, respectively. Even so, these metrics are the highest for any PCU benchmarked thus far, and the improved performance is largely due to the use of power modules that are cooled on both sides.

The 2013 Toyota Camry PCU closely resembles that of the 2008 Lexus LS 600h, which also uses power modules with two-sided cooling. Each module includes one IGBT and one diode with control and sensing pins protruding upward to the driver board (Fig. 5) and Cu collector and emitter bus bars extending downward to the phase output and the negative or positive dc bus (Fig. 6). Thin ceramic sheets are located between both sides of the module and the adjacent cooing infrastructure, with thermal paste on both sides of each insulator. A large metal arch support is used to apply substantial mechanical pressure to the entire stack-up of power modules to ensure sufficient heat transfer is achieved.

A clear advantage of using power modules with two-sided cooling is realized by comparing the number of Si devices with that in the previous generation. For each switch, the previous generation used three IGBTs/diodes in parallel, whereas the current generation uses only two IGBTs/diodes for the same power rating. In 2008, it was not clear whether Toyota was pursuing this type of design for mass-produced vehicles, as the 2008 LS 600h luxury sedan had relatively low production volume and a base sale price of $104,000. Although fewer devices are used in the current design, there are cost tradeoffs with the Cu bus bar infrastructure, costly ceramic insulators, and increased requirements to overcome mechanical stresses due to mismatching of coefficients of thermal expansion on both sides of the power devices.

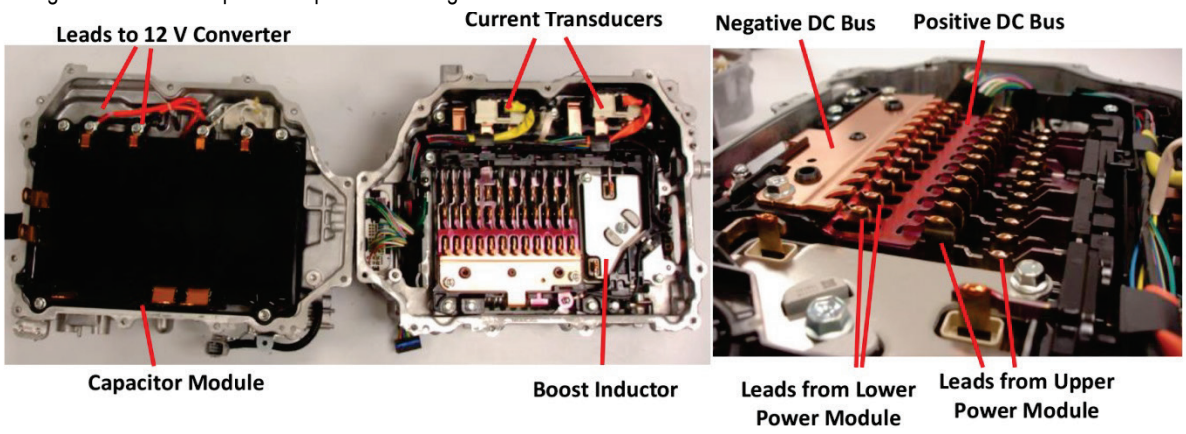


Figure 6: 2013 Toyota Camry capacitor, dc bus, and power modules.

A 420 V, 320 μF boost capacitor (connected to the battery input) and 750 V, 1,600 μF dc link capacitor are both located in the same module. It is manufactured by Panasonic and it contains internal bus bars that connect the battery input to the dc link and boost inductor, a ~70 kohm bleed resistor, and the 12 V dc-dc converter. In addition to the two-sided cooling infrastructure, a cast Al heat exchanger cools the 12 V dc-dc converter, which mates to the bottom of the cooling surface. The capacitor mates to the top side of the heat exchanger, but there is no additional material (e.g., thermal paste) to facilitate thermal coupling between the case of the capacitor module and the heat exchanger.

Overall, compared with the 2008 LS 600h PCU, it is clear that the design and packaging of the 2013 Camry PCU has been improved with less wasted space, simpler bus bars, and reduced driver and control circuit board complexity. It will be interesting to see if Toyota will use the two-sided cooling approach in other product lines.

Testing and characterization

Device characterization was performed on an IGBT from one of the 2013 Camry power modules. The current vs. voltage characteristic curve is provided in Fig. 7. At 200 A, the forward voltage drop of the IGBT is about 2 V. Therefore, the power loss at this operation point is about 400 W, and with two in parallel (for the motor inverter), the total conduction loss is 800 W at this operation point. The peak current required by the motor to produce peak torque is estimated at between 400 and 500 A. To derive inverter efficiency, switching losses and diode losses also need to be included, but for six-step operation at high speeds, switching loss contributions drop significantly, and so it is possible to attain inverter efficiencies above 99%, considering the peak power of 105 kW.

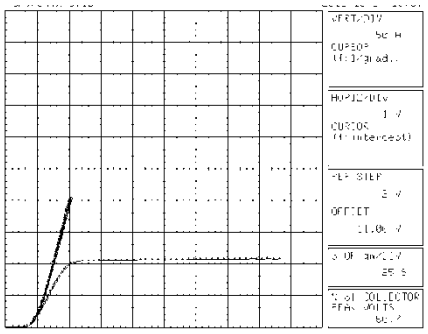


Figure 7: 2013 Toyota Camry device characteristics.

Remy induction motor characteristics

Remy provided 3-phase IMs with 10 poles, a maximum dc voltage of 700 V (~480 V peak ac), and a maximum current of 300 A (rms). The motor is cooled with automatic transmission fluid and has a maximum speed of 10,600 rpm. As shown in Fig. 8, simulation results from Remy predicted that the motor will produce a peak torque of about 320 Nm, a peak power of 180 kW, and efficiencies above 90% for peak power operation points over much of the operational speed range.

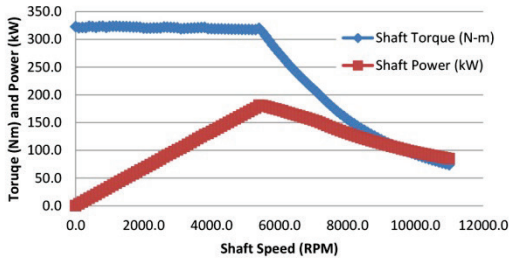


Figure 8: Simulated performance of induction motor.

Design of a mechanical interface was required to adapt the IM to ORNL's test setup. As shown in Fig. 9, a custom high-precision face-mount adapter and spline adapter shaft were designed and fabricated by ORNL. Also shown in Fig. 9 is the IM on the dynamometer test system with the oil cooling system. Both peak torque and efficiency results have been verified, but operation at a peak power of 180 kW has not yet been verified. ORNL is working with Remy to ensure proper control conditions are being met; detailed performance and efficiency information will be reported thereafter.

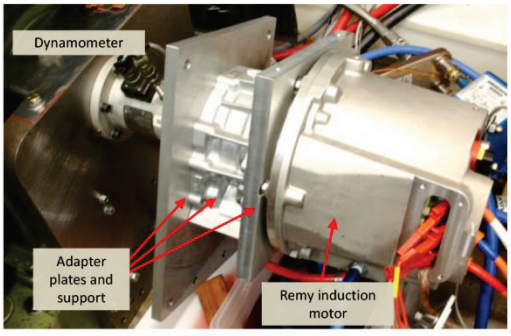


Figure 9: Adapter, shaft, and Remy induction motor in dynamometer test cell.

2012 Hyundai Sonata hybrid starter-generator

Design and functionality assessments

Although the PCU of the Hyundai Sonata hybrid has been reported upon in the past, a brief overview will be given since the PCU also contains the controls and PE that drive the HSG. The PCU assembly is shown in Fig. 10, where the compartments are identified according to their functionality. Both the HSG and primary motor operate off the same dc link, which is connected to a battery with a nominal voltage of 270 V. A water ethylene-glycol mixture cools the PCU, which has a cast Al heat exchanger. The upper section contains the 270 to 12 V dc-dc converter, and the lower section contains the HSG and motor drive components with interconnects labeled accordingly.

HSG and motor control boards are shown on the left in Fig. 11, with details regarding integrated circuitry and other notable information indicated. As shown on the right in Fig. 11, the HSG and motor PE modules are the same size, although the published power ratings for the HSG and primary motor are 8.5 kW and 30 kW, respectively. Detailed information about the PE module is shown in Fig. 12. Inverters for both the HSG and motor use two IGBTs and two diodes in parallel for each switch of the 3-phase inverter, giving a total of 12 IGBTs and 12 diodes. The IGBTs and diodes in the HSG inverter are roughly 8.9 by 6.0 mm and 6.6 by 4.0 mm, respectively. These are notably smaller than the IGBT and diode dimensions of the motor inverter, which are 10.2 by 9.7 mm and 9.2 by 5.41 mm, respectively.

The HSG assembly, shown in Fig. 13, is slightly larger than a conventional alternator. It mounts to the side of the engine and is belt-driven, similar to a conventional alternator. Published specifications for the HSG indicate that it is capable of producing a peak torque of 43 Nm and peak power of 8.5 kW and operating at up to a maximum speed of 15,750 rpm. The HSG replaces the conventional starter (which is gear and sprocket driven); it starts the engine from a cold start and restarts during stop-and-go driving conditions. Additionally, the HSG operates as a generator when the battery has a low state of charge, allowing the engine to replenish the battery pack even when the vehicle is not in motion. The overall mass and volume of the HSG are about 12 kg and 3.1 L, respectively.

The stator and rotor of the HSG, shown in Fig. 14, have masses of 5.1 kg and 2.0 kg, respectively. The 3-phase machine is an IPM machine with 36 stator slots and six poles, as is evident by the magnets shown on the right in Fig. 14. Each rotor pole consists of two magnets along the axial direction of the rotor. This is a common practice, as eddy currents within the magnets are reduced by segmenting them along the axial direction, an effect similar to that of using laminated steel. A resolver, shown in Fig. 13, is used for absolute position sensing. It has 12 stator poles and 3 salient lobes on the rotor. A thermistor is installed in the stator windings to monitor motor operation temperature, and it is accessed via the same connector as the resolver.

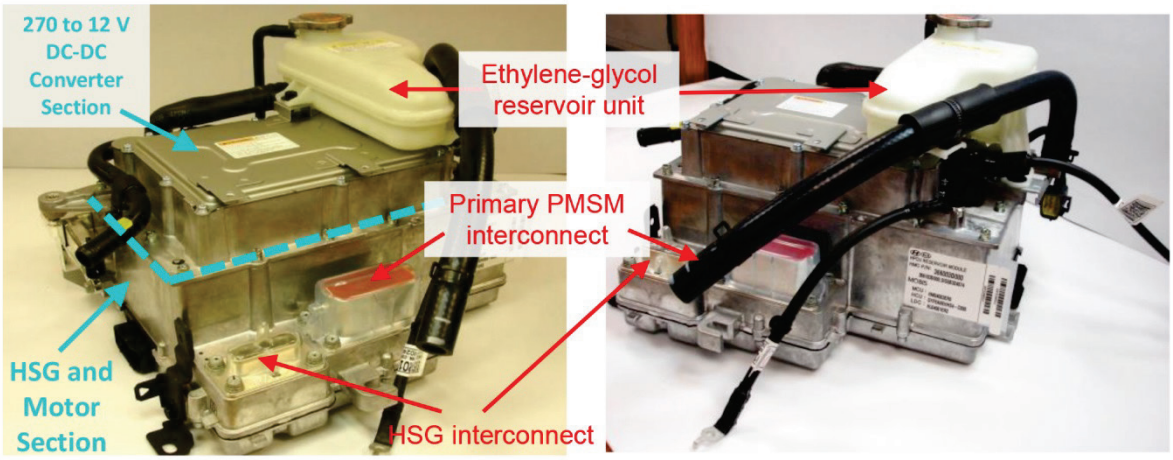


Figure 10: 2012 Hyundai Sonata power converter unit.

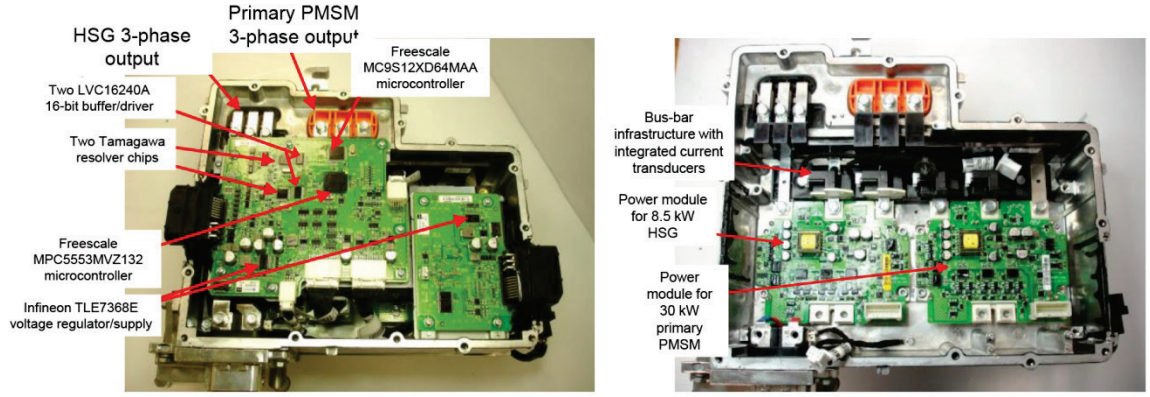


Figure 11: 2012 Hyundai Sonata control boards (left) and power modules (right).

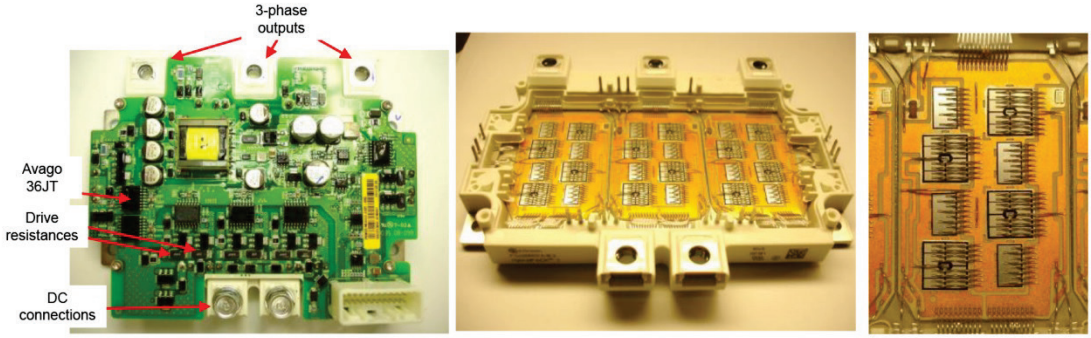


Figure 12: 2012 Hyundai Sonata HSG power module.

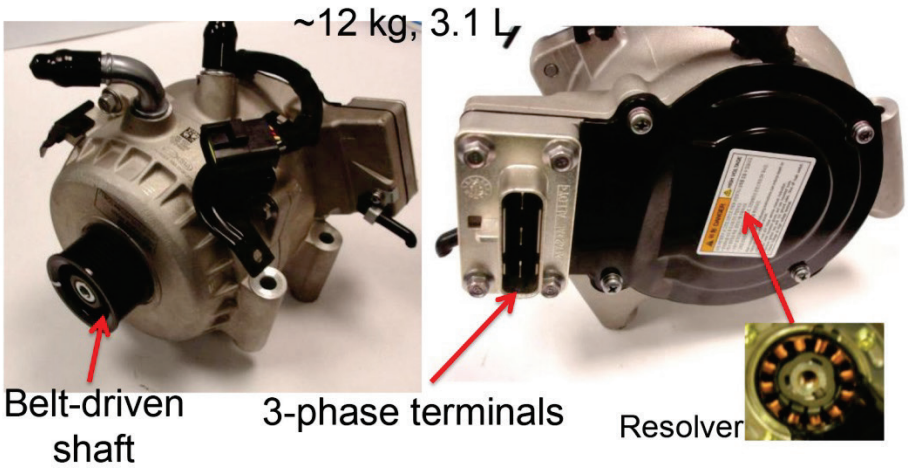


Figure 13: 2012 Hyundai Sonata HSG assembly.

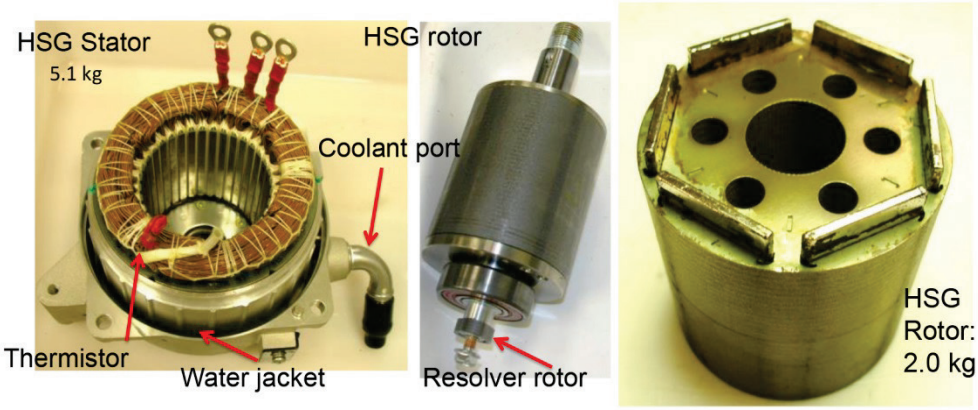


Figure 14: 2012 Hyundai Sonata HSG components.

Testing and characterization

The HSG was tested using the OEM PCU but with custom motor software controls developed and implemented by ORNL. Both motoring and regenerative operate mode were analyzed while efficiency, various temperatures, dc voltage, dc current, ac voltages, ac currents, mechanical power, ac electrical power, dc electrical power, and many other metrics were recorded at each operation point. The efficiency map in Fig. 15 indicates the measured HSG efficiency as it operated in motoring motor. It can be seen that the peak efficiency is about 88% for high loading between 6,000 and 8,000 rpm. Note that belt losses are included in this efficiency map, and in general they contribute 1–2% of the loss at high power levels and about 3–6% of the loss at low and moderate load levels.

One major finding of the tests is that the HSG actually operated above 20 kW, although the published power level is only 8.5 kW. All efficiency maps have a light-grey trace superimposed for operation at 8.5 kW and a light-green trace superimposed for operation at 20 kW. These curves simply portray the torque required to produce the given power level (8.5 or 20 kW) at each speed. This gives a clear picture of the nature of operation above 8.5 kW and 20 kW. Note that the peak efficiency is only 84% if the HSG operates within the published 8.5 kW power rating.

An efficiency map for the HSG inverter during motoring mode is shown in Fig. 16. The peak HSG inverter motoring efficiency reaches above 98% even if operation is kept below 8.5 kW. The combined (inverter and motor) efficiency map for motoring operation is shown in Fig. 17. A peak combined efficiency of 87% is reached, and if operation is below 8.5 kW, the highest efficiency is 82%. The combined (inverter and motor) efficiency map for the HSG operating in regenerative mode is shown in Fig. 18. Note that although the torque is indicated as positive, it is actually in the opposite direction to that of the motoring plots; but regenerative torque is plotted in a similar manner to facilitate comparison. Combined system HSG efficiencies for regenerative mode are very similar to those of the motor mode, with a peak efficiency of 86% and only 82% if operating below 8.5 kW.

A plot of various temperatures and power versus time during continuous testing conditions is provided in Fig. 19. A power level of 8.5 kW at 5,000 rpm was maintained for about 30 min and the motor temperature stabilized at about 120°C. At 3,000 rpm, the motor temperature reached 160°C after 3 min of operation. Operation at 8.5 kW was maintained at 7,000, 9,000, and 11,000 rpm, and the motor temperatures stabilized at about 100°C for all three test conditions.

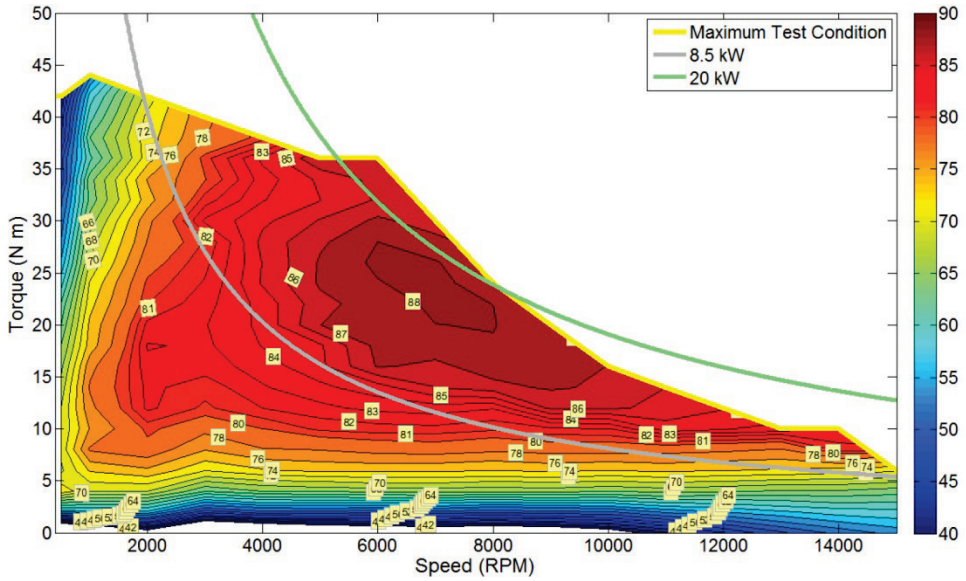


Figure 15: 2012 Hyundai Sonata HSG motoring efficiency (motor only).

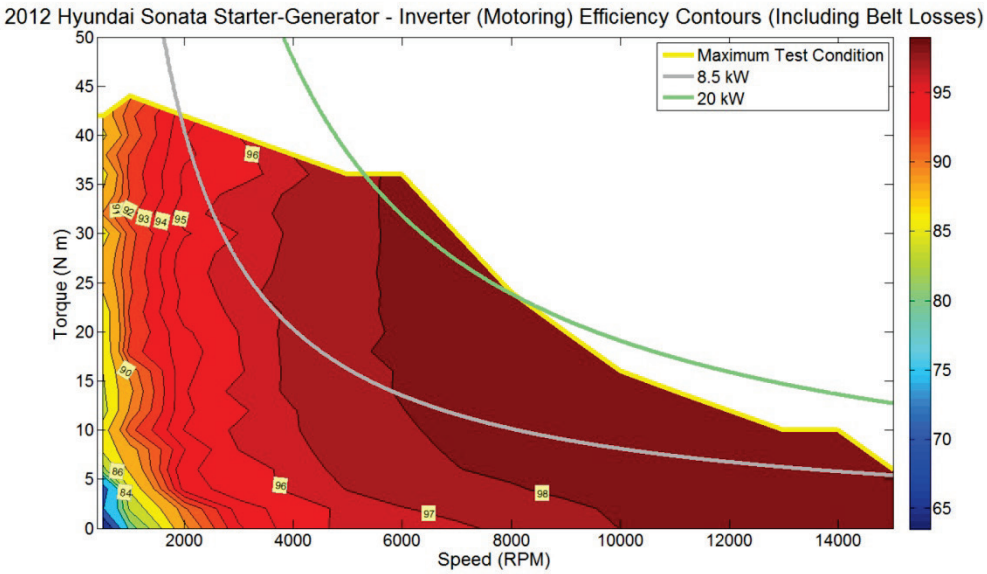


Figure 16: 2012 Hyundai Sonata HSG motoring efficiency (inverter only).

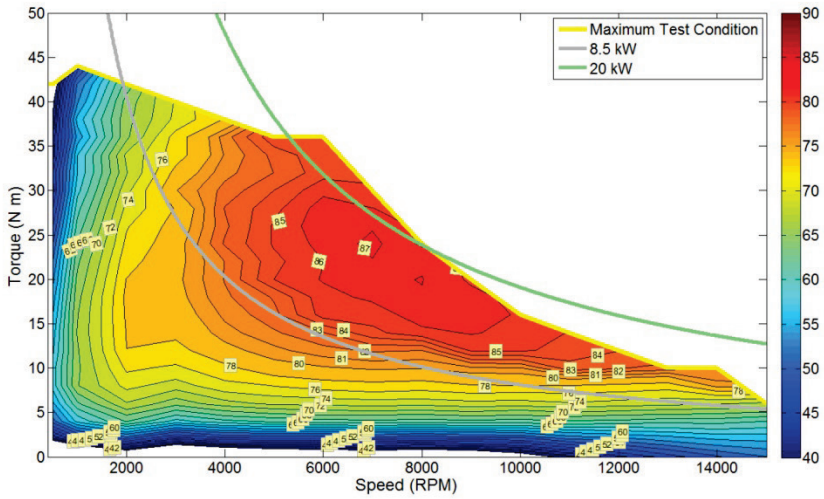


Figure 17: 2012 Hyundai Sonata HSG motoring efficiency (motor and inverter combined).

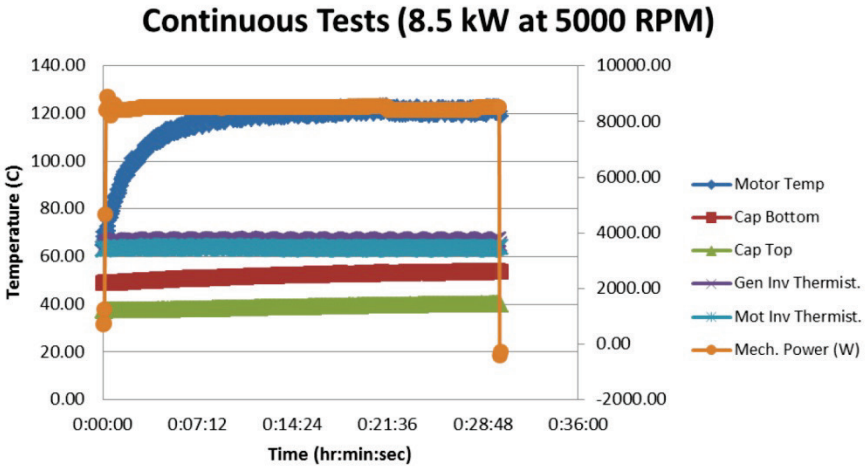


Figure 18: 2012 Hyundai Sonata HSG generating efficiency (motor and inverter combined).

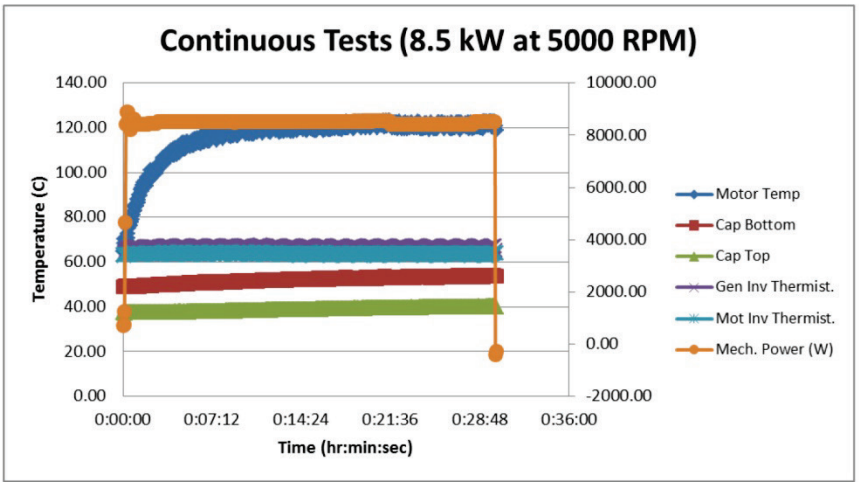


Figure 19: 2012 Hyundai Sonata HSG generating efficiency (motor and inverter combined).

Conclusions and Future Directions

Valuable information continues to be gathered on various EV/HEV components. Details of the 2013 Nissan LEAF charger design were determined and presented. Overall, the charger design uses mostly conventional techniques, except that the isolation stage includes a transformer with two secondary windings and the outputs are rectified with two full bridge rectifiers placed in series with balancing diodes in parallel with each full bridge. Conformational testing affirmed the anticipated functionality of the charger.

Details of the 2013 Toyota Camry PCU design were obtained and presented. The design is quite similar to that of the 2008 Lexus LS 600h, as it uses discrete power modules with cooling applied to both sides. This facilitates a 33% reduction in the number of devices required for the motor inverter, as smaller devices can be used because cooling is greatly improved. Power devices contribute a significant portion of the cost of the PCU.

IMs from Remy were tested and peak torque and efficiency were confirmed. ORNL is interfacing with Remy to ensure proper operation was implemented before publishing the results.

Dynamotor testing of the 2012 Hyundai Sonata HSG revealed that the PM machine is capable of operating well beyond its published peak power of 8.5 kW, up to about 24 kW. Peak combined efficiencies reached about 86–87% regardless of whether the HSG was operating in motoring mode or regenerative mode. A visual comparison of the motoring and regenerative efficiency maps reveals the slightly higher-efficiency behavior of the motoring mode. Although efficiencies are lower than for most machines benchmarked thus far, the HSG is much more efficient than a conventional alternator, which can be 50% efficient or less. Overall, the design is well suited for hybridization of mild and medium HEVs.

A summary of power density and specific power for motors and inverters that have been benchmarked is provided in Table 1.

Table 1: Comparison of specific power and power density for various EVs/HEVs benchmarked by ORNL.

Component & Parameter	2020 DOE Targets	2012 Leaf (80 kW)	2012 Sonata HSG 23 (8.5 kW)	2011 Sonata (30 kW)	2010 Prius (60 kW)	2008 LS600h Lexus (110 kW)	2007 Camry (70 kW)	2013 Camry (105 kW)	2004 Prius (50 kW)
Motor									
Peak power density, kW/L	**5.7**	**4.2**	**7.42** (2.7)	**3.0**	**4.8**	**6.6**	**5.9**		**3.3**
Peak specific power, kW/kg	**1.6**	**1.4**	**1.9** (0.7)	**1.1**	**1.6**	**2.5**	**1.7**		**1.1**
Inverter									
Excludes generator inverter (parenthetical values exclude boost converter mass/volume for Toyota Vehicles)									
Peak power density, kW/L	**13.4**	**5.7**	**5.6** (2.0)	**7.3**	**5.9** (11.1)	**10.6** (17.2)	**7.4** (11.7)	**12.7** (19.0)	**4.5** (7.4)
Peak specific power, kW/kg	**14.1**	**4.9**	**5.4** (2.0)	**6.9**	**6.9** (16.7)	**7.7** (14.9)	**5.0** (9.3)	**11.5** (17.2)	**3.8** (6.2)

FY 2013 Publications/Presentations

1. "Benchmarking EV and HEV power electronics and electric machines," presented at the IEEE Transportation Electrification Conference, June 2013.

2.4 System Integration and HIL Validation

Tim Burress (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1216; Fax: 865-946-1400
E-mail: burressta@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
E-mail: millerjm@ornl.gov

Susan Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 2012
Projected End Date: September 2013

Objectives

Overall Objectives:

Use ORNL's hardware-in-the-loop (HIL) system as a testing platform for development of next-generation TDSs.

- Validate converter, inverter, and motor performance using standard or custom drive cycles
- Provide feedback for DOE VTO APEEM program planning, target setting, and identification of R&D gaps
- Propose TDS refinements that address R&D gaps for the VTO APEEM program

FY 2013 Objectives

- Design and fabricate universal circuit boards needed for operation on the HIL system
  - Digital signal processor (DSP) control board
  - driver boards
- Work jointly with Vehicle Systems Integration (VSI) staff to define the needs of a high-performance dynamometer and other HIL components
- Perform subscale HIL testing with scaled motors

Technical Barriers

- Measurement of system and component efficiencies during transient conditions
- Limitations in refresh rates, continuous monitoring, and customizability of most commercially available power measurement systems

Technical Targets

- This project aids program planning and the establishment and verification of all DOE targets.

Accomplishments

- Completed design of universal control circuitry and board population
- Programmed and implemented DSP control board with driver circuitry needed in experimental test setup
- Built, programmed, and assembled power analysis equipment
- Developed and successfully operated subscale dynamometer system
- Designed, fabricated, and assembled custom IM with GlidCop and Al rotor bars for subscale testing
- Procured battery emulator and ordered dynamometer (by VSI team)

Introduction

Development and utilization of an HIL drive cycle testing platform for components expands testing and validation capabilities for prototype and commercial components. The expansion of HIL testing capabilities is important for DOE VTO program planning with regard to program portfolio development (by identifying development thrust areas) and target setting (perhaps additional ones) with consideration of system-wide impacts and characteristics. Drive cycle validation ensures prototype development is conducted with respect to realistic on-the-road operation. This project intends to increase the cohesiveness between DOE's APEEM and Vehicle Systems programs.

The VSI team at ORNL is developing an HIL platform for component testing that emulates drive cycle conditions by using a dynamometer that generates the appropriate torque (throughout a drive cycle speed reference profile) for environmental conditions (e.g., grade, temperature) and a given vehicle profile (e.g., mass, rolling resistance, drag coefficient). A functional diagram of the system is shown in Fig. 1. Items researched within DOE's APEEM Program are located within the green dotted boundary, and they constitute the primary focus of this project.

The system will use a battery emulator so impacts of converter or motor designs upon battery operation can be assessed. For example, if the size of the main inverter capacitor (one of the largest inverter components) is reduced, the full effect is not realized unless dc current ripple is monitored. A significant increase in current ripple will reduce the operational life of the battery; therefore, current ripple should be carefully considered in evaluating prototype designs. System-wide characteristics can be observed in

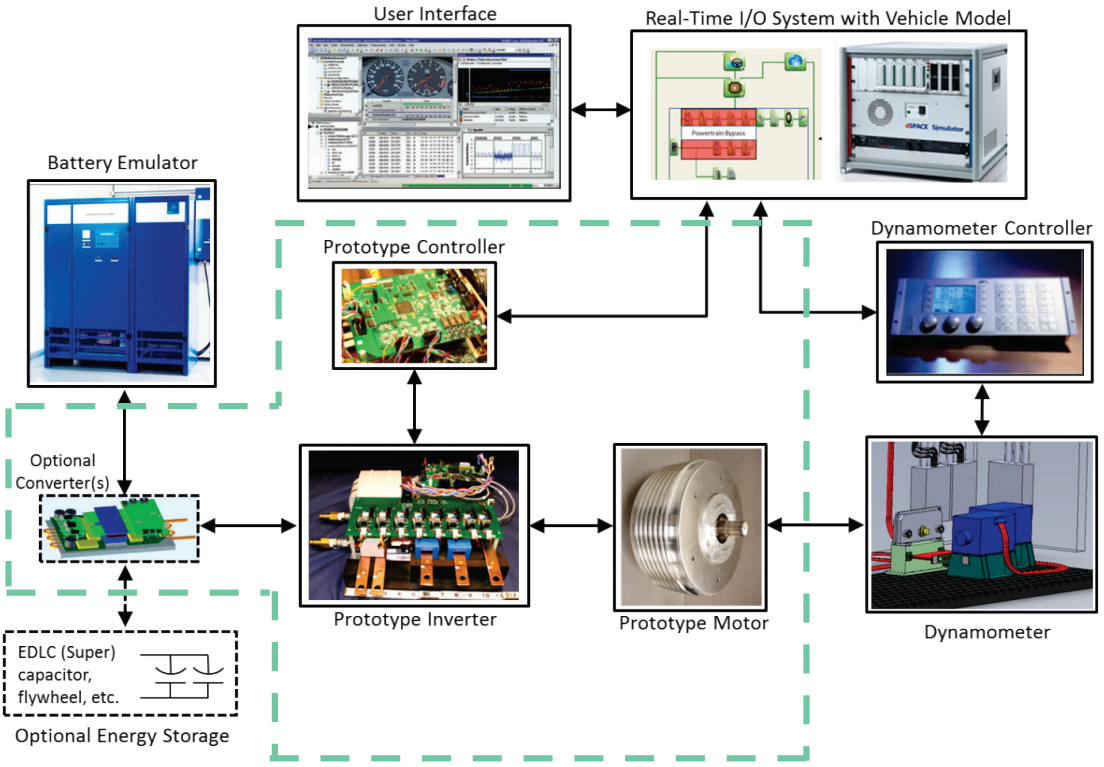


Figure 1: HIL testing platform under development.

evaluating requirements and impacts of operating with high dc-link voltages, which would require higher battery voltage levels or a bi-directional dc-dc converter. Another area of interest may be driveline matching, in which the impacts of various transmission architectures upon converter, inverter, and motor operation can be assessed. In combination with the emulation of vehicle operation described above, the HIL system will have the capability to emulate an EV transmission-transaxle or even HEV power split operation. Ultimately, the HIL system provides the capability to emulate realistic operation so system characteristics of various design and hardware arrangements can be monitored while components operate throughout a drive cycle. The focus of this project is to prepare the controls, inverter, motor, and other components for operation on the HIL system and to develop a data acquisition system to capture and record high-accuracy measurements over the extent of a drive cycle.

Approach

To prepare for operation on the full-size HIL system that is under development by the VSI team, a subscale system representative of the dynamometer system was used to carry out preliminary testing of controls and measurement developments. Fractional horsepower motors were used to facilitate rapid assembly of the system and minimize safety concerns. Nonetheless, the basic functionality of controls and measurement is the same regardless of scale. The following tasks were carried out to support and implement subscale HIL testing.

Design and fabricate circuit boards for dynamic testing

The HIL testing platform in the VSI laboratory is designed to test the entire EV (or HEV) drive system, which may include multiple converters and electric machines. Therefore, custom control and driver boards are needed to implement optimal control of these devices throughout the drive cycle. ORNL has previously developed optimized controls for individual components (e.g., motor/inverter and converter) of electric drive systems, but a new and more robust DSP and communication circuitry are needed for simultaneous operation of various components throughout challenging drive cycle profiles. Additionally, driver circuitry is required to operate the PE devices in various power conversion stages. A key part of the project is the development of these circuit boards for transient drive cycle operation.

Develop dynamic controls

ORNL has developed optimized motor controllers (for both commercial and prototype motors) for steady state operation to conduct operational efficiency mapping, determine peak performance, and analyze other operational metrics throughout the entire operation range. However, optimal operation during transient conditions for drive cycle testing presents a greater challenge, especially for erratic driving schedules.

Although detailed control algorithms will vary depending on the components used within each electric drive system, development and implementation of customizable controls for the primary motor types is a vital step in performing HIL drive cycle testing.

Develop dynamic measurement system

Many parameters and quantities need to be measured to perform full characterization of the electric drive system during HIL testing. Most of the parameters are the same as those needed during steady state performance and operational characterization. As shown in Fig. 2, many physical quantities such as dc voltage(s) and current(s), ac voltages and currents, torque, speed, and temperature need to be measured throughout the entire drive cycle. Additionally, it is preferable to stream this data to a memory storage device so that transient operation of the system can be inspected and analyzed after the tests are completed.

It is very important to synchronize the measurement of electrical power (obtained from voltage and current) and mechanical power (obtained from torque and speed). For steady state measurements, a lack of close synchronization of the measurements is less crucial because mechanical and electrical power levels are relatively constant for these conditions. However, transient power conditions require that the measurements be highly synchronized. Otherwise, both motor and inverter efficiency calculations will be erroneous, as it would be uncertain whether the transient mechanical power and electrical power were measured at the same instant.

Some electric power analyzers include the capability to measure torque and speed from a torque transducer. This capability greatly facilitates the synchronization of power measurements, as opposed to using separate instruments to obtain electrical power and mechanical power. Some power analyzers are advertised as having subsecond data refresh rates; but when appropriate time observation windows are used, the actual refresh rate is on the order of seconds. It is important to use an observation window that captures at least a few fundamental electrical cycles; otherwise, power calculations could be erroneous. For analysis of an electric drive during transient conditions, it is desirable to have subsecond refresh rates (e.g., 0.1 second). Otherwise, the value of having transient testing capabilities is diminished.

In addition to the issue of slowing refresh rates, it should be noted that these products provide only processed numerical data at these refresh rates, not actual waveform data. For example, ac rms current, ac rms voltage, and ac power can be obtained via Ethernet or serial communication at the published refresh rates; but the original waveforms are not available at the published refresh rates. Additionally, each observation window is not recorded consecutively in time; therefore, continuous waveform data are not available.

It was determined that there are no commercially available power analyzers that offer the capabilities desirable for comprehensive analysis of transient drive cycle behavior. Therefore, as a part of this project, ORNL developed a measurement system that is capable of measuring and recording data in a continuous manner.

Fabricate custom induction motors

A primary function of the HIL system is to evaluate prototype motors throughout transient drive cycle conditions. Since the IM is an alternative to RE PM motors, subscale IMs with Cu rotor bars and Al rotor bars were fabricated for comparison testing on the HIL system. Instead of using pure Cu, which has low mechanical integrity for high rotational speeds, an alumina-filled Cu termed “GlidCop” was used in rotor bar fabrication.

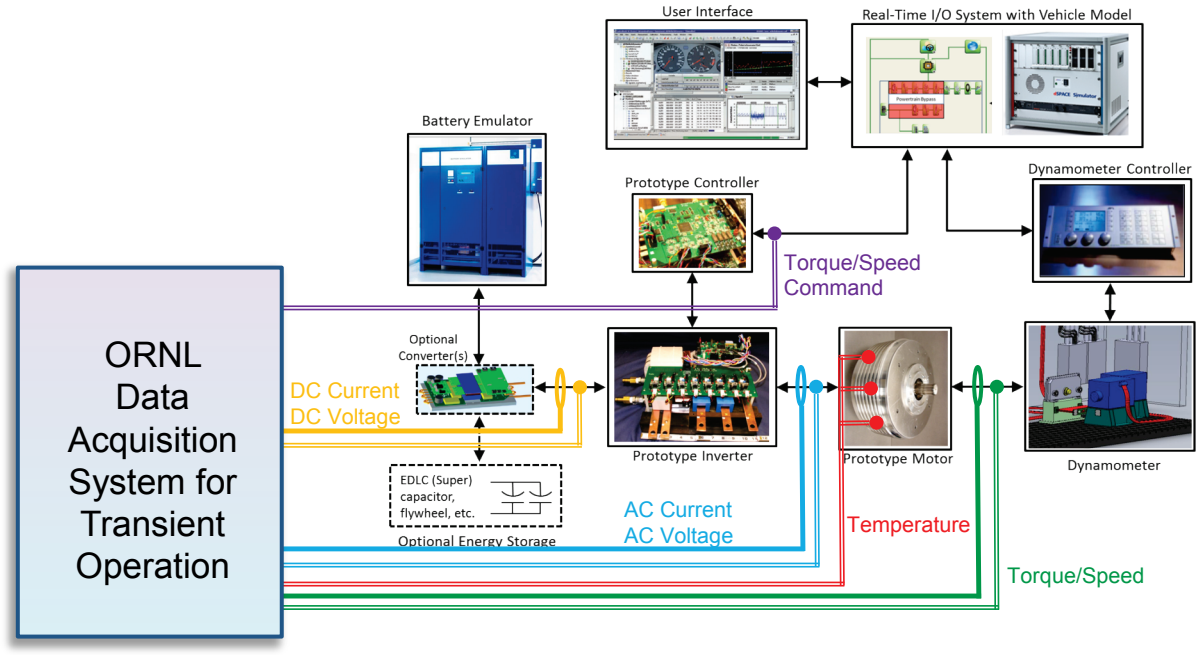


Figure 2: Measurement and data acquisition system diagram.

Perform subscale HIL testing

Subscale testing was carried out to evaluate developments for robust dynamic electric machine controls and the advanced custom measurement system. A commercially available fractional horsepower dynamometer (Fig. 3), was identified and purchased. It offers considerable flexibility for testing various machine types, and the procurement avoids excessive design and fabrication time, which is beyond the focus of this project. The subscale dynamometer kit includes a torque transducer to monitor torque between the motor under test and the loading generator.

Results

Design and fabrication of circuit boards

Previous work on control circuitry by Gui-Jia Su, Lixin Tang, and Cliff White was leveraged to develop the universal DSP board shown on the left in Fig. 4. The board has the capability to control at least two motors/inverters and two converters at once, with current and position feedback for motor operation, and voltage and current feedback for converter operation. The DSP board has the capability to communicate via various methods such as CAN, USB, and other serial communication formats. The performance of the universal DSP board and driver boards will be highlighted when subscale HIL test results are discussed.

Development of dynamic controls

Dynamic controls were developed to operate subscale motors with a dc load motor, which served as a dynamometer during subscale HIL testing. Control methods for various motor types were based on conventional control theory, but each required customization for robust operation. Controls for the IMs use observer feedback to improve the dynamic performance of the feedback control loop, which uses current and speed proportional-integral regulators. The performance of the controllers is highlighted when subscale HIL test results are discussed.

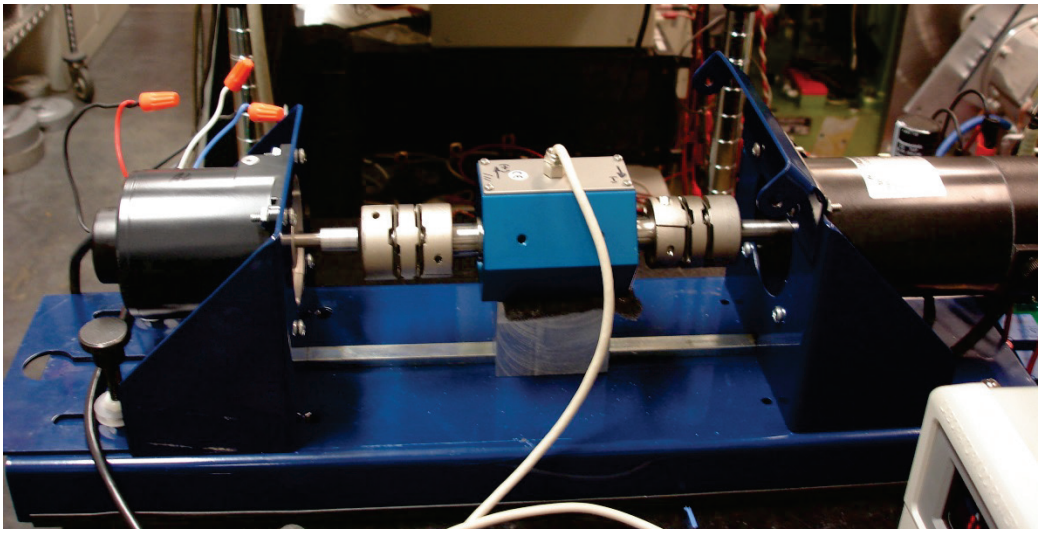


Figure 3: Fractional horsepower dynamometer assembly.

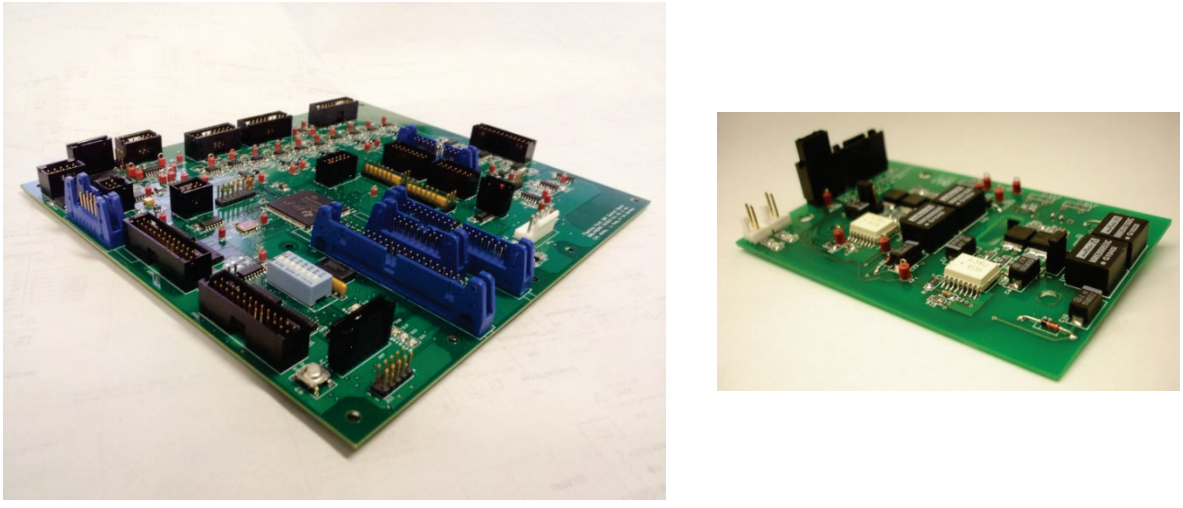


Figure 4: Universal DSP control board (left) and driver board (right).

Development of dynamic measurement system

After a survey of various platform options upon which to base the development of a measurement system, it was decided that hardware from National Instruments (NI) offered the most flexibility and customizability. The system (Fig. 5, left side) has an optional high-accuracy (14 bit), high-speed (50 MS/s) analog-to-digital accessory card that is well suited for current and PWM voltage measurement. Note that although switching frequencies on the order of kHz are used, PWM voltages have very high-frequency transients. For example, the transients associated with the switch-on and switch-off times of high-current power devices can be on the order of microseconds (1 MHz). Therefore, to appropriately monitor inverter efficiency, it is desirable to capture data at a rate that is even higher than 1 MHz.

In addition to high speed and accuracy capabilities, the NI system offers the capability to continuously stream data to a built-in hard drive. The robustness of the system allowed ORNL staff to focus on programming NI software to develop cutting-edge measurement capabilities without devoting too many resources to hardware development and data management. The graphical display (right side of Fig. 5) is an example of display options for the drive cycle data output by the custom software. Detailed results will be discussed in a later section.

Fabrication of custom induction motors

Copper and Al induction rotor bars were fabricated and assembled for comparison studies on the subscale HIL testing system. GlidCop is Cu that has ~15% alumina filler material to improve mechanical integrity without significantly reducing conductivity. These properties are attractive for IMs with high speed ratings, for which the mechanical properties of pure Cu can be a limitation. The fabricated GlidCop rotor bars and end rings, shown on the left in Fig. 6, had to be nickel plated before soldering, since the alumina makes normal bonding processes more difficult to perform. This is a primary drawback of alumina-filled Cu. Even more difficulty was encountered in the bonding of the fabricated Al pieces (shown on the right in Fig. 6). Aluminum quickly forms an oxidation layer that hinders many bonding processes and conductivity if the bond is not made properly. A collection of the IM pieces is shown in Fig. 7, where the stator, rotor shaft, bearings, empty rotor laminations, and two fabricated rotors are visible. The IM rotors are semi-closed slot with full slot skew for reduced ripple torque. A magnetic position encoder was attached to the shaft to facilitate speed feedback control.

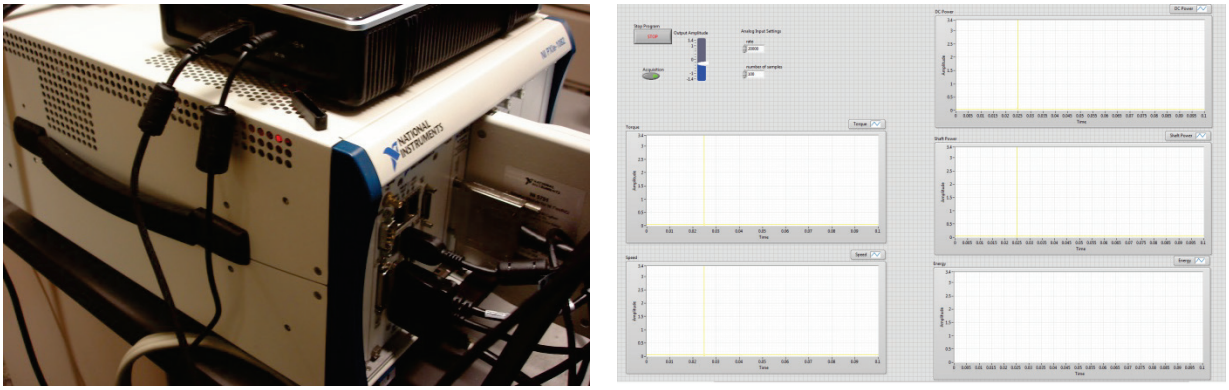


Figure 5: Measurement system (left) and display (right).

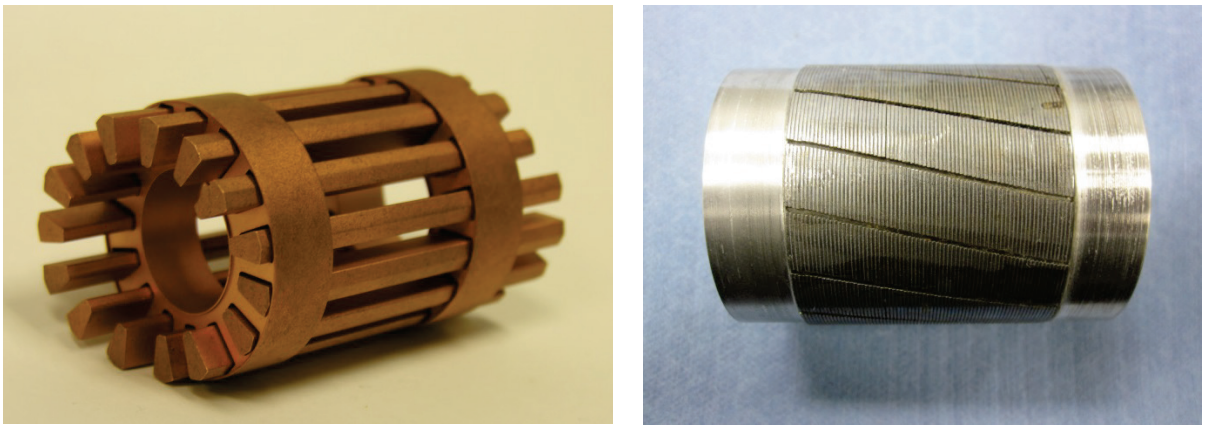


Figure 6: Fabricated GlidCop rotor bars and end rings.

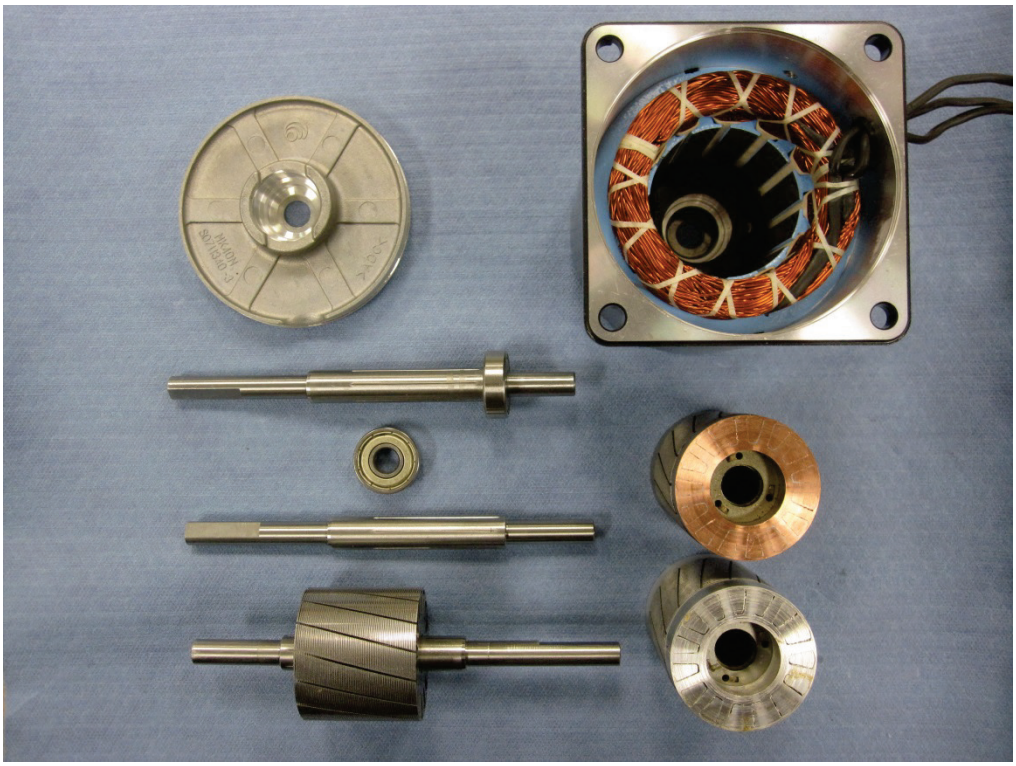


Figure 7: Scaled induction motor components (copper and aluminum rotors).

Subscale HIL test results

The scaled IMs were first tested under steady state conditions for efficiency and performance mapping. The efficiency map for the GlidCop Cu IM is shown in Fig. 8. The torque and speed axes were scaled by 560 and 2.44, respectively, to match those of Nissan LEAF motor operation. The efficiency is much lower than that of full-size electric motors, partially because of the much lower operation voltage of 42 V and because the physical air gap does not scale proportionally with power rating . It was also discovered that the Al bar motor performance was significantly lower, probably as a result of a manufacturing defect. Nonetheless, the overall FY 2013 goal of the project was not to develop, test, and compare the characteristics of these motors, but rather to develop and implement dynamic controls and an advanced measurement system.

The subscale dynamometer test system was used to emulate electric drive operation with a vehicle similar in size to a Nissan LEAF. The torque required to propel the vehicle throughout the US06 drive cycle was scaled to match the small IM performance and used as a command for the load motor, and the drive cycle speed profile (Fig. 9) was scaled and used as a speed reference for the proportion-integral loop of the small IM. The IM torque and speed operation points throughout the US06 drive cycle were scaled and superimposed on top of the steady state operational efficiency map in Fig. 10.

The superimposed torque and speed points in Fig. 10 are clear indicators that the US06 drive cycle does not require the electric drive to operate near peak torque or peak power conditions. However, it is important to note that some of the most heavily frequented areas of operation correspond with low motor efficiencies, and this is true for both subscale IM efficiencies and the full-size LEAF motor efficiencies. The scaled dc-link energy produced and regenerated by the scaled IM throughout the US06 drive cycle is shown in Fig. 11. The red trace represents the energy produced during motoring operation, and the green trace represents the energy recovered through regenerative braking. The blue trace represents the total energy, in which the regenerative energy reduces the overall required energy from the battery pack.

It is clear that the low efficiency of the scaled prototype motor yields very little benefit from regenerative braking. Simulations were conducted using the Nissan LEAF motor and inverter efficiency maps that were obtained with the Benchmarking project. The motoring, regenerative, and total energy using the LEAF components in the US06 drive cycle are shown in Fig. 12. It can be seen that the total energy at the end of the drive cycle is about 0.75 kWh versus a value of 7.6 kWh for scaled IM operation. Note that battery efficiency and transmission (gear and bearing) losses are not included in the basic vehicle model.

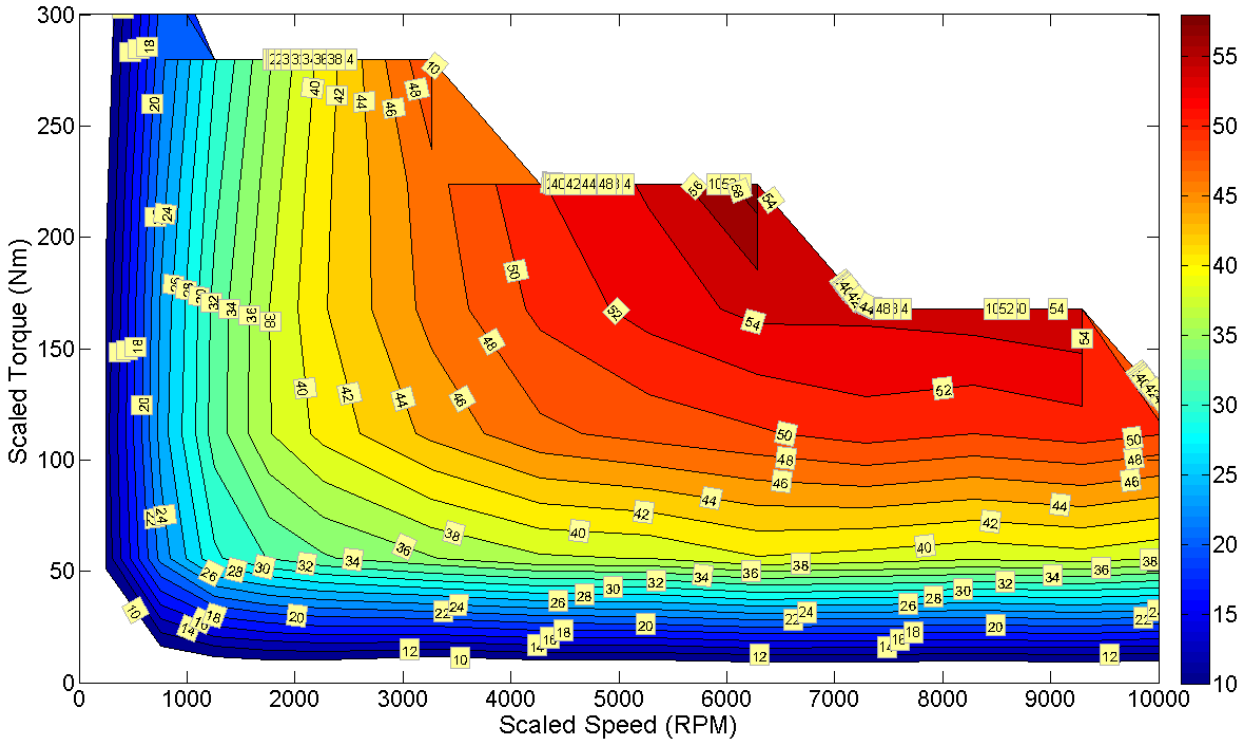


Figure 8: Scaled copper induction motor efficiency map.

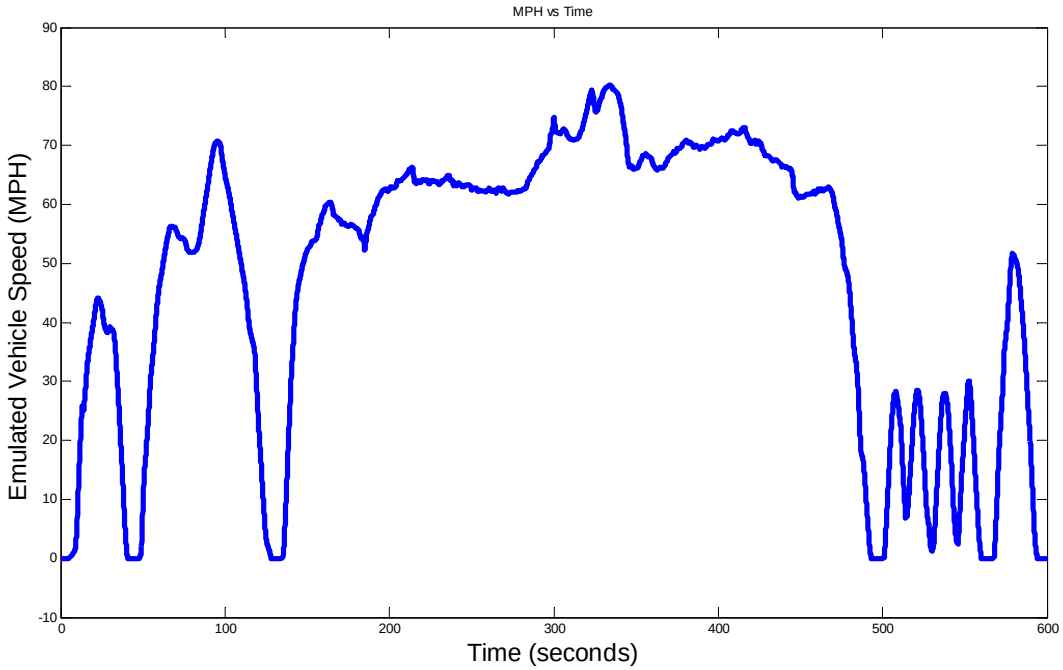


Figure 9: US06 drive cycle speed reference.

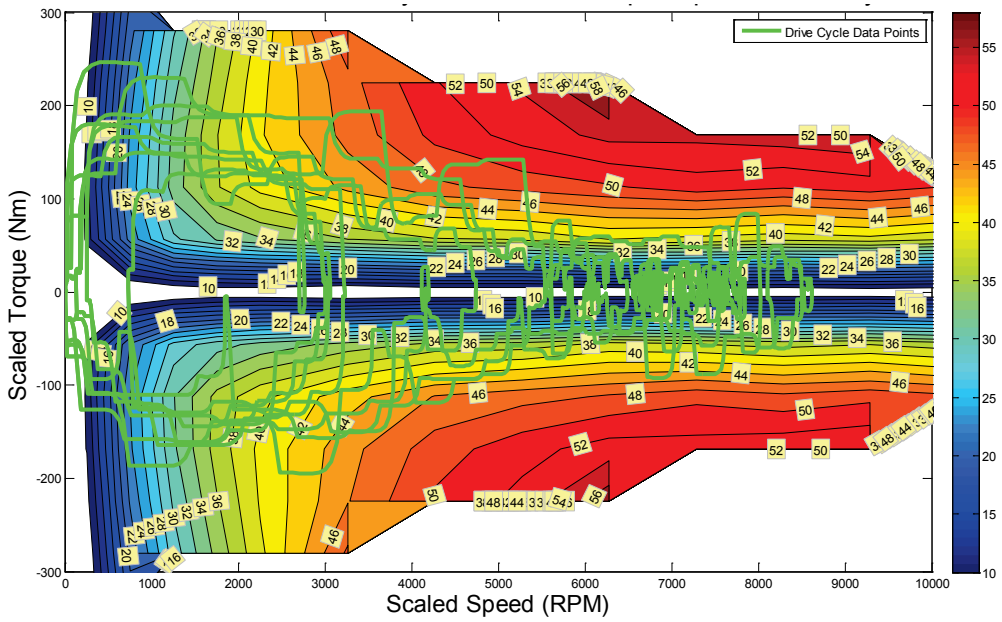


Figure 10: Overlay of US06 drive cycle operation points on scaled induction motor efficiency map.

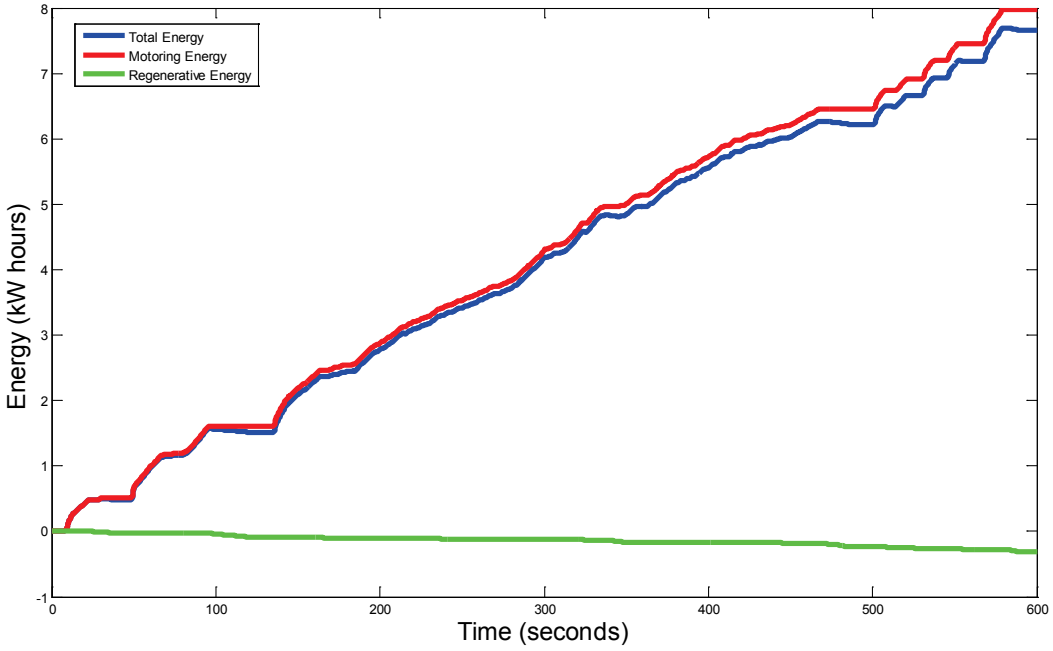


Figure 11: Scaled HIL energy produced and regenerated throughout drive cycle with induction motor.

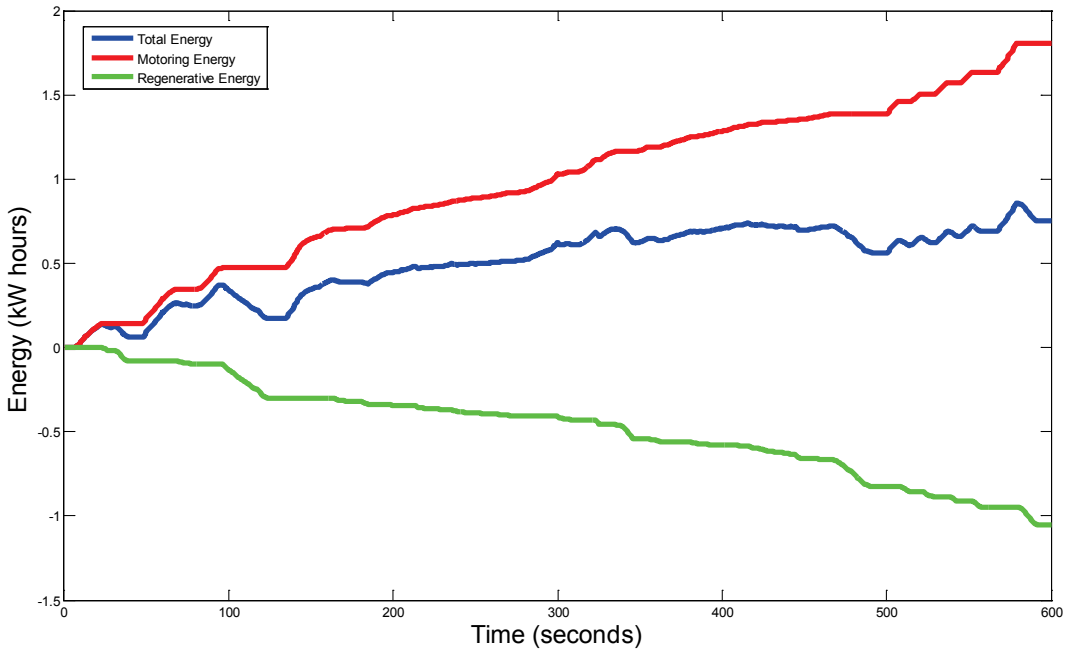


Figure 12: Simulated energy produced and regenerated throughout drive cycle with LEAF components and efficiencies.

For the vehicle to follow the drive cycle speed profile, the required torque and speed at the drive wheels is the same for both cases. However, since the efficiency characteristics of the scaled IM are inferior, much more energy is required from the battery for motoring operation for the same road conditions. Similarly, the inferior efficiencies also prevent the battery from recovering as much energy from regenerative braking. Using the total energy consumed throughout the drive cycle, the scaled IM drive system achieves only about 1.05 miles per kWh, whereas the simulated LEAF energy consumption leads to about 10.7 miles per kWh (includes aero load). According to DOE's fuel economy website, the LEAF is reported to achieve 3.4 miles per kWh during common driving conditions. In addition to transmission losses and battery efficiency, other aspects to consider are ancillary loads such as heating and air conditioning, lights, power steering, various pumps, and running lights. However, for the case of HIL comparison studies of electric drivetrain components, these considerations are not necessary.

Conclusions and Future Directions

The overall FY 2013 goal of this project was not to develop, test, and compare characteristics of prototype motors, but rather to develop and implement dynamic controls, an advanced measurement system, and various analysis methods for future operation on the full-size HIL system. The performance of the dynamic controller was robust, and it facilitated the capability of the subscale IM to follow the drive cycle speed profile, maintaining the emulated vehicle speed within 0.2 MPH of the reference. For propelling a LEAF-sized vehicle through the US06 drive cycle, the drastic difference between the scaled energy consumption curves of the subscale prototype IM and the simulated energy consumption of the Nissan LEAF drivetrain components highlights the importance of the energy efficiency of these components.

Various types of drive cycle profiles should be carried out for a true assessment of real-world drivetrain performance and characteristics. Enhancements of the custom measurement system can easily be implemented to address specific interests, such as spectrum analysis of various signals or current ripple analysis. The exemplar approach and analysis methods used to compare these technologies offers a framework for testing future prototypes and commercial components to analyze performance, efficiency, and other characteristics under realistic operation conditions. Ultimately, these results and analysis methods provide informative feedback with regard to focus areas for future R&D on converters, inverters, and electric motors.

FY 2013 Publications/Presentations

1. "System integration and HIL validation," presented at DOE Vehicle Technologies Program Advanced Power Electronics and Electric Motors R&D FY 2013 Kickoff Meeting, November 2013.
2. "System integration and validation," presented at 2013 US DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, May 2013.

3.1 Silicon to WBG Inverter Packaging

Zhenxian Liang (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1467; Fax: 865-946-1262
Email: liangz@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 2012
Projected End Date: September 2015

Objectives

- Develop advanced PE packaging technologies for comprehensive improvement in the cost-effectiveness, efficiency, reliability, and power density of automotive electric drive systems.
  - In FY 2013, develop novel packaging technologies for SiC power modules, enabling exploitation of the superior attributes of WBG materials.

Technical Barriers

State-of-the-art automotive power modules and power inverters and converters have disadvantages in electrical performance, cooling capability, thermomechanical performance, and manufacturability. These are barriers to meeting the DOE APEEM 2020 targets for cost, efficiency, and density.

Technical Targets

- Develop all-SiC power modules to replace their Si counterparts in automotive PE systems for high-power-density, high-frequency, and high-temperature operation.
- Advance packaging and manufacturing technologies for SiC power modules with lower thermal resistance, small electric parasitics, and high-temperature reliability that can be manufactured efficiently.

Accomplishments

- Developed advanced power module packaging technologies, based on a directly integrated cold-base plate concept, that feature a 33% reduction in specific thermal resistivity compared with conventional technologies.
- Fabricated a group of phase-leg power modules (50–100 A/1,200 V) with different combinations of power device (Si, SiC) and thermal packages.
- Performed comprehensive characterization and comparative system evaluation. Combining the attributes of the latest SiC power devices and advanced packaging enables an all-SiC power module with a 3× increase in current density and a 50% reduction in power losses compared with an all-Si module.

Introduction

There has been significant progress over the past decade in developing PE packaging technologies for Si devices/modules for electric drive systems in automotive applications. The focus has been on improving the systems' electrical performance, thermal management, thermomechanical reliability, and manufacturability. Advancements in power module packaging can be briefly categorized into three generations, depending on the materials and processes employed. As a baseline, first-generation packaging features solder die attachment, wire bond interconnection, and interfacial assembly. The second-generation package employs one of the following techniques: a planar bond, integrated cooling, or more reliable bonding materials. The third generation involves further integration of dual planar bond and double-sided cooling concepts, and so on. These technologies have greatly advanced the metrics for cost, reliability, functionality, power density, and efficiency of automotive PE systems. For further advancement, it is generally accepted that WBG semiconductor power devices—such as SiC and GaN MOSFETs—offer superior properties compared with their Si counterparts such as IGBTs, the power semiconductor switches mainly used in PE systems in medium- and high-power applications. A promising development in past decades is that WBG power devices, especially SiC MOSFETs and JBS diodes, have started to penetrate Si application regimes. Following the successful supply of discrete power devices, a group of all-SiC power modules have recently been developed by manufacturers such as CREE, Rohm, Infineon, and Fuji. They typically have a single-phase-leg topology, made up of SiC MOSFETs and SiC JBS diodes, and are rated at 100 A, 1,200 V.

These module packages typically employ the first-generation structure and conventional manufacturing processes. They are assembled into inverter/converter systems in which a thermal interface grease must be used between cold plate and module packages. The attributes of SiC devices, such as high-power-density, high-frequency and high-temperature operation, have not been fully explored yet.

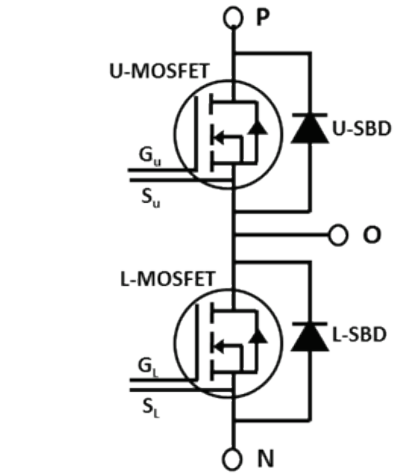
This project emphasizes the integration of an advanced direct liquid cooling concept into all-SiC power module

packaging, enabling exploitation of SiC performance. Technical details such as packaging structure and associated packaging process technology were developed. Performance improvements were characterized by experimental measurements; and efficiency, cost, and reliability benefits to a PE system were evaluated.

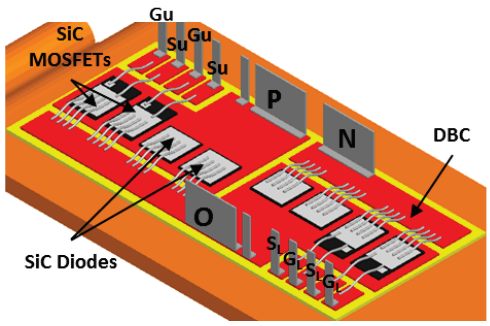
Approach

Figure 1(a) is a schematic of a one-phase-leg all-SiC power module, which is a basic building block for various automotive power converters/inverters. It is made up of two units (upper and lower) of SiC MOSFETs and SiC diodes. Power MOSFETs and diodes are commercially available in the form of bare dies, both rated at 50 A/1,200 V. The current rating of the power module can be increased by paralleling multiple dies. Figure 1(b) shows a layout of the die placement and interconnection pattern for a 100 A/1,200 V phase-leg power module. The power switch unit consists of two SiC MOSFETs and two SiC diode dies in parallel. The electrical interconnection is achieved by bonding AL wires to the tops of the dies and soldering the dies on Cu traces of a DBC substrate; electrical insulation is provided by the Al oxide (Al_2O_3) ceramic slice inside. The parasitic electric resistances of the current flow paths cause ohmic power loss and affect the efficiency and junction temperatures of power switches. The packaging interconnection parasitic inductances will cause voltage overshoot on SiC switches, limiting their switching speed and increasing their switching losses. The layout of multiple SiC dies on a DBC substrate, and their interconnections, has been optimized to reduce these parasitic electrical parameters using electromagnetic simulation tools.

In the first-generation packaging structure of the SiC modules shown in Fig. 2(a), the power stage—including SiC dies, interconnections, and substrate—is directly bonded onto a Cu base plate by solder and then encapsulated. All the power and signal I/O terminals/pins are located on the top surfaces of the modules. For thermal management, the module must be mounted mechanically onto a cold plate, which provides coolant flow paths and keeps the SiC die temperature below a safety threshold. In this assembly, a necessary thermal interface material, such as a thermal grease, severely degrades the cooling efficiency. This study proposes a new cooling structure. As schematically illustrated in Fig. 2(b), the SiC power stage is directly soldered to a cold-base plate. This specialized part replaces the base plate, thermal grease, and cold plate in the conventional packaging structure (Fig. 2(a)). The integration not only improves the cooling efficiency but also reduces the volume and weight of the SiC power module assembly, as well as the manufacturing steps.

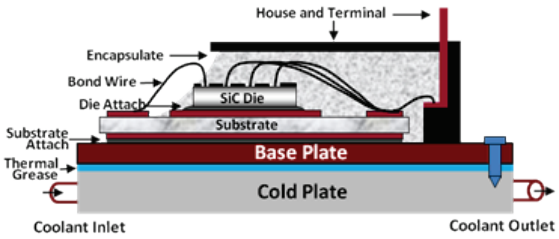


(a)

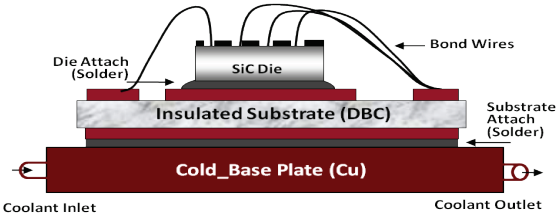


(b)

Figure 1: Electrical design of an all-SiC module: (a) electrical diagram (U-upper unit, L=lower unit) and (b) multiple SiC die layout and interconnection configuration.



(a)

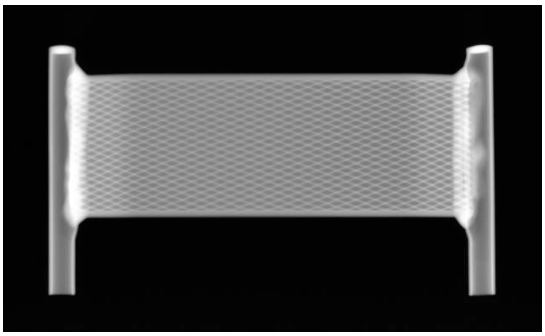


(b)

Figure 2: Schematics of SiC power module packaging structures and materials: (a) conventional interfacial thermal assembly and (b) direct cooling by integrated cold-base plate package.

Figure 3(a) shows a photo of a cold-base plate like the one employed in this study. It measures 105 mm (L) by 58 mm (W), including coolant inlet and outlet. Its main body is made of a flat Cu tube with an outline thickness of 3 mm. The effective cooling surface measures 60 mm (L) by 30 mm (W). It contains internal fins to increase cooling efficiency, and they offer excellent thermal uniformity as coolant flows below the entire surface. The x-ray image shown in Fig. 3(b) exposes the unique internal crisscross fin structure for control of coolant flow. The Cu offers excellent solderability that makes it possible for the power stage (on the DBC) to be directly bonded by solder.

(a)



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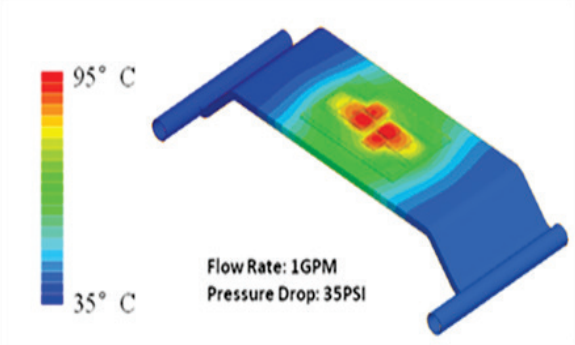


(c)

Figure 3: Cold-base plate and thermal performance: (a) photo of the integrated cold-base plate; (b) x-ray image of the plate; and (c) temperature distribution of the power module on the integrated cold-base plate.

The thermal performance of this package was investigated via a computational fluid dynamics (CFD) simulation using the computational tool COMSOL. Figure 3(c) shows the calculated temperature distribution of the whole module under these conditions: each die has a power loss of 12.5 W; inlet coolant temperature is 25°C, flow rate is 1 gpm (308 lpm), and pressure drop is 35 PSI (241 kPa). The effective thermal resistance of an SiC die related to the whole module assembly, including power stage and cold plate, is 0.7K/W, significantly smaller than the resistance in a conventional module assembly with typical thermal grease and a standard Al cold plate.

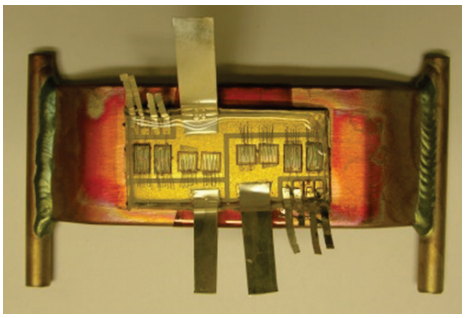
To manufacture complete power module prototypes, a set of package parts was designed and fabricated using in-house packaging capabilities. They include die attachment solder and the top interconnection wire bond, DBC power substrate, power and signal terminals, baseplate, encapsulate, and so on.

For comparison purposes, the conventional interfacial cooling structures also were manufactured. The conventional cold plate is a solid Cu plate with thermal conductivity [k=400 W/(mK)] and mechanical strength. Its dimensions are 75 mm (L) × 32 mm (W) × 3 mm (H).

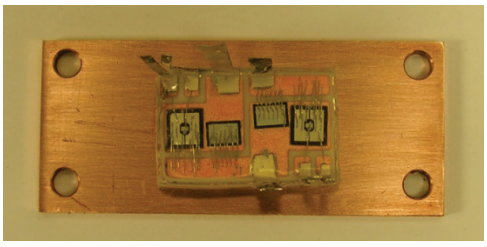
To examine the advantages of this SiC power module applied in an electric drive system, an Si IGBT/ PiN diode phase-leg power module with the same current/voltage rating (50 A/1,200 V) was fabricated. The packaging components in the Si modules are identical to those in the SiC modules except for the power semiconductor dies.

Results

Several SiC and Si power modules were packaged, including samples for special thermal electrical tests. Figure 4 presents two examples: an all-SiC 100 A/1,200 V phase-leg module with integrated cold-base plate (a) and an all-Si 50 A/1,200 V module with conventional base plate (b).



(a)



(b)

Figure 4: Photos of representative power modules: (a) all-SiC 100 A/1,200 V module with integrated cold-base plate and (b) all-Si 50 A/1,200 V module with conventional base plate.

The electrical parameters of the modules were characterized using various experimental methods. The static I-V curves were measured at different junction temperatures. Figure 5 shows the test

results for a 50 A/1,200 V SiC MOSFET in the module. Through these tests, the conduction losses of semiconductor devices and packaging parasitic electric resistances were also obtained.

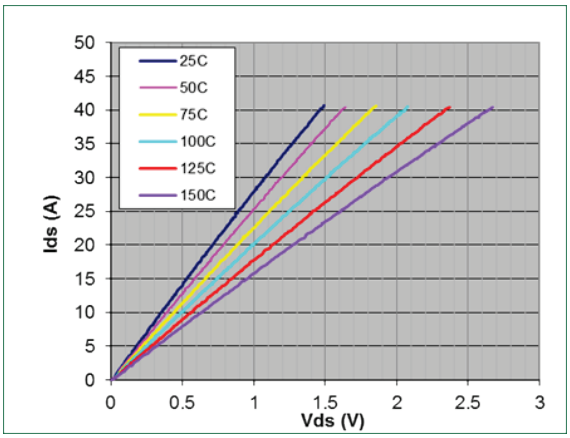


Figure 5: Static I-V characteristics of 50 A/1,200 V SiC MOSFET.

Figure 6 shows the typical electrical waveforms of an SiC MOSFET during turn-off transition at a bus voltage of 600 V and current of around 50 A. The fastest switching speed (less than 100 nS) of SiC devices was experimentally identified with a specially designed in-house gate drive circuitry. The package parasitic inductances were measured by switching power devices in a specific testing circuit.

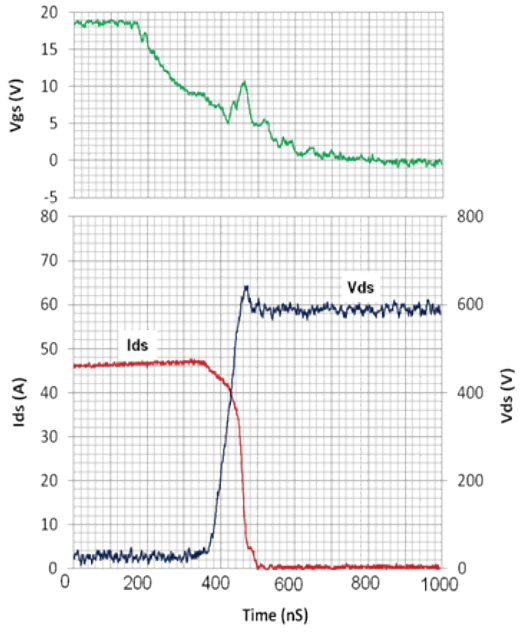


Figure 6: Switching waveforms of 50 A, 1,200 V SiC MOSFET during turn-off transition.

The switching power losses, including turn-on and turn-off parts, can be calculated from this test at different voltages and currents, temperatures, and so on. Figure 7 presents the switching power loss of the SiC MOSFET versus current under different operating temperatures (up to 175°C).

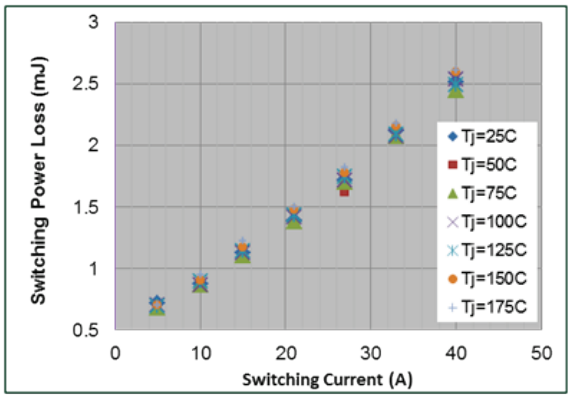


Figure 7: Switching power loss of 50 A/1,200 V SiC MOSFET vs. current at a different temperature (up to 175°C).

The thermal parameters of the module package were characterized with an established thermal test setup in which the body diode of a SiC MOSFET was used to self-heat. Its forward voltage drop was also used as the temperature sense parameter to measure the junction temperature. The calibration curve of this body diode voltage, *Vf*, versus temperature at *Ifc* =1 mA was firstly acquired. The *Vf* changes linearly with temperature with a temperature coefficient of –2.45 mV/°C. When a larger current *Ifp* and voltage *Vfp* are applied to the body diode of the SiC MOSFET for 10 min, the device temperature is increased to a certain level. The corresponding input power equals the product of *Ifp* and *Vfp*. Then the input power is quickly turned off, and the current going through the diode is switched to *Ifc*. A *Vf* variation curve over time can be recorded. After the conversion of *Vf* to the device junction temperature based on the calibration data, a cooling temperature curve (over time) can be obtained. With input electrical power and temperature change, the thermal impedance of the module package can be calculated.

Figure 8 summarizes the thermal resistance data for both conventional and integrated cooling module assemblies. The specific thermal resistivity is used as an indicator of the thermal performance of the module assembly, which includes the thermal resistivity of all packaging components and the cold plate. The specific thermal resistivity is a normalized thermal resistance to its die area, which represents the thermal performance of a package. It can be seen that the specific thermal resistivity of the integrated cooling packaging is more than 33% lower than that of a conventional package.

In a comparative study, the electrical and thermal performance of Si power modules was also characterized, using the same methodology used for the SiC modules, and the performance of the modules was compared one to one.

Figure 9(a) presents a comparison of static I-V characteristics of an IGBT in the Si module and a MOSFET in the SiC module. Their switching losses (sum of turn-on and turn-off parts) are shown in Fig. 9(b). It can be clearly seen that the SiC MOSFET exhibits less conduction power loss and less switching power loss than the Si IGBT.

As power devices operate in an inverter or converter, the total conduction loss depends on the current, voltage drop, and

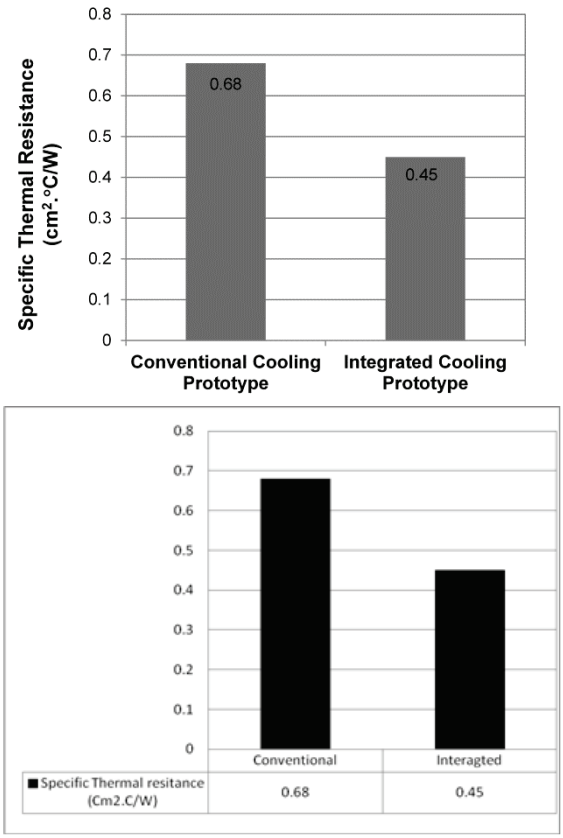


Figure 8: Comparison of specific thermal resistivity between conventional module assembly and integrated cooling packaging.

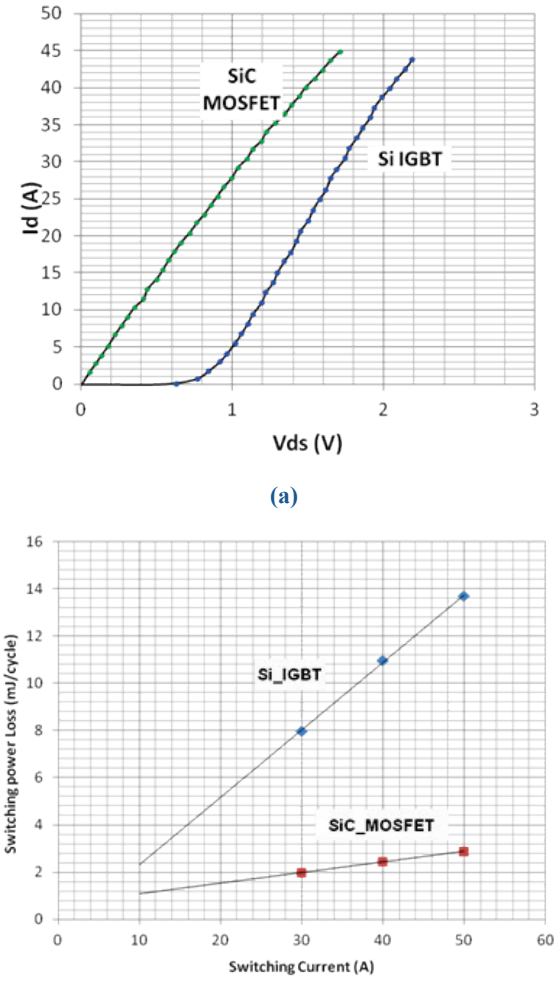


Figure 9: Comparison between 50 A, 1,200 V SiC MOSFET and Si IGBT switch (at room temperature): (a) static I-V characteristics and (b) switching loss vs. current (at bus voltage of 600 V).

duty cycle (*D*); the switching loss is related to current magnitude (*Id*), blocking voltage, switching speed, and switching frequency (*f*). As discussed earlier, the electrical power losses in power devices will generate self-heating and cause the device temperature to rise. For thermal management, the power density or heat flux in the die is more directly related to the cooling efficiency, because the thermal dissipation capability depends greatly on the die area (size).

By combining the specific thermal resistivity with different cooling configurations, the temperature rise of a power device can be calculated. Figure 10 shows the junction temperature increase from the ambient level (here, the inlet temperature of the coolant) versus current for four different device/package combinations. They are an Si IGBT in a conventional cooling configuration, an Si IGBT on an integrated cold-base plate, an SiC MOSFET on a conventional cold plate, and an SiC MOSFET in an integrated cooling package. The cooling configuration is shown to greatly affect the junction temperatures of power devices. With a fixed current, for example 30 A, the increase in the junction temperature ranges from ~50 to 90°C between the best and the worst combinations. Device temperature is directly related to module reliability and lifetime: higher temperatures lead to a significant reduction of the power module lifetime.

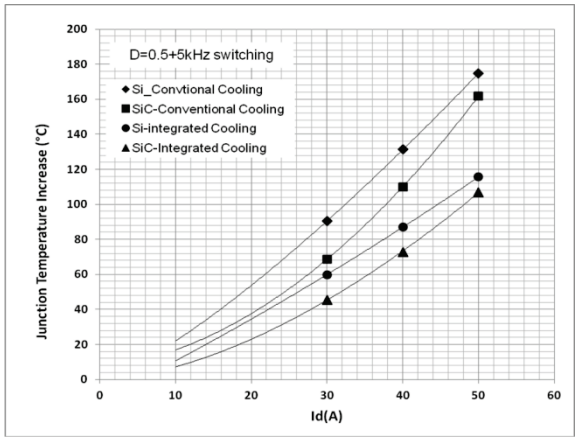


Figure 10: Comparison of device junction temperature increase vs. current between different power semiconductor and cooling combinations for a typical operation: D=0.5, f=5 kHz.

On the other hand, if the maximum operational boundary is set based on the package reliability and the semiconductor temperature limits, the maximum handling current density of a power switch can be determined accordingly. For instance, as shown in Table 1, the allowed current density of a power device for four combinations increases from 66 A/cm^2 to 185 A/cm^2 for a 100°C temperature increase, which can be a case for a coolant temperature of 25°C and a junction temperature of 125°C. These maximum current density values define the minimum die size of the power semiconductors for a designed system current (or power) level. It is well known that die size is a dominant factor in power module cost. The 3× die size reduction from the worst combination to the best one is significant for reducing the PE system cost. Furthermore, the data demonstrate that the power semiconductor device type plays an important role in these improvements. For example, the die size can be reduced 1.9 to 2.2 times as a result of changing from an Si IGBT to an SiC MOSFET because of the lower power loss density of the latter. The die size can be reduced 1.3 to 1.5 times by using an integrated cooling package instead of a conventional packaging cooling configuration.

Table 1: Current density allowed for different power semiconductor and cooling combinations at ΔTj=100°C for a typical opertion (D=0.5, *f*=5kHz)

Item	Si_ conventional cooling	SiC_ conventional cooling	Si_ integrated cooling	SiC_ integrated cooling
Current density J_d (A/cm^2)	65.35	144.97	97.57	184.98

The analysis and data discussed are closely related to a defined operation condition (here, D=0.5, f=5 kHz). The contributions of the packaging technology and the power semiconductor technology to the improvements in power module efficiency, cost, and reliability can be further analyzed using these performance parameters for any specific application cases.

Conclusions and Future Directions

All-SiC phase-leg power modules fabricated in-house at the ORNL Packaging Laboratory feature the adoption of the latest industrial SiC power devices—MOSFETs and JBS diodes—and second-generation packaging with integrated direct cooling structure. Combining the attributes of SiC and advanced packaging, these modules offer superior performance over Si counterparts.

The module's performance improvements, leading to high-efficiency, high-density system operation beyond the limits of Si, resulted in improvements in system cost, efficiency, and reliability.

Further advancement of WBG automotive PE depends greatly on improvement of power packaging technology through advances in structure, materials, and processing techniques to fully exploit the attributes of WBG power devices: high power density, high frequency, and high-temperature operation. Future development of advanced WBG power modules will include the following:

- Integrate direct double-sided cooling.
- Realize low-parasitic electrical parameters.
- Enable a high-temperature, highly reliable package.
- Provide highly intelligent functionality.
- Allow extensive integration of the converter/inverter system.

These advancements will enable considerable strides in achieving DOE power density and cost targets for PE systems in electric drive vehicles.

FY 2013 Publications/Presentations

Publications

1. Z. Liang, P. Ning, F. Wang, "Development of advanced all-SiC power module packaging," *IEEE Transactions on Power Electronics*, special issue on WBG devices, 2013 (in press).
2. Z. Liang, P. Ning, F. Wang, "Advanced packaging of SiC power module for automotive applications," *Proceedings of the Fifth IEEE Energy Conversion Congress and Exposition*, Denver, September 15–19, 2013.
3. Z. Xu, M. Li, F. Wang, Z. Liang, "Investigation of Si IGBT operation at 200°C for traction applications," *IEEE Transactions on Power Electronics* **28**(5), 2604–2615, May 2013.
4. P. Ning, Z. Liang, F. Wang, L. Marlino "Double-sided cooling design for novel planar module," *Proceedings of the IEEE Applied Power Electronics and Exposition*, Long Beach, Calif., March 17–21, 2013.

Presentations

1. Z. Liang, "Development of automotive power module packaging," SAE Electronic Systems for Vehicle Propulsion/Intelligent Vehicle Systems Symposium, Troy, Mich., September 18, 2013.
2. Z. Liang, P. Ning, F. Wang, "Advanced packaging of SiC power module for automotive applications," IEEE Energy Conversion Congress and Exposition 2013, Denver, September 18, 2013.
3. Z. Liang, "WBG power device packaging," DOE Annual Merit Review, Washington, D.C., May 14, 2013.
4. Z. Liang, "Cross-industry reliability: Automotive power module perspective," 2013 PV System Symposium, Santa Clara, Calif., April 30, 2013.
5. P. Ning, Z. Liang, F. Wang, and L. Marlino "Double-sided cooling design for novel planar module," IEEE Applied Power Electronics Conference 2013, Long Beach, Calif., March 17–21, 2013.

FY 2013 Patents

1. Z. Liang, L. Marlino, P. Ning, F. Wang, "Power Module Packaging with Double Sided Planar Interconnection and Heat Exchangers," US Patent application publication, US 2013/0020694 A1, January 24, 2013.

3.2 WBG Gate Driver and Smart Power Module

Leon Tolbert (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1332; Fax: 865-946-1262
Email: tolbertlm@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 2012
Projected End Date: September 2015

Objectives

- Develop a highly integrated power module phase leg (rated at 1,200 V and 200 A), incorporating WBG devices, that includes (1) an integrated gate drive, (2) an isolation chip, and (3) a power supply, in a package that allows it to work at high temperatures (up to 150°C ambient) and device junction temperatures of up to 200°C.
- Build a smart gate drive with protection features, high current capability, and active gate control to minimize switching loss and chance of noise-induced gate turn-on that can lead to shoot-through.
- As a final goal, produce 55 kW inverter phase-leg modules that can work at high temperatures and meet 2020 targets of 14 kW/l and 14 kW/kg, and 2015 targets of $5/kW, and 98 % efficiency.

Technical Barriers

PE modules lack the integration necessary to achieve future DOE 2020 VTO cost targets. PE converter components are discrete, bulky, and temperature-limited. Gate drives and packaging for new WBG devices are limited in their ability.

Technical Targets

- Construct an integrated gate-drive solution that can operate at the ambient temperatures seen in an engine compartment.
- Design and fabricate on-chip input isolation prototypes. Determine functionality, blocking voltage, and transient immunity of chip prototypes.
- Develop an isolated power supply on chip (PwrSoC) to power the module.
- Explore a fast, reliable, low-loss, cost-effective overcurrent protection scheme for SiC MOSFETs.
- Develop an active current balancing (ACB) scheme to eliminate the current unbalance of parallel-connected SiC MOSFETs.
- Eliminate cross talk for WBG power devices in a phase-leg configuration, leading to lower switching losses, fast switching speed, and high reliability.
- Integrate a high-temperature gate driver integrated circuit (IC) into an SiC-based phase-leg power module for functionality verification.

Accomplishments

- Developed and experimentally verified a highly integrated gate drive that operates successfully at 200°C.
- Fabricated and verified the functionality of an isolation chip. Demonstrated an input PWM signal frequency of 5 MHz.
- Designed and verified a common mode rejection test printed circuit board (PCB). The design allows for testing in excess of 30 kV/μs.
- Completed the layout of the isolation chip.
- Fabricated a power supply in package, consisting of a boost converter and on-chip inductor for characterization.
- Designed an isolated PwrSoC schematic. Preliminary simulation results are encouraging. A plan for isolated feedback control to regulate the power supply has been established.
- Fabricated the hardware prototype of the SiC MOSFETs with three overcurrent protection methods (solid state circuit breaker [SSCB], desaturation technique, and fault current evaluation).
- Extensively evaluated the performance of the protection schemes under various conditions, considering variation of fault type, decoupling capacitance, and protection circuit parameters.
- Proposed protection schemes capable of clearing a short-circuit fault within 200 ns, irrespective of the junction temperature variation of SiC MOSFETs.
- Based on the testing results, compared each method to explore the benefits and drawbacks of each one and its potential applications.
- Verified the ACB scheme by simulation and experiment, demonstrating the elimination of current unbalance for two parallel SiC MOSFETs.

- Developed an active gate driver to eliminate cross talk for a phase leg using WBG devices, and integrated the logic signal synthesis of the proposed gate auxiliary circuit with the latest version of a high-temperature gate driver IC.
- Developed a board-level integrated power module and conducted the preliminary test for functionality verification.

Introduction

The EV and HEV have brought significant challenges for PE modules, both for the power devices and for their packaging technologies. One critical design task is to develop highly integrated power modules to reduce the total weight and volume of the power distribution systems.

Input isolation

The control circuitry of the power module requires an isolation barrier for the interface between the logic-level control signal and voltage level of the gate driver that operates the high side of a power phase leg. The isolation solution for the power module must meet the same high-temperature requirements as the power module. The isolation capability must block the rms high voltage across the phase legs and reject the dV/dt transient noise in the power module. The physical layout area of the isolation design should be minimized to reduce the overall size of the power module.

Power supply on chip

To reduce the size of the integrated power module as well as assist in high-temperature operation, an isolated PwrSoC is under development. The power supply receives a dc voltage (9–18 V) from a standard car battery and outputs a +20 V potential and a –2 V potential providing power to the module. The power supply should be operable up to 200°C and be able to supply 250 mA of current.

Overcurrent protection schemes for SiC power MOSFETs

Overcurrent protection of SiC MOSFETs remains a challenge because of a lack of extensive use and testing. Compared with overcurrent protection of Si devices and SiC JFETs, overcurrent protection of SiC MOSFETs is more challenging in the following aspects.

From a thermal point of view, SiC MOSFETs tend to have lower short circuit withstand capability than Si IGBTs and MOSFETs because of their smaller chip area and higher current density.

Besides thermal breakdown, an overcurrent condition also has a negative impact on the long-term stability of SiC MOSFETs, which have traditionally suffered gate oxide reliability issues induced by poor interface quality.

Even when fast fault response time becomes the design focus of the protection scheme for SiC MOSFETs, the objective is quite challenging in a fast-switching environment.

There are no known publications discussing the overcurrent protection of SiC MOSFETs since they have become commercially available. The objective of this research is to help designers select a proper protection method based on the analysis and performance evaluation of different protection schemes.

Active current balancing for parallel-connected SiC MOSFETs

In high-power applications such as HEVs or utility converters, parallel connection of SiC MOSFETs is required, because SiC devices usually have smaller dies than do Si devices as a result of lower yield in this less mature manufacturing process. Current unbalance among the parallel devices can occur when the individual devices or the external circuits are not exactly identical or symmetrical. Unbalanced current can lead to uneven distributed power loss and temperature rise, localized overcurrent, and even the failure of the entire module. To account for that, the current rating of the power module is usually less than the sum of all the devices' ratings, and the current capability of the devices is not fully utilized. This work proposes a novel ACB scheme. The scheme is able to sense the unbalanced current in the devices and continuously adjust the gate delay to eliminate this unbalance. It achieves high speed and arbitrarily fine time resolution that matches the fast switching speed of SiC devices; therefore, it has low circuit complexity and cost.

Cross talk mitigation

SiC devices have an inherent capability for fast switching. However, in the phase-leg configuration, the interaction between two devices during a switching transient (cross talk) might increase switching losses, reduce the reliability of the power device and, eventually, limit the switching speed of SiC devices. Considering the intrinsic characteristics of high-voltage SiC power devices—such as low threshold gate voltage, low maximum allowable negative gate voltage, and large internal gate resistance—cross talk is a serious issue, and a suitable solution for cross talk suppression is essential.

Approach

High-temperature gate driver

A revised multi-chip solution was developed in FY 2013. The functionality of the previous gate driver solution was split across three dies. The decision to split the functionality into several components was driven by our colleagues in the Ampere Lab in Lyon, France. They had purchased an engineering run and provided an area on their reticle. The conditions were that each die would be roughly 3 by 3 mm, which is drastically smaller than in previous efforts; the previous most recent gate drive chip was 9 by 5 mm. The new generation of the gate drive comprises a voltage regulator die, signal management die, and output buffer die. To facilitate a full phase-leg design, the voltage regulator die has two sets of regulators, a 5 V regulator for the low-voltage logic and a 6.4 V charge pump regulator. The charge pump regulator on the past generation had performance issues at high temperatures, but the regulator on this effort was revised to improve its performance over temperature. The signal management die also has two signal paths so that a phase leg may be driven. The buffer die can be set up so as to double the output current (~10 A) or to drive two power switches.

The entire multi-die solution allows a lot of flexibility for end users in setting up their signal chains. For testing and to mitigate parasitics, the bare die was bonded onto a high-temperature PCB. The experimental validation of the revised gate drive will begin in FY 2014. The test procedure will involve lifetime reliability testing, because part of the revision was to improve the reliability through the addition of redundant metal traces and substrate tie-downs. The substrate tie-downs should provide a low-resistance path for heat to flow off the chip, and the redundant metal traces should improve electromigration immunity.

Input isolation

The input isolation design has been focused on an on-chip-transformer–based input isolation design. The on-chip transformers designed in the chip prototypes are around 200 µm in diameter. This is multiple orders of magnitude smaller than off-chip isolation transformers. The main drawback of the on-chip transformer is the limited dc blocking voltage. The transformer uses stacked coils on a chip metal interconnect to create the primary and secondary windings. There is limited insulating oxide between the two coils. The Si-on-insulator chip prototype 1 uses a three-metal interconnect technology. The maximum oxide insulating thickness of prototype 1 is roughly 0.9 µm. The reported SiO_2 field strength is greater than 700 V/µm. Prototype 2 uses a six-metal interconnect technology. The estimated dc blocking for prototypes 1 and 2 is estimated at 630 and 2440 V, respectively. Although prototype 2 has a much higher dc blocking voltage, the chip technology is not capable of high-temperature operation. Therefore, both prototypes will be tested and the limitations of each will be experimentally discovered.

The on-chip design is implemented in 5 V complementary metal-oxide semiconductor (CMOS) technologies. The design block diagram is shown in Fig. 1. The transformer size is small because of the use of GHz-level voltage pulses passed through the transformer. The transmitter controls the di/dt through the primary transformer winding to create a voltage pulse. The receiver then detects the voltage pulses and recreates the input logic signal.

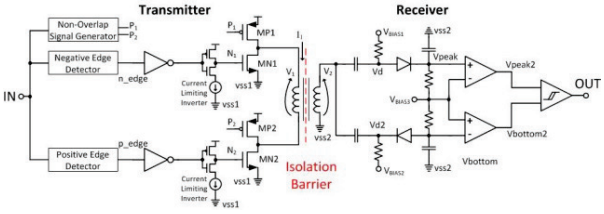


Figure 1: On-chip design block diagram.

Power supply on chip

To provide the +20 V potential, an active clamp boost converter topology was chosen for its low number of components as well as its wide input range capability. An active clamp flyback converter was adopted to provide the −2 V potential for the same previously mentioned reasons. Figure 2 shows the schematic of the power supply. A major difficulty in designing a PwrSoC, let alone an isolated one, is implementing on-chip inductors (or transformers). All inductors have some series resistance that must be minimized for efficient operation of a dc-dc switched mode power supply. This is a challenge because to reduce the series resistance, the size of the inductor must increase. Since size reduction is a design constraint, a tradeoff must be reached that allows implementation of an efficient PwrSoC. The transformers depicted in Fig. 2 are made up of stacked 12 and 23.5 nH inductors with 820 mΩ and 4.5 Ω of series resistance, respectively. The outer diameter of the transformer is 2000 µm. A feedback control scheme is required to regulate the +20 V and −2 V outputs. Since the converter is isolated, the feedback must also be isolated. To accomplish this, a PWM scheme was implemented on the secondary side of each converter. The PWM signal is then transmitted to the primary side, where a controller processes the signal and is used to drive the MOSFET switches of the converter.

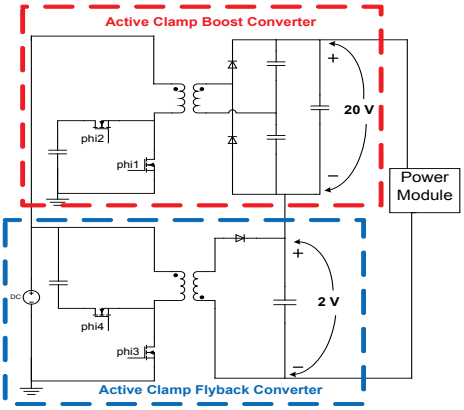


Figure 2: Schematic of isolated power supply on chip (the feedback control circuitry is not shown).

Overcurrent protection schemes for SiC power MOSFETs

First, the short-circuit capabilities of commercial SiC MOSFETs were determined. Based on this, several candidates, including conventional protection techniques and newly proposed methods, were implemented and evaluated through Saber simulation with real component models. Finally, a step-down converter-based hardware test setup was built to verify and compare these methods through extensive measurements.

Active current balancing for parallel-connected SiC MOSFETs

In high-power applications of SiC MOSFETs where parallelism is employed, current unbalance can occur and affect the performance and reliability of power devices. A novel ACB scheme was proposed. This scheme includes three basic building blocks, as shown in Fig. 3: (1) The current unbalance sensing block senses the unbalanced current in the devices. (2) The current balancing controller generates the correction needed based on the measured unbalance. (3) Then, the active gate control varies the gate drive signal delay according to the instruction from the balancing algorithm. The three blocks form a negative feedback loop.

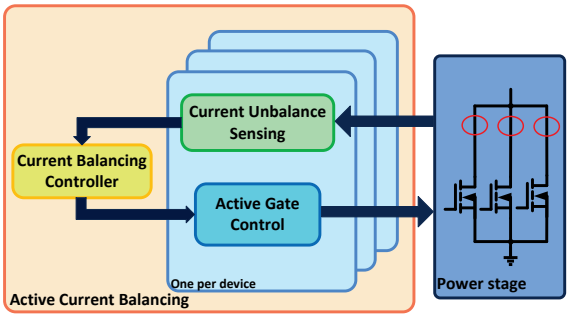


Figure 3: Block diagram of the proposed ACB.

The proposed current unbalance sensing technique measures the difference instead of the actual value in the two parallel devices, using a differential current transformer (DCT). The schematic is shown in Fig. 4. It has two 1-turn primary windings in opposite directions. If current unbalance exists and the currents in the two windings are unequal, there will be net flux change, and current in the secondary will generate output voltage, *V out*, the polarity of which indicates the polarity of unbalance. The proposed DCT has negligible impact on the system efficiency and component stresses because the 1-turn primary winding has very low resistance and leakage inductance.

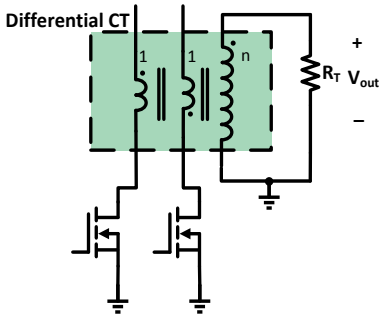


Figure 4: Schematic of the proposed DCT.

A novel variable gate delay (VGD) circuit is proposed as the core of the active gate control block. The schematic is shown in Fig. 5. During a turn-on transient, M1 is in saturation and its drain current is controlled by its Vgs. Therefore, *Vcontrol* controls the charging current of the power switch gate and thus its turn-on delay. The proposed VGD circuit achieves continuous tuning of gate delay with arbitrarily fine time resolution.

The proposed current balancing controller (CBC) is implemented based on an integrator circuit, as shown in Fig. 6. The output of the DCT is integrated with a gain of 1/sR1C1. The output of the integrator is connected as *Vcontrol* of the VGD. In conjunction with the DCT and VGD, the CBC closes the negative feedback loop and adjusts the gate signal delay so that the output of the DCT is zero; thus the current unbalance is eliminated.

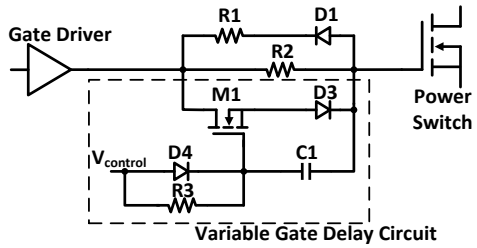


Figure 5: The proposed variable gate delay circuit.

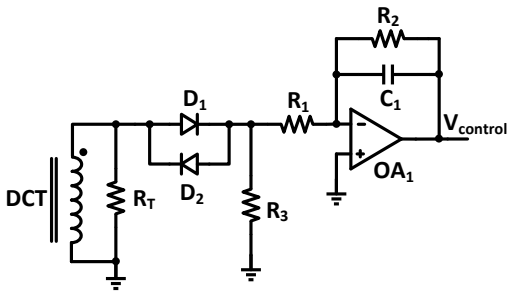


Figure 6: Simplified schematic of the proposed current balancing controller.

Cross talk mitigation

A gate impedance regulation (GIR) –based active gate driver circuit was developed for cross talk mitigation (it is illustrated in the FY 2012 progress report). To fully avoid cross talk for fast-switching SiC power devices in a phase-leg configuration, a gate voltage control (GVC) –based active gate methodology was proposed, as shown in Fig. 7. Compared with the conventional gate drive circuit (S_{1_H}, S_{2_H} or S_{1_L}, S_{2_L}), two auxiliary transistors (S_{a1_H} and S_{a2_H} or S_{a1_L} and S_{a2_L}) together with one diode (D_{a_H} or D_{a_L}) are added between the gate-source terminals of each device, whereas the commonly used negative isolated power supply is not needed. Figure 8 displays the active gate driver board with the proposed gate auxiliary circuit.

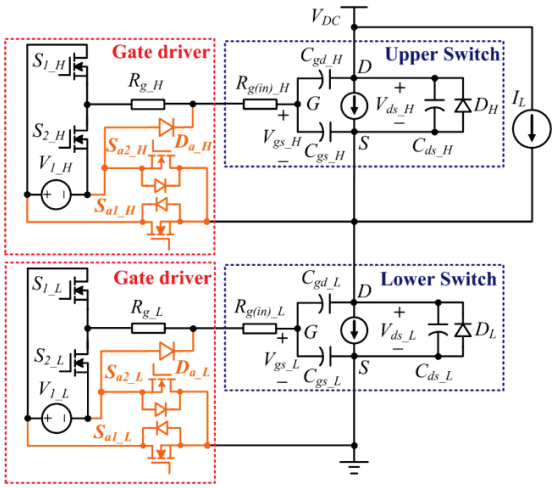


Figure 7: Active gate driver with GVC assist circuit.

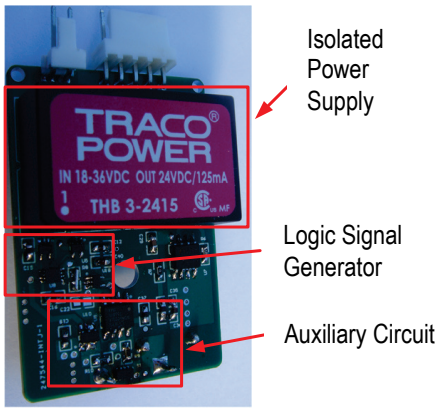


Figure 8: Active gate driver board.

Board-level integrated power module

Based on a phase-leg power module built with CPM2-1200-0025B SiC MOSFETs and CPW5-1200-Z050B SiC Schottky diode bare dies from CREE (Fig. 9), a board-level integrated power module was developed. It can be seen from Fig. 10 that the smart power module integrates the gate driver auxiliary power supply board, gate driver board, and phase-leg power module in a sandwich structure. Based on chip-on-board techniques, the high-temperature gate driver IC developed by the University of Tennessee is bonded with the gate driver board to switch the power devices.

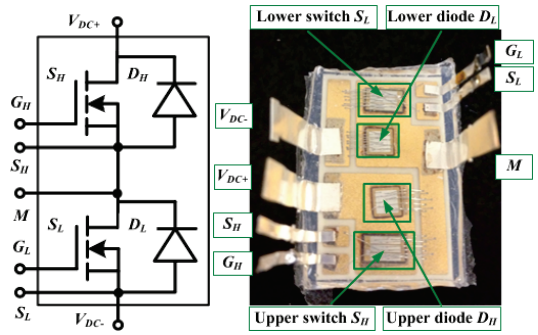


Figure 9: 1,200 V SiC-based phase-leg power module.

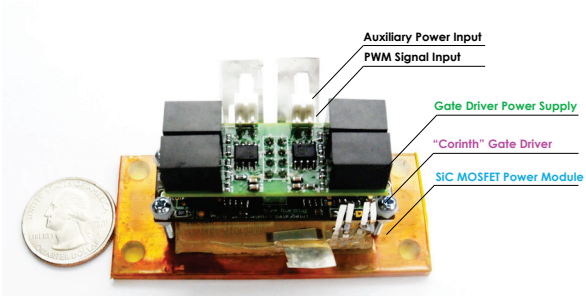


Figure 10: Board-level integrated power module.

Results

Input isolation

A circuit to test the common mode rejection (CMR) of the input isolation chips was designed. The circuit injects a high-voltage transient to the ground potential of either the transmitter or the receiver of the isolation design. The injected voltage is around 25 kV/µs. This dV/dt can be adjusted by changing a resistor-capacitor network and by adjusting the dc link voltage. The dV/dt ranges from 2 kV/µs to greater than 30 kV/µs. Typical CMR ratings of isolators are around 5 to 50 kV/µs. The discrete components used in the test circuit are rated for 600 V. The setup uses two transmitter/receiver isolation pairs. The first transmitter/receiver pair isolates the PWM signal up to the high-voltage domain, and the second pair isolates the PWM down to the low-voltage domain for measurement. A dynamic CMR test is defined by an injected common-mode voltage while the input and output are switching. A failed test is defined as a false switching of the output signal of the receiver circuit.

A polyimide PCB is used to test the input isolation chips and CMR scheme. Each isolation chip contains both the transmitter and receiver of the isolation design. However, each chip will use only the transmitter or the receiver. The design is a two-chip solution. On the polyimide PCB, four chips are bonded directly to the PCB substrate. The four chips make up two transmitter/receiver pairs.

Test results are shown in Figs. 11 and 12. Figure 11 shows the basic functionality of the isolation chips. The frequency of the input logic signal is 1 MHz, well beyond the needed frequency of the power module. The output signal matches the input with a propagation delay of 69 ns. Figure 12 shows a CMR test. The input signal switches to high, causing the output signal to switch immediately afterward. A common-mode voltage of 6 kV/µs is injected to the ground potential of the high-voltage domain. The output signal is not disturbed by the common-mode voltage pulse.

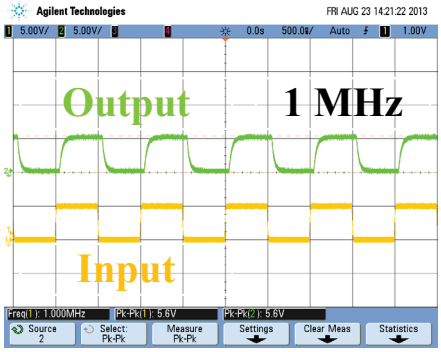


Figure 11: Functionality test waveform, f = 1 MHz.

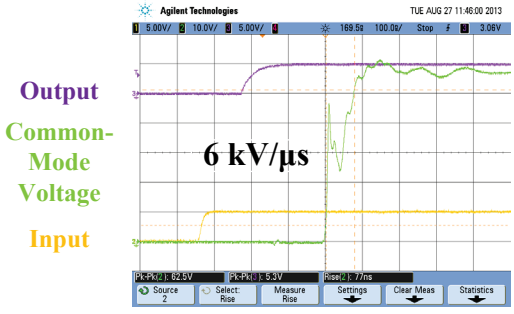


Figure 12: Dynamic common-mode voltage test.

Power supply on chip

Preliminary schematic simulation results for the power supply without any regulating feedback control are shown in Fig. 13. In Fig. 13, the two potentials in reference to the secondary side ground can be observed. These simulations support Fig. 2 as a viable power supply system.

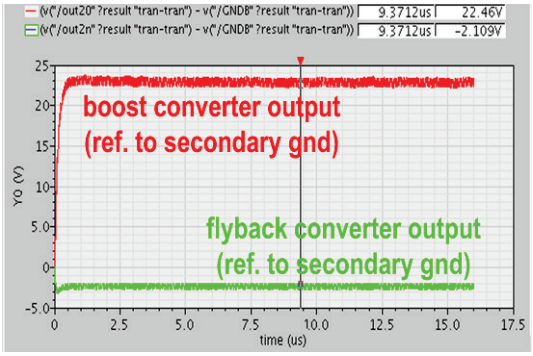


Figure 13: Preliminary simulation results for the outputs of the boost converter and flyback converter in reference to the secondary side ground.

Overcurrent protection schemes for SiC power MOSFETs

Two conventional candidates were implemented: (1) an SSCB and (2) a desaturation technique. A third protection scheme, based on the fault current evaluation, is also proposed to protect SiC MOSFETs under a short-circuit condition. These were implemented with a special focus on the design optimization, and comparisons of their performance were provided. The fabricated hardware test bed is shown in Fig. 14.

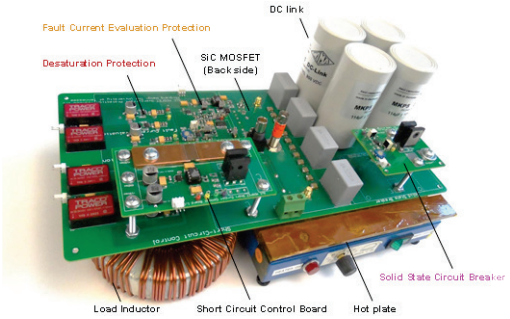


Figure 14: Hardware testbed of the protection schemes.

1. Solid-state circuit breaker

Figure 15 describes an SiC MOSFET–based step-down converter with a normally-on SSCB taking advantage of the well-known desaturation protection schemes of IGBTs. The SSCB could be inserted either in series with the energy storage capacitors (position A), or in series with the main power loop (position B). Inserting it into the main power loop can reliably detect and clear overcurrent faults, while considerable power dissipation is a concern. At position A, the loss associated with the SSCB is small, since only ripple current goes through the SSCB in series with the dc link energy storage capacitors. However, SiC MOSFETs could still be destroyed by the short-circuit loop from the dc source V_{dc} or the front-end rectifier to the device.

Figures 16 and 17 show the testing results under hard switching fault (HSF) and fault under load (FUL) condition. In both fault types, the fault response time is well below 200 ns, and the fault peak current is below 60 A.

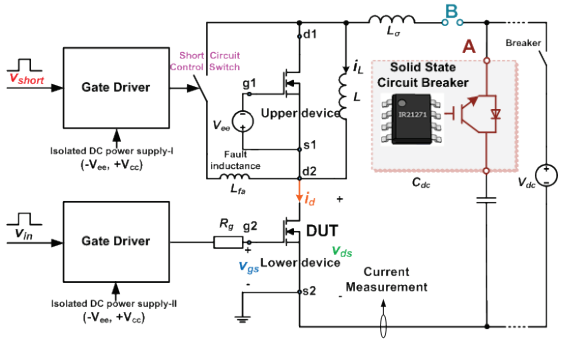


Figure 15: Step-down converter with an SSCB.

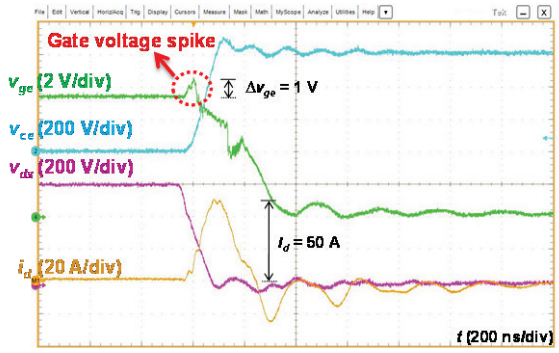


Figure 16: Protection under hard switching fault condition.

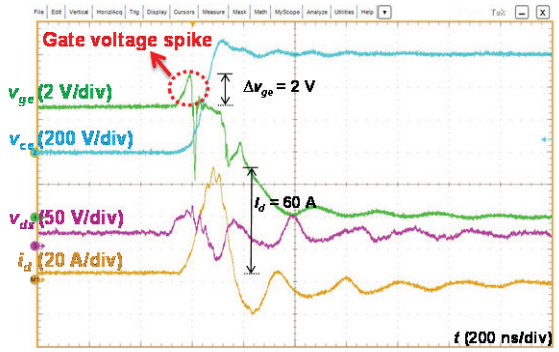


Figure 17: Protection under fault-under-load condition.

2. Desaturation technique

The desaturation protection circuit implemented in this work is shown in Fig. 18. The drain-source voltage of the device under test is monitored by the sensing diode D_{ss}, and the R-C network (R_{sat1}, R_{sat2} and C_{blk}). When the device is "on" and saturated, D_{ss} will pull down the voltage across C_{blk}. When the device pulls out of saturation under overcurrent condition, the buffer output will charge C_{blk} up and trip the comparator.

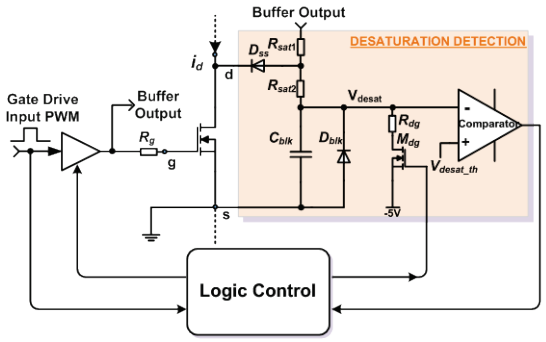


Figure 18: Implementation of desaturation technique.

Figure 19 shows experimental waveforms with a desaturation protection scheme under an HSF condition. The blanking time is set at 100 ns. The HSF fault current is limited to 130 A within 210 ns.

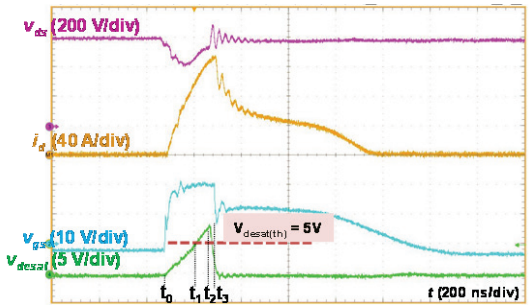


Figure 19: Protection waveforms under hard switching fault.

3. Fault current evaluation

A novel overcurrent protection scheme is also proposed to realize fast response time and strong noise immunity simultaneously; the circuit implementation is shown in Fig. 20. There are four main function blocks: fault current evaluation, logic control, gate voltage clamping, and soft turn-off.

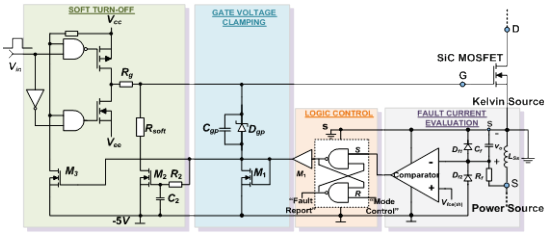


Figure 20: Fault current evaluation protection scheme.

Fault current evaluation is used to dynamically estimate the fault current by an resistor-capacitor filter during a short-circuit transient. The logic controller could activate/deactivate the protection circuit according to the input fault current evaluation results. Once the protection circuit is activated, the gate voltage clamping could limit the transient short-circuit current, and the device would be softly turned off to suppress the voltage overshoot during a turn-off transient.

Figures 21 and 22 show experimental waveforms with the fault current evaluation protection scheme under HSF and FUL conditions. With R_f = 200 Ω, C_f = 1 nF and $V_{fce(th)}$ = –3 V, the current protection threshold is around 100 A. The HSF fault current is limited to 130 A within 140 ns; then it is clamped to around 50 A, with a corresponding clamped gate voltage of 12 V. Following a delay of 400 ns, the device is softly turned off. Similar protection characteristics are also shown under FUL, while its fault peak current (120 A) is a little higher owing to longer protection delay.

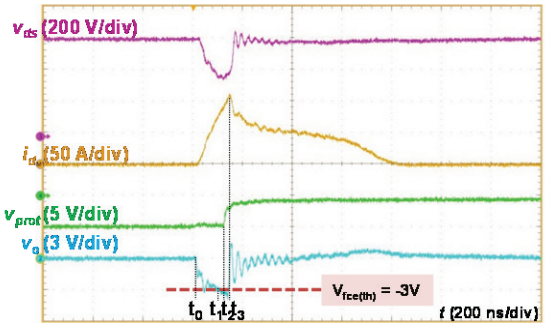


Figure 21: Protection waveforms under hard switching fault.

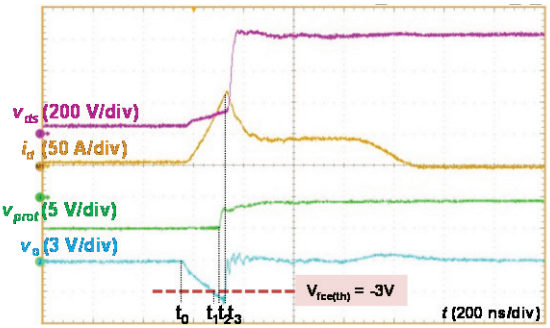


Figure 22: Protection waveforms under fault under load.

Active current balancing for parallel-connected SiC MOSFETs

The ACB system is implemented with the DCT, VGD, and CBC described earlier and verified in a buck converter with two parallel SiC MOSFETs, model CMF20120D. The simplified schematic is shown in Fig. 23. The Vth of M1 is 1.0 V lower than that of M2. The variable delay is applied to M1 while a reference voltage is applied to the M2 VGD so that the relative delay between the two devices can be both positive and negative. Figure 24 shows the experimental results. The current unbalance during turn-on transition is greatly reduced by the ACB scheme. Since the ACB scheme directly measures the unbalanced current and reduces it by negative feedback, it can reduce any current unbalance, regardless of the cause.

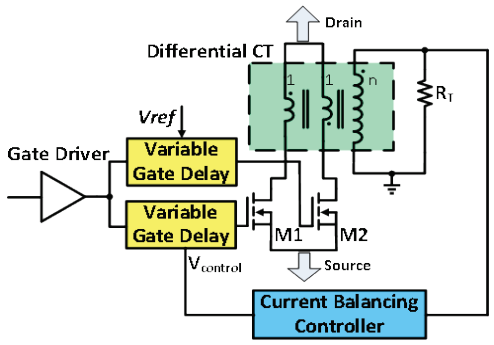


Figure 23: Simplified schematic of the proposed ACB system.

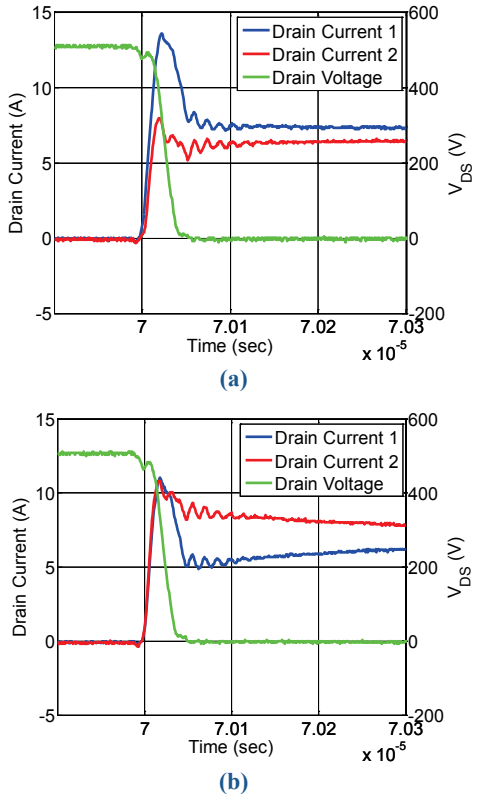


Figure 24: The switching waveforms (a) with and (b) without the ACB scheme enabled.

Cross talk mitigation

To evaluate the effectiveness of the GVC-based active gate driver for cross talk suppression, comparison experiments were conducted, using a double-pulse tester with CMF20120D SiC MOSFETs, on three different groups: a conventional gate driver, a GIR-based gate driver, and the latest GVC-based gate driver, as shown in Table 1. Figure 25 displays the comparison waveforms under three different groups with the operating condition of 800 V/10 A with 10 Ω gate resistance and load current, I_L, of 10 A . It shows that compared with the GIR-based gate driver, the GVC-based gate driver is more effective at suppressing cross talk: the turn-on energy losses during the turn-on transient of the lower switch are reduced by up to 19% instead of 17%. The slew rate of the drain-source voltage is further improved from 24 to 25 V/ns.

More experimental data under different operating conditions provided in Fig. 26 indicate that compared with the GIR-based gate driver, the GVC-based gate driver can effectively eliminate cross talk and enhance switching performance. Note that to clearly demonstrate the effectiveness of the proposed active gate driver, the experimental data for the second and third groups shown in Fig. 26 are normalized based on data for the first group (Table 2). In summary, the GVC-based gate driver is a more effective solution for cross talk suppression. Also, considering the all-transistor-based auxiliary circuit, the auxiliary components of the GVC-based gate driver are suitable for gate driver chip-level integration.

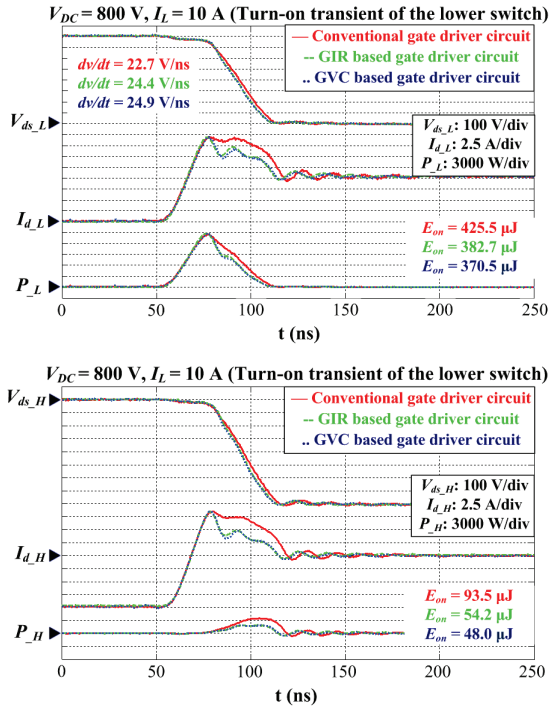


Figure 25: Lower and upper switch waveforms during turn-on transient of lower switch.

Table 1: Three comparison groups

1st Group	Conventional gate driver
2nd Group	GIR-based gate driver
3rd Group	GVC-based gate driver

Table 2: Eon and dv/dt vs. I_L under the first group with Vdc of 800 V and Rg of 10 Ω

I_L (A)	5	10	20
E_{ON} (µJ)	381.3	519.0	852.6
dv/dt (V/ns)	23.5	22.7	21.1

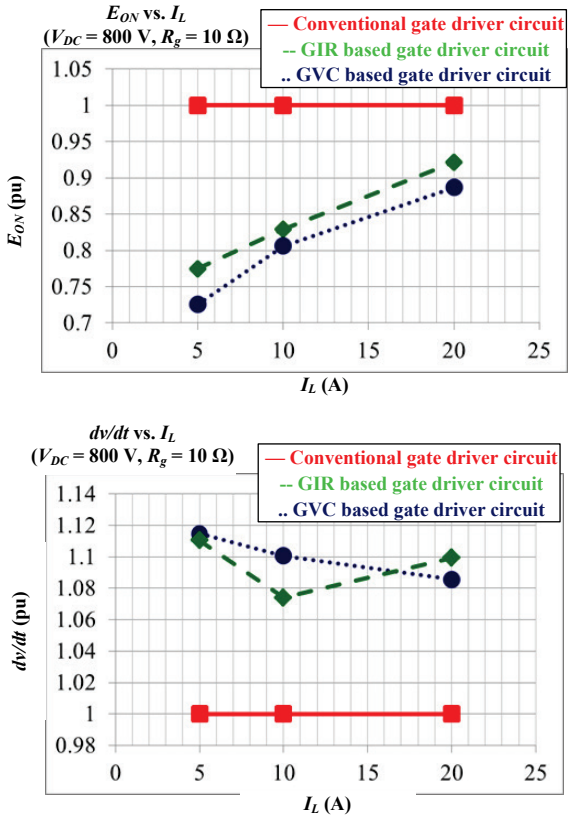


Figure 26: The GVC-based gate driver is more effective for reducing turn-on energy loss and improving dv/dt under different operating conditions.

Board-level integrated power module

Preliminary testing was carried out to evaluate the switching characterization of the SiC-based phase-leg power module. Figure 27 displays the drain-current and drain-source voltage of both the upper and lower switches during the switching transient of the lower switch under operating conditions of 800 V/30 A with 5 Ω gate resistance. It shows that with the same gate resistance, the ringing during the turn-on transient is more serious than that during the turn-off transient. In addition, the overshoot voltage of the upper switch during the turn-on transient (902 V) is higher than that of the lower switch during the turn-off transient (642 V). Also, because of the cross talk and its induced shoot-through current, the switching loss of the upper switch (240 µJ) becomes comparable to that of the lower switch (370 µJ) during the switching transient of the lower switch.

More experimental data taken under different operating conditions (Fig. 28) indicate that the cross talk–induced energy losses make up a large portion of the total switching losses. Therefore, it is essential to apply the latest version of the University of Tennessee–developed gate driver IC integrated with the anti-cross talk circuitry for the next version of the 1,200 V SiC-based phase-leg power module.

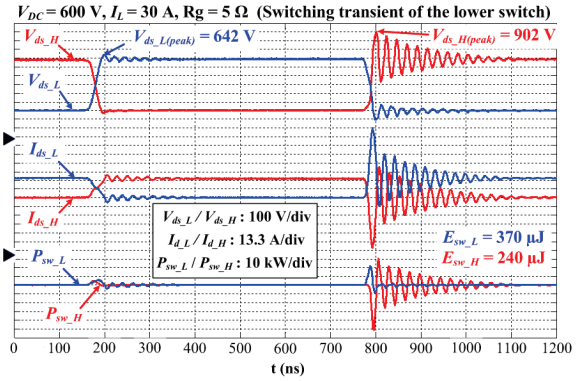


Figure 27: Typical switching waveforms of power module.

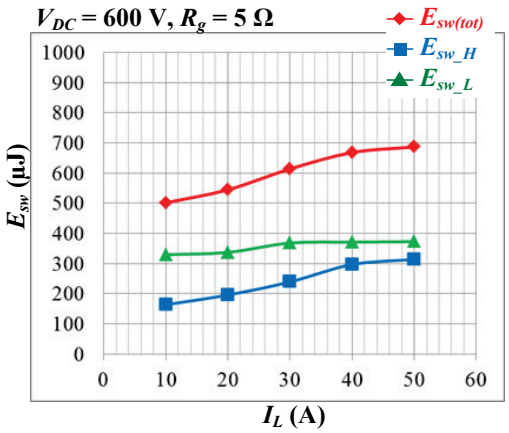


Figure 28: Switching loss dependence on I_L.

Conclusions and Future Directions

Input isolation

A high level of integration is desired for the input isolation and other components of the project. An on-chip solution for input isolation is the current focus for integration with the power module. Two chip prototypes have been designed. The first prototype has been fabricated and tested. The chips have performed well and operate above 1 MHz signal transmission. The CMR of the isolation chips has been demonstrated at 6 kV/µs. The second chip prototype is designed to improve the CMR and rms isolation voltage. This design will be fabricated in October and arrive for testing in early 2014.

Power supply on chip

An isolated PwrSoC schematic has been developed, and a feedback control scheme for regulating the output voltages has been established. Currently, the transmitter and receiver for the PWM feedback signal are being designed. In the near future, the power supply schematic will be combined with feedback control and the completed system will be fine-tuned. Future effort will be spent on shrinking the size of the on-chip transformer and improving the efficiency of the dc-dc converters.

Overcurrent protection schemes for SiC Power MOSFETs

Three overcurrent protection methods have been presented for SiC MOSFETs under both HSF and FUL conditions. The design considerations and associated issues of these methods were analyzed and verified through experiments. A qualitative comparison of these techniques was made for fault response time, temperature-dependent performance, and their potential applications to help the designer select an appropriate protection scheme. The experimental results based on a step-down converter indicate that the proposed protection schemes have the capability to clear a short-circuit fault within 200 ns, irrespective of the junction temperature variation of SiC MOSFETs. The integration of the protection method into a gate driver chip will be investigated.

Active current balancing for parallel-connected SiC MOSFETs

An ACB scheme was proposed. Experimental results show that the proposed DCT is able to accurately measure the unbalance current despite its small size. And the novel, simple VGD circuit is able to continuously adjust the gate delay with arbitrarily fine resolution for fast-switching SiC MOSFETs. The proposed ACB system can automatically adjust the gate signal and remove current unbalance. Based on this work, ACB for multiple SiC devices in parallel will be investigated in the future.

Cross talk mitigation

A GVC-based gate assist circuit using two auxiliary transistors together with a diode is proposed for cross talk suppression in a phase-leg configuration. The test results with CMF20120D SiC MOSFETs verify that without the negative turn-off gate voltage, this gate assist circuit has the capability to fully suppress cross talk under different operating conditions. It also improves switching performance compared with the conventional gate drive, even with –2 V turn-off gate voltage: turn-on transient becomes fast; turn-on switching loss can be reduced by up to 19.4%; and spurious negative gate voltage is always suppressed within its required range. Accordingly, this all-transistor–based gate assist circuit offers a simple, efficient, cost-effective solution for cross talk elimination. Also, it is a promising option for gate driver chip-level integration.

Board-level integrated power module

A board-level integrated power module has been developed, including a high-temperature SiC MOSFET power module, an Si-on-insulator gate driver, and a gate driver power supply. The preliminary switching performance of the power module was characterized through double-pulse tests. Experimental results show the fast switching speed of the integrated power module, as well as associated ringing issues.

The high-voltage and high-temperature input signal isolation will be added to the gate driver and integrated with the power module. A ceramic substrate–based high-temperature gate driver will be fabricated to replace the polyimide PCB board, with the aim of further increasing the power density and high-temperature capability of the integrated power module.

FY 2013 Publications/Presentations

1. Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, B. J. Blalock, F. Wang, “Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs,” *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 15–19, 2013, Denver, Colorado, 2013.
2. Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, F. Wang, “Active current balancing for parallel-connected silicon carbide MOSFETs,” *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 15–19, 2013, Denver, Colorado, 2013.
3. Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, “A novel gate assist circuit for cross talk mitigation of SiC power devices in a phase-leg configuration,” in *Proceedings of IEEE APEC*, pp. 1259–1265, March 2013.
4. Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, “A gate assist circuit for cross talk suppression of SiC devices in a phase-leg configuration,” in *Proceedings of the IEEE Energy Conversion Congress and Exposition*, Sept. 15–19, 2013, Denver, Colorado, 2013.
5. Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, “Active gate driver for cross talk suppression of SiC devices in a phase-leg configuration,” accepted for publication in *IEEE Trans. Power Electronics*.
6. Z. Wang, X. Shi, L. M. Tolbert, F. Wang, B. J. Blalock, “A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules,” accepted for publication in *IEEE Trans. Power Electronic*.

3.3 WBG dc-dc and On-Board Charger

Gui-Jia Su (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1330; Fax: 865-946-1262
Email: sugj@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 2013
Projected End Date: September 2016

Objectives

- Overall project objective
  - Develop low-cost, high-efficiency, high-power-density all-WBG dc-dc converters and OBCs. The aim is to reduce charger converter cost by 50% and weight and volume by a factor of 2 compared with the state of the art and provide charger efficiency of more than 96%.
- FY 2013 objective
  - Research architecture candidates for a dc-dc converter and charger best suited for functional integration and target power throughput levels of 2.2 kW for a 14 V dc-dc converter and 6.6 kW OBC. The efficiency of both functions should be greater than 95% at 75% of the rated power.

Technical Barriers

- Reducing OBC and dc-dc converter cost, weight, and volume
- Achieving high efficiency
- Overcoming the limitations of existing semiconductor and magnetic materials to address charger and converter cost, weight, volume and efficiency targets

Accomplishments

- Completed a modeling, analysis, and simulation study for several isolation converter architectures and down-selected one for prototype development.
- Developed a control strategy for the isolation converter to reduce the battery ripple current of twice the ac main frequency that is inherent in single-phase ac-dc converters. Simulation results show the control strategy enables a 60% reduction in the ripple current and thereby a significant size reduction in the bulky dc link capacitor in the front ac-dc converter.
- Completed a DBC substrate design for WBG switch phase-leg modules for Cree SiC MOSFETs and Schottky diodes.
  - DBC cards based on the design were fabricated.
  - Several SiC MOSFET phase-leg modules using the DBC cards were assembled.
- Conducted testing and evaluation of Efficient Power Conversion (EPC) low-voltage (<200 V) enhancement mode GaN (eGaN) switches for possible use in the 14 V dc-dc converter.
- Conducted testing and evaluation of International Rectifier (IR) 600 V GaN switches packaged by Delphi for use in high-voltage converters.
- Completed a design for a 6.6 kW isolation converter using ORNL-designed SiC phase-leg modules and planar ferrite cores.
- Completed tests of a baseline 5 kW Si-based integrated charger, using the selected isolation converter candidate, that demonstrated an isolation converter peak efficiency of 98% and a charger system (ac line to dc output) peak efficiency of 93% at 65% rated load.

✧ ✧ ✧ ✧ ✧

Introduction

The stand-alone OBCs and 14 V dc-dc converters that currently dominate plug-in EVs and AEVs are not cost-effective and have performance limitations that stem from limitations in existing semiconductor and magnetic materials. The result is a plateau in charger and converter performance because (1) Si switches constrain switching frequencies to typically 100 kHz, and (2) inductors and transformers based on soft ferrite magnetic materials further limit power density and efficiency because of low saturation flux densities (~0.38 T) and high core losses at high frequencies. The limitations in switching frequency and material properties result in bulky and expensive passive components—including ac filter capacitors, inductors, and transformers—in currently available OBCs. As shown in Fig. 1, passive components contribute more than 30% of the charger cost in state-of-the-art Si-based technology.

As a result, OBCs

- add significant cost (~$106/kW), weight, and volume (e.g., the 2012 Nissan LEAF 6.6 kW OBC weighs 16.2 kg and has a volume of 10 L)
- are relatively inefficient (85–92%)

- are unidirectional (can charge the battery but are incapable of vehicle-to-grid support, a highly desirable function in future smart grids)

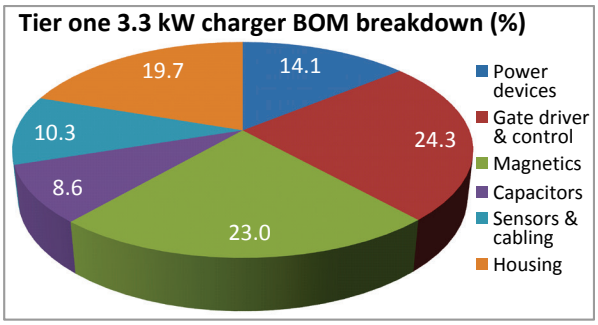


Figure 1: Bill-of-material breakdown for a tier one 3.3 kW OBC.

Emerging WBG devices, including SiC and GaN and advanced soft magnetic materials, are poised to offer significant improvements in ac-dc and dc-dc converters. Their ability to operate with enhanced efficiency over higher frequencies and temperatures minimizes passive component requirements and reduces cooling demands, providing opportunities for revolutionary strides in PE.

This project is targeted at leapfrogging existing Si-based charger technology to address charger and converter cost, weight, volume, and efficiency requirements. It proposes to overcome the limitations of existing semiconductor and magnetic materials by using WBG devices, advanced magnetic materials, and novel control strategies to significantly increase power density, specific power, and efficiency at lower cost.

Approach

Our strategy to address the limitations of state-of-the-art OBCs and dc-dc converters is multifold:

- Push the envelope on functional integration of the traction drive, 14 V dc-dc converter, and OBC.
- Take up the challenge of introducing WBG materials, specifically GaN, into automotive applications to determine what performance, packaging, cost, and efficiency benefits can be gained.
- Perform analysis, modeling, and simulation that lead to a functional prototype meeting VTO OBC specific power, power density, and efficiency requirements while significantly reducing the current cost levels.
- Design, build, test, and demonstrate prototypes.
- Work with U.S. DRIVE to develop insights and lessons learned from the automotive community pertinent to dc-dc converters and OBCs.
- Collaborate with industry stakeholders, universities, and other national laboratories to maximize the impact of this work.

Three technical approaches are being pursued. First, integrated bidirectional WBG OBCs will be developed that (a) provide galvanic isolation; (b) provide an integrated function for dc-dc conversion of high voltage to 14 V; (c) use soft switching at the dc-dc stage to reduce electromagnetic interference (EMI) and improve efficiency. Figure 24 shows an integrated dc-dc converter and charger architecture consisting mainly of an ac filter, a WBG front active converter, a dc bus capacitor, and a WBG isolation converter. The isolation converter integrates the functions for charging both the high-voltage traction battery and the 14 V battery for vehicle accessory loads. It includes high-frequency transformers and dc filters as well as WBG switches. A topology for the front end active converter and isolation converter was selected via simulation and experimental verification.

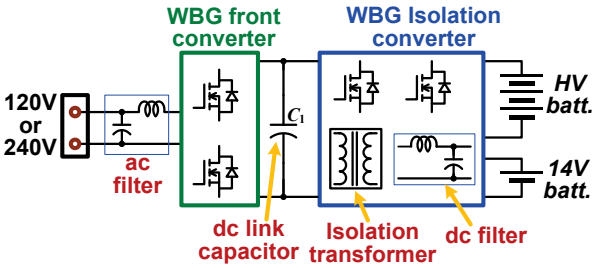


Figure 2: An integrated dc-dc converter and charger architecture.

Second, increasing power density and specific power without sacrificing efficiency is aggressively pursued by exploiting high switching frequency with WBG devices (especially GaN switches) and using advanced soft magnetic materials (nanocomposites) to drastically reduce the cost, weight and volume of the ac and dc filters and isolation transformer. Because the availability of WBG power modules is limited, SiC and GaN devices are purchased or obtained directly from device vendors, tested, characterized, and packaged for use in converter design and prototype development. Prototypes will be built and tested first using SiC devices—for which wafer processing and device fabrication technologies have advanced to the stage that SiC MOFETs and other switches are available commercially—and then GaN switches as that technology matures and devices with high current ratings become available.

Finally, a control strategy for the isolation converter will be developed to shrink the bulky dc link capacitor. This is necessary to filter out the large voltage ripple— with twice the grid supply frequency—inherent in single-phase ac-dc converters.

Three front end active converters were studied through simulation. The first is based on an ac/ac matrix converter that employs four pairs of switches of reverse blocking capability (Fig. 3). The main advantage of the ac/ac matrix converter is the elimination of the dc bus capacitor. However, because reverse blocking WBG switches are not available, the ac/ac matrix converter requires a switch and a diode connected in series for each of the switches shown in Fig. 3, significantly increasing conduction losses. We found that the efficiency penalty of existing SiC diodes makes it difficult to achieve the required charger system efficiency.

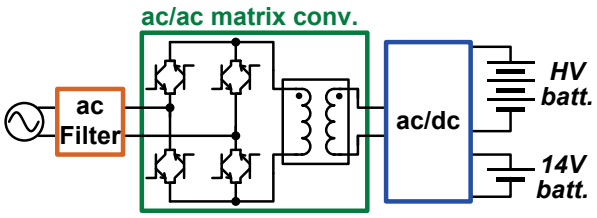


Figure 3: Using ac/ac matrix converter to eliminate the dc bus capacitor.

The second approach (Fig. 4) employs an H-bridge ac-dc converter and uses a ripple energy buffer to eliminate the ripple voltage. The ripple energy buffer uses a buck-boost converter to remove the pulsating ripple power from the main dc bus capacitor, C_1, and dump it to the energy buffer capacitor, C_2, significantly reducing the capacitance of C_1. This approach shifts the cost of the bulky dc bus capacitor to the additional switches and passive components of the ripple energy buffer. Therefore, the cost, weight, and volume savings in the dc bus capacitor must exceed the cost, weight, and volume added to the other components for this approach to be beneficial in reducing charger system cost, weight, and volume. Our simulation study shows this is not the case.

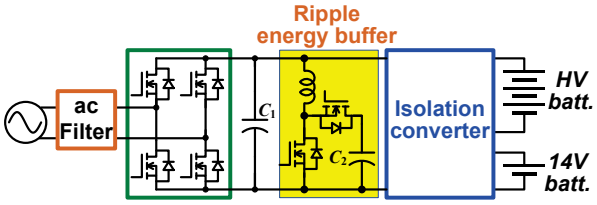


Figure 4: Use of a ripple energy buffer to eliminate the ripple voltage.

In the third approach, instead of using a ripple energy buffer, we developed a battery ripple current reduction control strategy for the isolation converter to reduce the bulky dc link capacitor (Fig. 5). Simulation results (see Results section) show the control strategy reduces the ripple current by 60%, enabling a significant reduction of the bulky dc link capacitor in the active front ac-dc converter.

Further, WBG traction drive inverters and motors will be operated as the active front converter and used to replace the ac filter inductor, significantly reducing the OBC cost, weight, and volume.

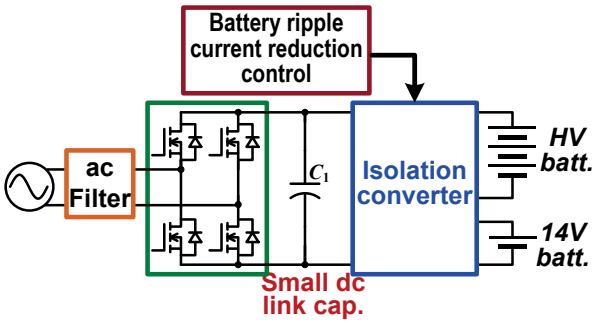


Figure 5: Using a battery ripple current reduction control strategy for the isolation converter to reduce the bulky dc link capacitor.

Figure 6 shows the integrated isolation converter topology selected through simulation. It is made up of a dual H-bridge phase shift dc-dc converter and a 14 V buck converter coupled through a high-frequency transformer. One H-bridge is connected to the high-voltage traction battery and the other to the active front ac-dc converter. Sharing of the transformer (for galvanic isolation) and other switch components between the OBC and the 14 V converter leads to substantial cost, weight, and volume savings for the OBC compared with a stand-alone counterpart. Other features of the integrated charger include these:

- It provides bidirectional power flow and thus can offer additional desired functions such as vehicle-to-grid and vehicle-to-home applications.
- It can charge the 14 V battery from the grid in addition to normal operation from the high-voltage traction battery.
- It uses the parasitic capacitance of the switches and the transformer leakage inductance to achieve zero-voltage switching for EMI noise reduction and efficiency improvement.
- The dual H-bridge converter enables the OBC to charge the battery over a wide range of voltages by providing a voltage buck and boost function through phase shift and duty ratio control.

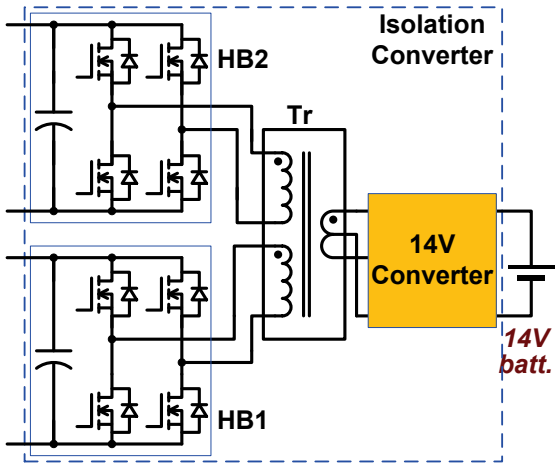
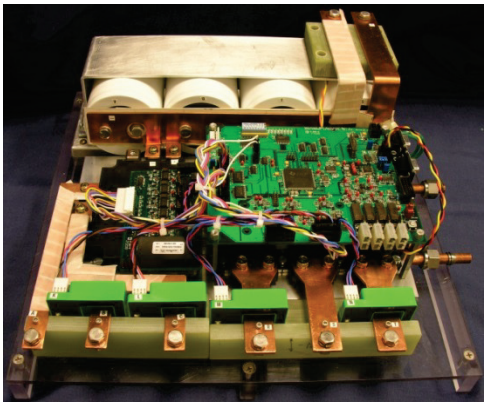


Figure 6: Isolation converter topology.

An Si-based 5 kW prototype consisting of an electrical drive system and an isolation converter was built to test the charging function and verify the selected topology. The isolation converter and the experimental results will serve as the baseline for comparison with WBG-based prototypes to be developed in the next phase of this project. The TDS consists of two inverters (one rated at 55 kW for the traction motor and one at 30 kW for the generator), a 10.9 kW induction motor, and a PM motor (used as a generator) rated at 8.2 kW. Figure 7 shows the inverters and test motors. The 55 kW inverter was fabricated with a 600 V/600 A six-pack intelligent IGBT module, and the 30 kW inverter was assembled with a 600 V/300 A six-pack IGBT module. The dc bus capacitor bank was constructed using four 375 µF film capacitors rated at 600 V. These components are mounted on a 12 by 7 in. water-cooled cold plate. Because of their relatively low power ratings, the measured zero-sequence resistances of the generator and motor are quite

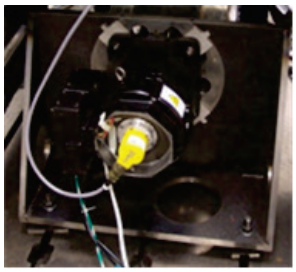
large—23.8 mΩ and 165.74 mΩ, respectively—compared with those of production HEV/EV motors. For example, the measured zero-sequence resistances of the 2007 Toyota Camry generator and motor are 21.58 mΩ and 10.75 mΩ, respectively. The combined zero-sequence resistance value of the test motors is thus 189.54 mΩ, more than five times that of the two motors in the Camry (32.32 mΩ). These high-resistance motors (manufactured by General Electric) will have a significant impact on the measured charger system efficiency in the following test results.

The isolation converter prototype, rated at 5 kW, was fabricated using superjunction Si power MOSFETs and a planar transformer with two high-voltage and one 14 V PCB windings. The parasitic capacitances of the MOSFETs, along with the transformer leakage inductance, are used for zero-voltage switching. Figure 8 shows the isolation converter prototype. All the components are mounted on an Al cold plate with a 6 by 7 in. footprint. Gate driver PCBs are mounted directly over the MOSFETs to eliminate wire connections between them. A control PCB using a TI TMS320F2808 fixed-point DSP controller is used to implement the dc bus voltage, grid current, battery charging voltage, and current control blocks. It is located on the top. Figure 9 shows the planar transformer, which is constructed using a flat ferrite core and heavy Cu PCBs for primary and secondary windings. The planar transformer measures 5×2.5×0.78 in.



(a) Inverters

(b) Induction motor



(c) PM motor

Figure 7: Photos of Si-based traction drive inverters and motors used in the charger tests.

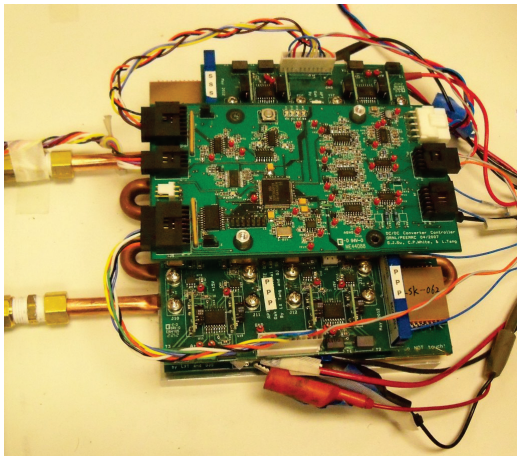


Figure 8: Photo of the 5 kW charger dc-dc converter.

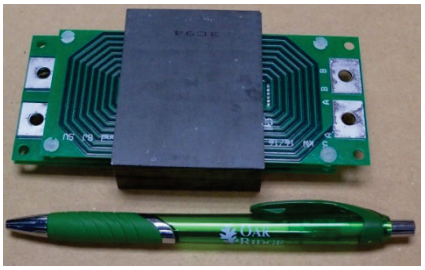


Figure 9: Photo of the planar transformer (footprint: 5 by 2.5 in.).

Results

Battery ripple reduction control

Figures 10 and 11 show simulated waveforms of the grid source voltage, battery charging current, and dc bus voltage in the selected topology shown in Fig. 5, with and without the battery ripple current reduction control. The control reduced battery ripple current by 60%, demonstrating the effect of the control strategy to use the isolation converter to reduce the bulky dc link capacitor.

Si-based isolation converter and charger system tests

The Si-based isolation converter prototype was first tested with a resistive load bank. Figure 12 gives typical operating waveforms, in which V_{bat}, v_{Tr1}, v_{Tr2}, I_{bat}, i_{Tr1}, and I_{in} are output dc voltage, transformer primary voltage, transformer secondary voltage, output dc current, transformer primary current, and input dc current, respectively. Smooth transitions in the transformer voltage waveforms indicate soft switching operations. Figure 13 plots measured isolation converter efficiency vs. output power. The efficiencies are greater than 97% for output power levels up to 5.2 kW, and the maximum value is 98.0 %.

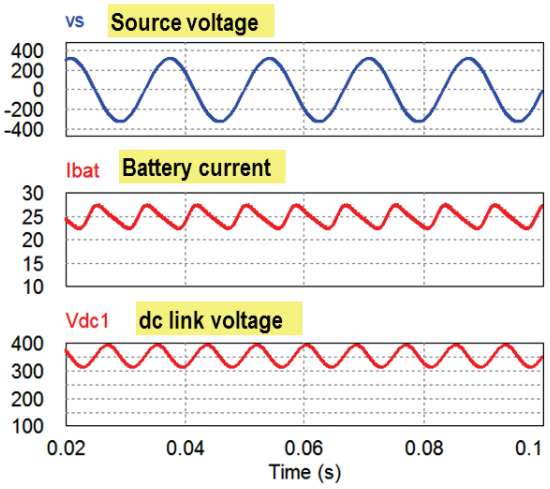


Figure 10: Waveforms showing large ripple in battery current without ripple reduction control.

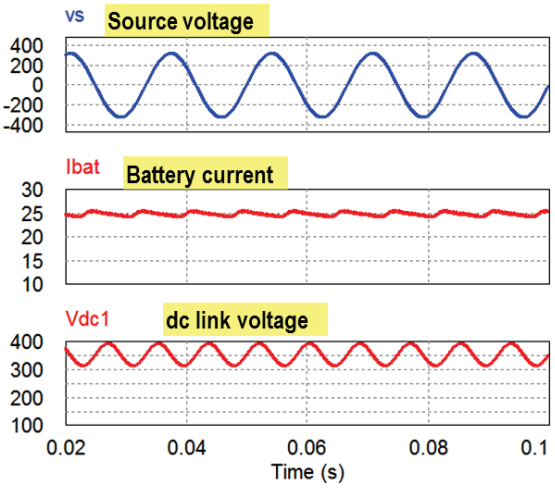


Figure 11: Waveforms showing significant reduction of battery ripple current with the ripple reduction control.

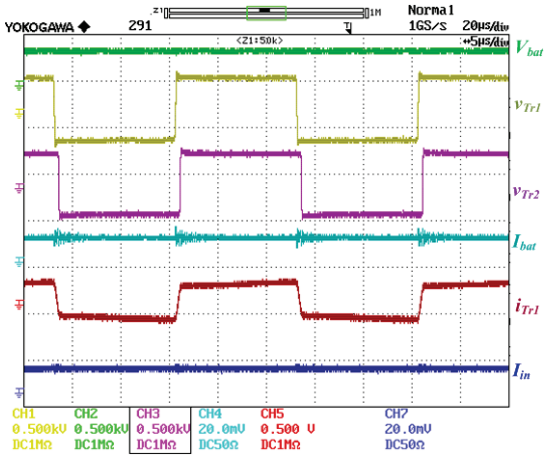


Figure 12: Isolation converter operating waveforms showing, from top, output dc voltage, V_{bat}, 500 V/div; transformer primary voltage, v_{Tr1}, 500 V/div; transformer secondary voltage, v_{Tr2}, 500 V/div; output dc current, I_{bat}, 20 A/div; transformer primary current, i_{Tr1}, 25 A/div; and input dc current, I_{in}, 20 A/div.

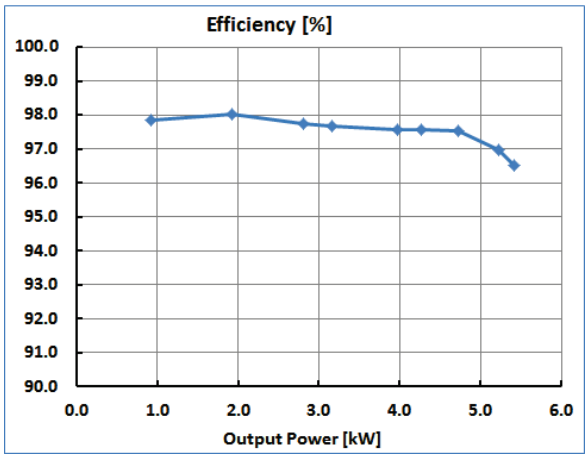


Figure 13: Measured efficiency of the 5 kW Si-based isolation converter.

The isolation converter and the traction inverters and test motors were then combined to function as an OBC, and the whole charging system was successfully tested at both 120 and 240 V grid voltages. Figure 14 shows typical operating waveforms of the system with a 120 V input voltage and 3 kW charging power. Figure 15 illustrates waveforms of the system with a 240 V input voltage and 5 kW charging power. Figure 16 plots the measured system efficiency of the charger at a grid voltage of 240 V. The maximum efficiency is 92.8%, which dropped to 90.0% at 120 V grid voltage. This efficiency reduction illustrates the impact of the Cu losses in the high-resistance test motors. It is thus reasonable to expect higher efficiencies for production EV/HEV motors, which have much lower stator winding resistances.

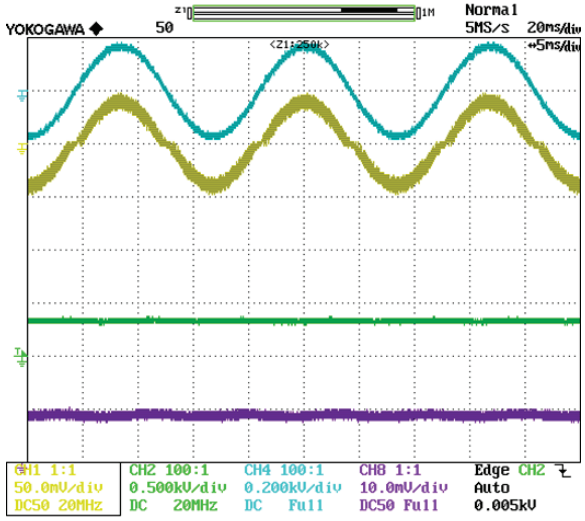


Figure 14: Waveforms of the charger system with 120 V input and 3 kW charging power. From top, grid voltage (200 V/div), grid current (50 A/div), charging voltage (500 V/div), and charging current (10 A /div).

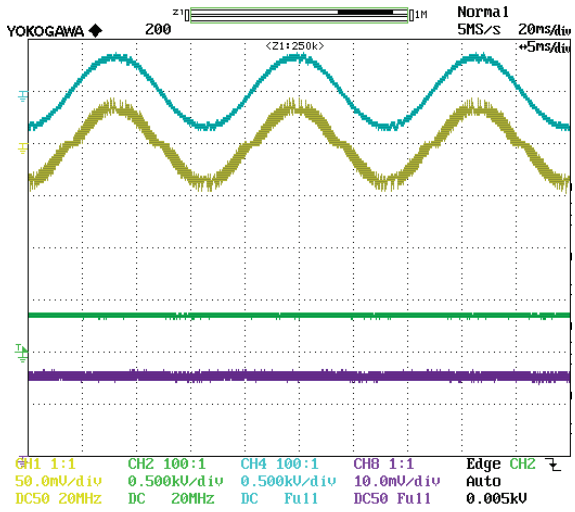


Figure 15: Waveforms of the charger system at 240 V input and 5 kW charging power. From top, grid voltage (500 V/div), grid current (50 A/div), charging voltage (500 V/div), and charging current (10 A/div).

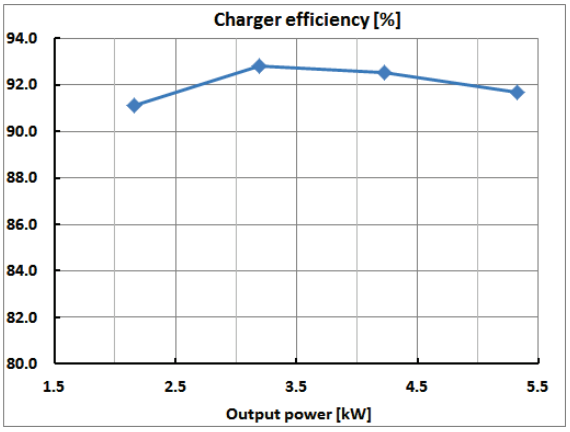


Figure 16: Measured charger system efficiency at a grid voltage of 240 V.

GaN device tests

Several low-voltage (<200 V) eGaN switches made by EPC were tested and characterized for possible use in the 14 V dc-dc converter. Using evaluation boards, a test setup was assembled for testing the eGaN switches in different 14 V converter topologies, including synchronous buck, boost, and full bridge converters. Test results were incorporated into the GaN switch simulation model for the 14 V dc-dc converter. The resultant converter model should produce more accurate results, enabling use of the simulation results for iterations of converter design optimization while reducing the need for experimental verification.

Figure 17 shows the EPC eGaN test setup and Fig. 18 shows typical EPC eGaN switching waveforms in a full-bridge dc-dc converter with 12 V output. Measured turn-on and turn-off times are 22 and 29 ns, respectively. A maximum efficiency of 94.7% was recorded at a switching frequency of 370 kHz with a resistor load.

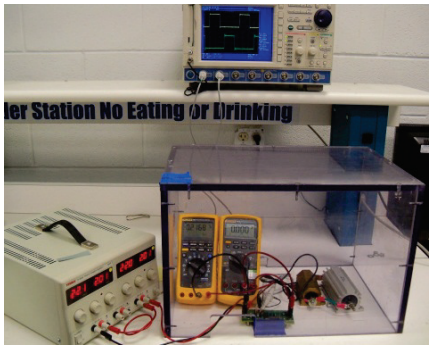


Figure 17: EPC eGaN test setup.

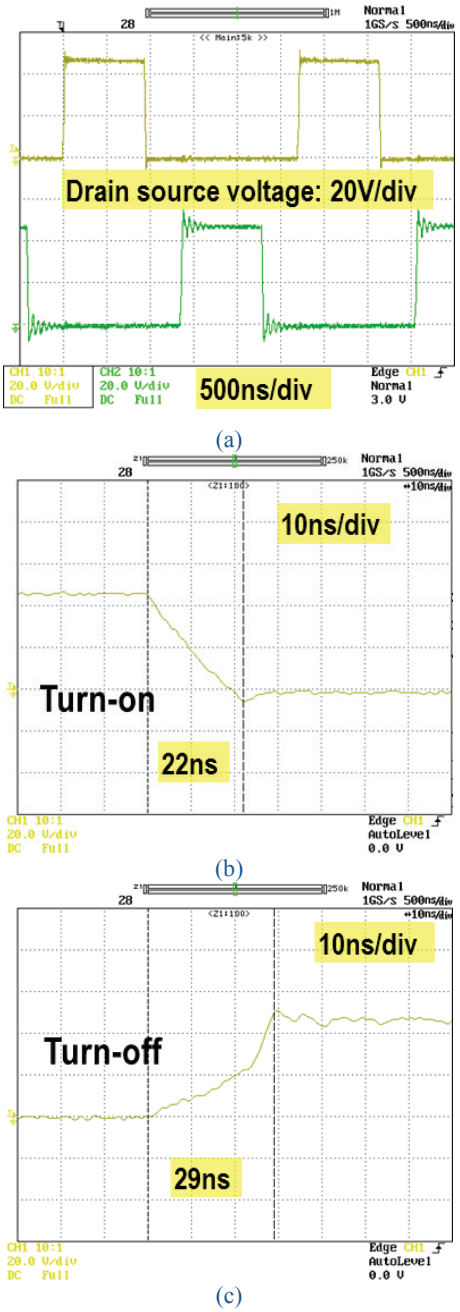


Figure 18: EPC eGaN voltage switching waveforms in a full-bridge dc-dc converter.

IR 600 V GaN switches were tested and evaluated for use in the high-voltage charger converters. A test board (Fig. 19) for characterizing the IR GaN switches packaged by Delphi was designed and fabricated. The test setup (Fig. 20) is flexible and can be reconfigured for double-pulse tests to measure switching losses and test loads in a half-bridge configuration for efficiency measurement. The test circuit includes an SiC Schottky barrier diode (SBD) in parallel with each of the IR GaN switches. The IR devices are packaged in a cascade connection of a normally-on GaN high-electron mobility transistor (HEMT) fabricated on a Si substrate and a low-voltage Si MOSFET, which makes them operate as normally-off switches.

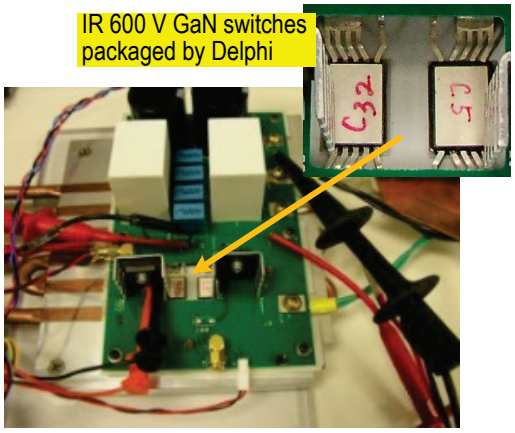


Figure 19: IR 600 V GaN switch test board.

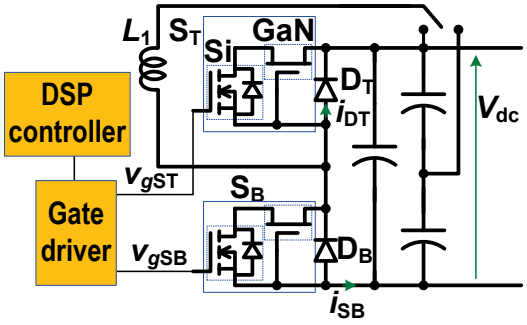
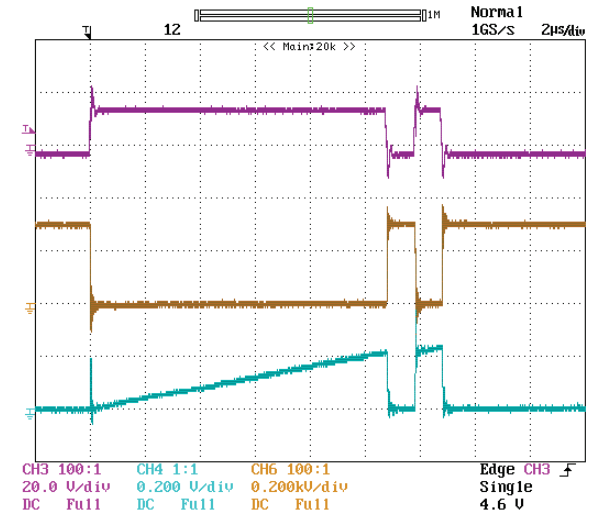
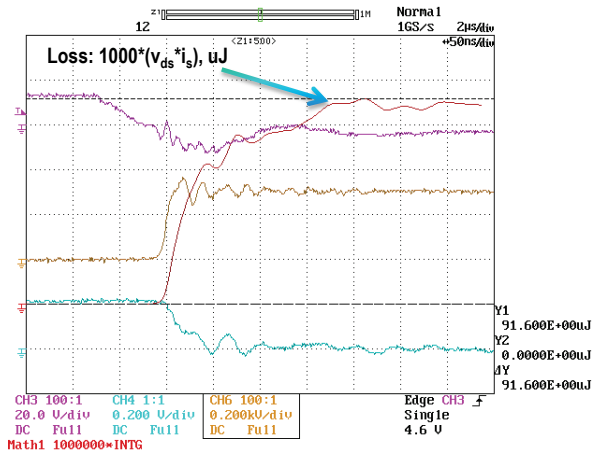


Figure 20: IR 600 V GaN switch test circuit.

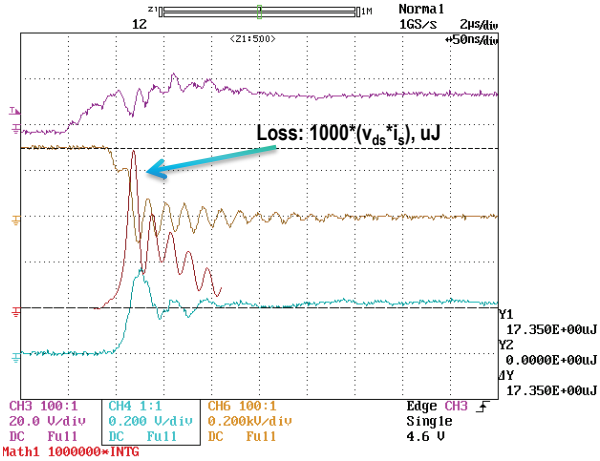
Double-pulse tests were first performed with the top switch, S_T, kept off or switched complementarily. Figure 21 shows double-pulse test results with S_T kept off and V_{dc}=300 V. Measured switching losses are 91.6 µJ for turn-off and 17.35 µJ for turn-on. Figure 22 shows double-pulse test results with S_T switched complementarily. Observing the diode current, i_{DT}, it is apparent that the GaN device can conduct current in the reverse direction at a lower voltage drop than the SiC diode. This indicates that the IR GaN switches can be used for synchronous rectification operation by turning on the switch while current is passing through the antiparallel SiC diode. The transition of current between the SiC diode and the GaN switch was also investigated for optimizing the gate control signals. The transitions took a rather long time, measured at about 500 ns.



(a) Full test cycle waveforms



(b) Turn-off



(c) Turn-on

Figure 21: Double-pulse test results with S_T kept off. CH3: v_{gSB}, 10 V/div; CH4: i_{SB}, 10 A/div; CH6: v_{DSB}, 200 V/div; 2 us/div.

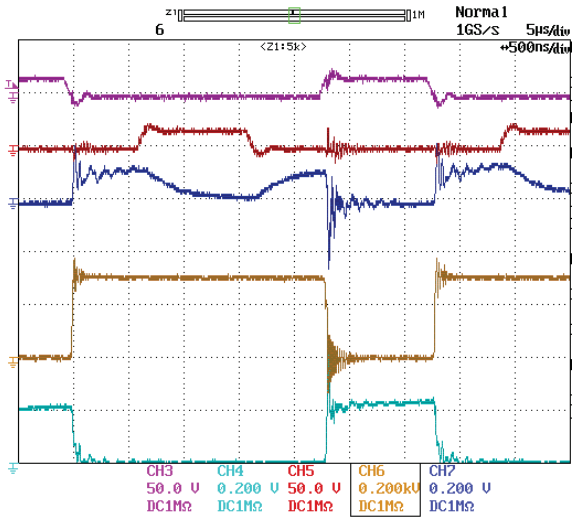


Figure 22: Double-pulse test results with S_T switched complementarily. CH3: v_{gSB}, 50 V/div; CH4: i_{SB}, 10 A/div; CH5: v_{gST}, 50 V/div; CH6: v_{DSB}, 200 V/div; CH7: i_{DT}, 10 A/div; 500 ns/div.

After the double-pulse tests, further experiments were carried out by operating the IR GaN switches in a half-bridge inverter with an inductor load at a dc bus voltage of 300 V and switching frequencies of 100–300 kHz. Figure 23 shows typical operation waveforms at a switching frequency of 300 kHz. Estimated efficiency is about 98% at an output power level[dmc2] of 1 kW.

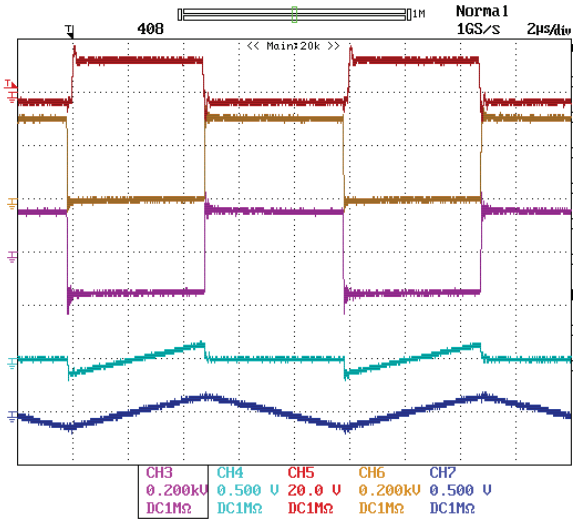
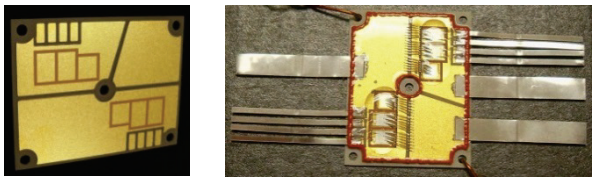


Figure 23: IR GaN switch operation waveforms in a half-bridge inverter with an inductor load. CH3: v_{out}, 200 V/div; CH4: i_{SB}, 25 A/div; CH5: v_{gSB}, 20 V/div; CH6: v_{DSB}, 200 V/div; CH7: i_{L1}, 25 A/div; 2us/div.

SiC-based isolation converter design

SiC switch phase-leg modules rated at 1,200 V/100 A were fabricated on ORNL-designed DBC substrates using Cree SiC MOSFETs and SBDs (Fig. 24).

Incorporating the results from the simulation study, a power circuit design for a 6.6 kW isolation converter using the ORNL-designed SiC phase-leg modules and planar ferrite cores was completed. Figure 25 is a 3D drawing of the isolation converter design. It comprises a primary switch PCB and its gate driver board, a secondary switch PCB and its gate driver board, a 14 V converter board, a DSP control board (top), and a planar transformer assembly. All the components are mounted on a 7 by 5 in. heat exchanger. At a switching frequency of 200 kHz, the transformer core size was reduced by 50% and the power module footprint by 15%, compared with the Si-based 5 kW baseline; a high converter efficiency of 98% was maintained.



(a) DBC card (b) Assembled SiC MOSFET module

Figure 24: DBC design and SiC switch phase-leg modules fabricated using the DBC cards.

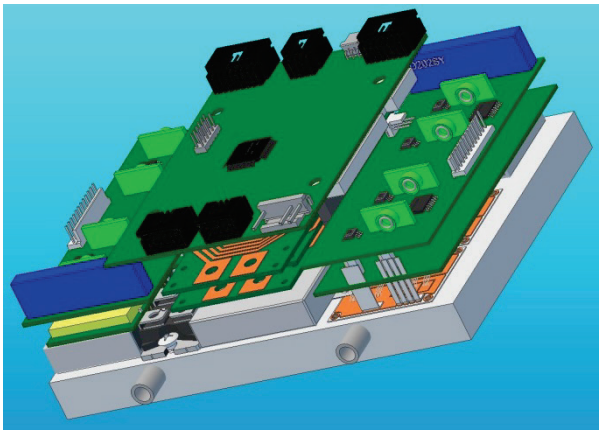


Figure 25: Three-dimensional drawing of the SiC isolation converter design.

Conclusions and Future Directions

This project is aimed at leapfrogging existing Si-based charger technology to address charger and converter cost, weight, volume, and efficiency. It proposes to overcome the limitations of Si semiconductor and magnetic materials by using WBG devices, including SiC and GaN; using advanced magnetic materials; and employing a novel integrated charger architecture and control strategy.

ORNL has developed a new integrated OBC and dc-dc converter architecture that significantly reduces the number of components (power circuit components alone are reduced by 47%, not counting savings in gate driver and control logic circuits). ORNL has built and tested a 5 kW Si-based prototype demonstrating an isolation converter peak efficiency of 98% and charger peak efficiency of 93%. Test results validated the new

integrated charger and dc-dc converter architecture and provide a baseline for measuring the benefits of WBG counterparts. ORNL also developed a control strategy for the charger isolation converter to reduce the battery ripple current—twice the ac main frequency—inherent in single-phase ac-dc converters. Simulation results show the control strategy reduces the ripple current by 60%, enabling a corresponding reduction of the bulky dc link capacitor in the active front end converter.

Emerging GaN devices fabricated on Si substrates are poised to offer significant improvements in power converters at a cost comparable to Si device costs. Their enhanced switching speed and reduced switching and conduction losses may enable these switches to minimize passive component requirements, a major driver of cost, weight, and volume in charger and dc-dc converters. ORNL has characterized both low-voltage (<200 V) and high-voltage (600 V) GaN switches, which generated valuable design data for hardware development of OBCs and dc-dc converters.

Incorporating the simulation results, ORNL completed a power circuit design for a 6.6 kW isolation converter using the ORNL-designed SiC phase-leg modules and planar ferrite cores.

Future work will be directed at building and testing prototypes for a 6.6 kW SiC isolation converter and OBC, a 6.6 kW GaN isolation converter and OBC, and a 2 kW GaN 14 V converter.

FY 2013 Publications/Presentations

1. G.J. Su, "WBG dc-dc and on-board charger," presented at the DOE Vehicle Technologies Program Advanced Power Electronics and Electric Motors R&D FY 2013 Kickoff Meeting, November 13–15, 2012.
2. G.J. Su, "WBG converters and on-board charger," presented at the 2013 DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, May 13–16, 2013.
3. G. J. Su and L. Tang, "An integrated onboard charger and accessory power converter for plug-in electric vehicles," 5th *IEEE Energy Conversion Congress and Exposition (ECCE 2013)*, pp. 1592–1597, September 15–19, 2013.

3.4 Power Electronics and Regenerative Energy Storage Systems Matching

Omer C. Onar, Ph.D. (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1467; Fax: 865-946-1362
E-mail: onaroc@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
E-mail: Susan.Rogers@ee.doe.gov

Start Date: October 2012
Projected End Date: September 2013

Objectives

- Develop a bi-directional buck-boost dc-dc converter between the RESS and the dc link (traction drive inverter input)
- Review and analyze bi-directional dc-dc converter architectures
- Model, simulate, and analyze a battery/ultracapacitor (UC) hybrid energy storage system (ESS)

Technical Barriers

The most important barrier is the boost ratio/range and efficiency that drive dc-dc converter architectural choices. A bi-directional dc-dc converter architecture should be selected depending on the difference between the battery voltage and the reference traction drive inverter voltage. Passive components of a dc-dc converter should be sized to keep the cost low and power density high with respect to the DOE VTO goals. Another significant barrier is the potential cost added by the dc-dc converter and hybrid ESSs. For example, in a battery/UC hybrid ESS, the UC increases the cost; however, it also reduces the battery size and prolongs its lifetime. These advantages are a tradeoff for the up-front cost of the UC.

Technical Targets

- Achieve power density of more than 13.4 kW/L
- Achieve specific power of more than 14.1 kW/kg
- Achieve a service life of more than 15 years or 13,000 h

Accomplishments

- Reviewed, modeled, and simulated bi-directional dc-dc converter architectures that interface the RESS with the traction drive inverter and created a summary review report discussing the operating principles, controls, advantages, and drawbacks of these converter architectures
- Reviewed and analyzed hybrid RESS architectures and created a summary report based on the advantages, drawbacks, control systems, performance, number of components, and other characteristics
- Reviewed, analyzed, modeled, and simulated four battery/UC hybridization strategies
  - Built simulation models of the battery and UC
  - Modeled hybridization architectures
  - Simulated a representative portion of the Urban Dynamometer Driving Schedule (UDDS) that includes acceleration, braking, and idling conditions for t = [690, 760] for these hybridization architectures
  - Collected data and compared the simulation results
  - Created a comparison results table for the RESS hybridization architectures

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Introduction

To provide more efficient propulsion without sacrificing performance or increasing fuel consumption, more than one energy storage device, each with different power/energy characteristics, can be used in PEVs. In such a system, proper power budgeting, based on the specific characteristics of energy sources, should result in higher efficiency, longer life and reduced wear on energy sources, and overall size and cost reduction. The combination of energy sources should be able to store, supply, and recapture high-power pulses in a typical or worst-case drive cycle, as well as supply the steady demands of the car. A hybrid architecture composed of a high-power-density component such as a UC and a high-energy-density component such as a rechargeable battery offers the advantages of both.

The energy storage devices in EVs should be able to meet demands the vehicle may encounter under any condition. Rechargeable chemical batteries are the traditional energy storage source for EVs. However, since the source needs to supply the peak power demands of the traction motor during transients and rapid accelerations, and since existing technologies do not provide a battery with sufficiently high power densities, the size and cost of the battery pack significantly increase if it is required to supply all the load demands.

A PEV traction battery may be sized to successfully meet the energy capacity needs for a given single-charge travel distance requirement. But since the present generation of highly energy-dense lithium-ion batteries has a relatively low power density, this single power source may not be capable of sourcing or sinking large, short bursts of acceleration or regenerative braking energy. Moreover, battery longevity is directly related to both the depth of discharge and the quantity of micro or macro charge/discharge cycles, i.e. the short, powerful charge/discharge cycles associated with sharp acceleration and hard regenerative braking. Battery C-rate is the parameter that expresses battery discharge intensity; in a battery-powered system, because low C-rates tend to increase battery life span, instantaneous charge/discharge pulses or fast fluctuating currents should be avoided. The problems associated with cycling batteries at high C-rates include decreased capacity, excessive heating (which requires additional cooling), and increased dc resistance (ESR). Capacity and ESR are the metrics used to define battery performance and therefore end of life.

Without a secondary ESS, the battery pack must supply all vehicle power demands. The result may be an oversized system with massive energy density to compensate for power density shortcomings. This may increase the size and cost of the battery pack or, if a smaller pack is used, shorten the battery lifetime and cause thermal runaway problems. For this reason, UCs are proposed, because of their higher specific power and cycling efficiency, to relieve peak power transfer stresses on the battery bank. A hybrid system combining these two energy sources, batteries and UCs, can not only better meet both the energy and power requirements of the drive train but also provide the flexibility of using smaller batteries with less peak output power. Because of their very low internal resistances, UCs have very small time constants and can deliver high-power charge and discharge pulses for relatively short durations. The manufacturer performance ratings for certain UCs state a 20% decrease in initial capacitance and doubling of internal resistance over a period of 1,000,000 cycles. Curves showing whether this wear and tear is linear or nonlinear over time are not provided, but it is not likely that a system with a 1,000,000 cycle rating would see serious degradation for a substantial length of time or energy throughput.

Employing UCs with batteries in a proper, efficient, and cost-effective manner can increase the peak current capacity of the overall architecture. Therefore, the hybrid architecture could benefit from intermediate storage of high power in a buffer stage designed to deliver or receive current for the highest peaks, thus reducing both the number and the depth of battery discharge cycles.

Approach

This section reviews and describes hybrid battery/UC architectures.

Passive parallel hybrid architecture

In the passive parallel configuration, the battery and UC are connected directly in parallel without any interfacing converter. Combining two power sources passively in parallel is the simplest method, as the output voltages of both sources are automatically equalized by virtue of being directly connected to the same bus. The passive parallel connection architecture is shown in Fig. 1 with the bi-directional converter interfacing the common ESS bus to the dc link and motor drive. Since the converter is operated to provide a constant input voltage to the dc link /motor drive, increasing the mechanical load on the machine will tend to increase the motor current, decreasing the dc link voltage. This will cause more power to be drawn from the ESS through the bi-directional converter to return the dc link to its nominal voltage. On the other hand, whenever braking occurs, the motor drive operates as a generator and recaptures the braking energy to the dc link. Therefore, dc link voltage increases during braking or a reduction in mechanical load, and the bi-directional converter is operated in reverse (from dc link to ESS bus) to regulate the dc link voltage.

This architecture provides simplicity and cost effectiveness for hybrid ESSs. In this connection architecture, it is expected that the UC will act faster than the battery because of its lower time constant. Therefore, it is anticipated that the UC will provide transients and fast power variations while the battery supplies a relatively slow varying current as a result of its slower dynamics.

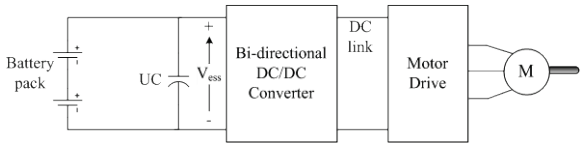

Figure 1: Passive parallel connection architecture.

However, immediately after current is drawn from the UC, because the UC and battery are directly connected, the battery will supply a similar current profile for voltage equalization, since there is no active battery current waveform shaper, limiter, or controller. The lack of effective control of battery current presents a drawback to the passive parallel connection architecture. In addition, the nominal battery and UC voltages must be sized to match, further restricting the system configuration.

Ultracapacitor/battery cascaded hybrid architecture

The most common UC/battery configuration connects the UC terminals to the dc link through a bi-directional dc-dc converter. In this architecture, the battery is directly connected to the dc link and a bi-directional interface is used for UC connection (Fig. 2). Figure 3 shows another common view of the same connection architecture. In this case, the power contribution from the UC can be effectively controlled, and the bi-directional dc-dc interface helps to efficiently and more completely recapture braking energy. Moreover, a UC voltage can be selected that is different from the nominal dc link voltage. This allows the UC energy capacity to be increased or decreased regardless of the system dc voltage, as UC energy capacity varies by the square of its voltage. Since the battery is directly connected to the dc link, input voltage to the motor drive is relatively constant and further dc-link voltage regulation is not required. This provides simplicity of control so that voltage control loops may be eliminated.

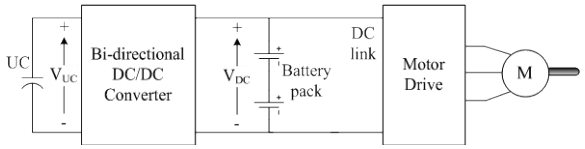

Figure 2: Ultracapacitor/battery configuration.

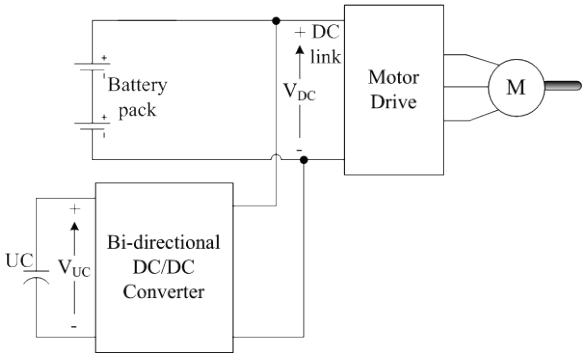

Figure 3: Another representation of the same ultracapacitor/battery configuration.

The disadvantage of this architecture is that the braking energy captured by the battery is not directly controlled. Braking energy recovered by the battery depends on the power level, battery state of charge (SoC), and amount of energy captured by the UC. The other drawback is that the bi-directional dc-dc converter must operate properly even with low UC voltages and therefore higher current values, so current ratings of the switches and other PE should be chosen appropriately.

Battery/ultracapacitor hybrid architecture

For the battery/UC architecture shown in Fig. 4, the device positions are simply switched compared with the UC/battery configuration.

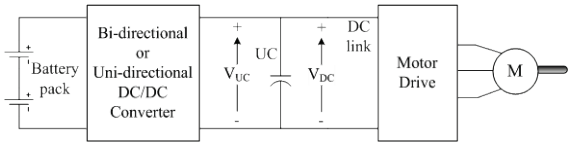

Figure 4: Battery/ultracapacitor architecture.

The main advantage of this architecture is that the battery voltage can be maintained at a lower level. During braking, the UC is recharged directly from the dc link; and some portion of the braking energy, appropriately current-limited, can be transferred to the battery. Since the UC is directly connected to the dc link, it acts as a low-pass filter and takes care of fast load transients. However, the battery pack should be controlled so that it continually maintains an appropriate voltage across the UC and dc link. The control strategy for the battery pack may be designed so that it supplies the average and slow-changing load variations while the UC supplies the rest, acting as a buffer with faster dynamics. If the UC is not large enough or charged continually, the dc link voltage will be allowed to fluctuate over a wide range; in this case, the motor drive inverter should be capable of operating over a large input voltage range.

In this architecture, for simplicity and cost effectiveness, the battery pack converter can be unidirectional. Since the overall system is that of a PEV, the battery pack can be configured to receive a charge only from an onboard generator or an external source. The UC can be the only device responsible for capturing braking energy. This scheme would provide a significant amount of simplicity for power budgeting during braking.

Cascaded hybrid architecture with two converters

As another alternative, one energy storage device can be cascaded to the motor drive through a dc-dc converter and the other cascaded through a first and second dc-dc converter. The cascaded converters configuration is presented in Fig. 5.

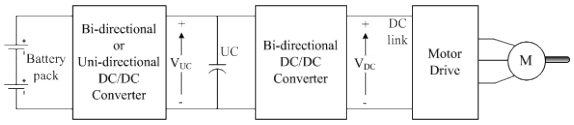

Figure 5: Cascaded converters configuration.

In this configuration, both battery and UC voltages can be decoupled from the system voltage and from each other. It is preferred that the battery converter control the battery output current and therefore the stress on the battery. If the UC is undersized or the battery converter not appropriately controlled, the UC voltage can vary substantially. At low UC voltages, the input current to the UC converter can be very high, leading to higher conduction losses and a need for switches rated for high current. Additionally, the UC dc-dc converter must provide stable operation over a wide voltage input range.

The major disadvantage of the cascaded converter architecture is that additional losses may be encountered at the battery power flow path because there are two cascaded converters between the battery and dc link. The battery converter can again be a unidirectional converter for control and configuration simplicity. In the case of a boost converter for the battery, the battery power contribution can be controlled easily by current control mode. The UC converter can be controlled for dc link regulation, and the battery can be controlled so that it supplies a smoother current profile during the operation.

As in the battery/UC architecture shown in Fig. 4, the positions of the battery and UC can be switched, leading to a slightly different cascaded converters architecture. However in this case, the power contribution from the UC might result in more fluctuation voltage applied to the battery terminals. On the other hand, since the battery is the dc link–side energy storage device, dc link voltage regulation could be easily accomplished by the use of a nearly constant battery voltage.

Multiple parallel converters hybrid architecture

In a multiple parallel converter architecture, each energy storage device has its own bi-directional dc-dc converter for interfacing with the dc link, and the output of all converters is held in parallel. A block diagram of this architecture is shown in Fig. 6.

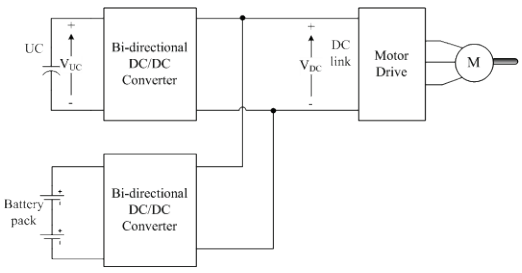

Figure 6: Multiple parallel connected converters architecture.

Although this architecture is called a multiple input converter, it is not a "true" multiple input converter since each energy storage device has an individual converter and their contributions to the dc link are paralleled. This architecture offers the most flexibility and offers more functionality than the cascaded converters architecture. The battery and UC voltages are decoupled from each other as well as from the dc link voltage. Since the power controls and power flow paths from the energy storage devices are totally decoupled, this architecture is superior in terms of stability, efficiency, and control simplicity. Reliability is also improved because one source can keep operating even if another fails.

The battery can be operated in current control mode, supplying the load variations averaged and smoothened over a period of time. Meanwhile, the UC can be operated in voltage control mode, maintaining a nearly constant voltage across the dc link. Therefore, the UC will supply fast load variations and transients during both rapid acceleration and sudden braking. This is because these load activities directly affect the dc link voltage, and as long as dc link voltage is regulated quickly enough, all load demands will be satisfied.

The bi-directional dc-dc converters discussed for the architectures described in this section could be typical two-quadrant converters, able to operate in boost mode in one direction and buck mode in the other (Fig. 7). This architecture is also called a half-bridge bi-directional dc-dc converter.

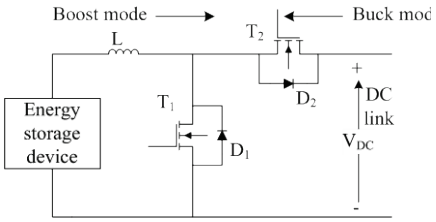

Figure 7: Bi-directional dc-dc converter.

As shown in Fig. 7, for power flow from an energy storage device to the dc link, inductor *L*, switch T_1, and diode D_2 form a boost converter. To accommodate power flow from the dc link to an energy storage device, switch T_2, diode D_1, and inductor *L* form a buck converter. Of course, other types of bi-directional converters could also be used. Some of them are presented in the following subsections.

Multiple dual active bridge converters hybrid architecture

It is known that conventional buck-boost converters can step the source voltage up or down at the cost of inducing a negative voltage output. Therefore, an inverting transformer is usually employed to obtain a positive output voltage. Although the transformer adds cost and volume, it may be advantageous when there are two input sources for both isolation and coupling. Two buck-boost type dc-dc converters for the UC and battery can be combined through the magnetic coupling of a transformer reactor. However, neither conventional buck-boost nor buck-boost with transformer architectures is suitable for vehicle propulsion systems because they are not capable of bi-directional operation. On the other hand, dual-active-bridge dc-dc converters can be employed for the combined operation of batteries and UCs. Although transformers typically add cost and volume to a system, the transformer in the dual-active-bridge converter operates at very high frequency and may therefore be very small and cheap. Having a transformer in the converter architecture may be advantageous when there are two or more input sources because they can be combined through the magnetic coupling of a transformer reactor. A dual-active-bridge converter with two input sources is presented in Fig. 8. Although this architecture completely isolates the input sources from the dc link, it requires a greater number of switches at increased cost. If only isolation is required, the number of switches can be reduced by employing half-bridge inverters/rectifiers instead of full-bridge versions. This dual-active bridge architecture with half-bridge converters would cut the number of switches in half (Fig. 9).

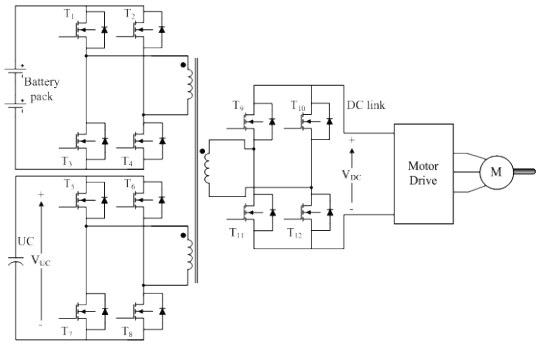

Figure 8: Dual-active-bridge converter with full-bridge converters.

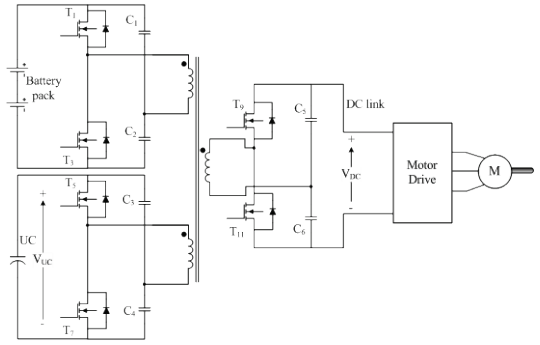

Figure 9: Dual-active-bridge converter architecture with half-bridge converters.

Dual-source bi-directional converters

In the multiple converters configuration discussed earlier, each converter shares the same output and so the combination of converters occurs at the output. A dual-source bi-directional converter configuration applies the combination at the input, instead of paralleling the converter outputs at the dc link. This configuration is presented in Fig. 10.

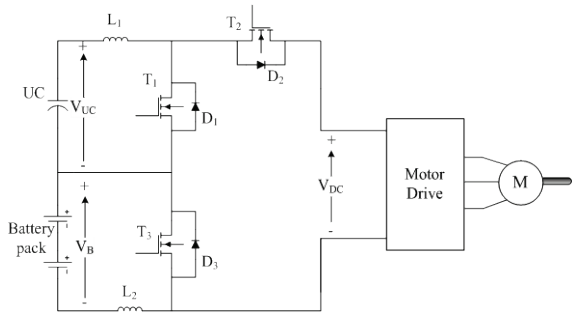

Figure 10: Dual-source bi-directional converters architecture.

Although this architecture is similar to a multiple parallel-connected converter configuration, there is one less switch in the dual-source input case. For the UC, inductor L_1, switch T_1, and diode D_2 form a boost converter when transferring power from the battery to the dc link. For the battery, inductor L_2, switch T_3, and D_1-D_2 path form a boost converter when transferring power from the UC to the dc link. During regenerative braking, the interface should be operated in buck mode. Switch T_2, diode D_1, and inductor L_1 form a buck converter from the dc link to the UC. On the other hand, some regenerative braking energy can be conveyed to the UC by applying a PWM signal to T_1. In this case, switches T_2 and T_1, diode D_3, and inductor L_2 will form a buck converter from the dc link to the UC. By applying an appropriate duty cycle to T_1 and T_2, braking energy can be properly shared. Although one switch is eliminated, a complicated control system is the main drawback of this configuration compared with the multiple converter configuration.

Multiple modes single converter hybrid architecture

In this design, only one bi-directional converter is required, and the UC voltage is selected to be higher than the battery voltage. The UC is directly connected to the dc link to supply peak power demands, and the battery is connected to the dc bus through a diode. The bi-directional dc-dc converter is connected between the battery and UC (Fig. 11) to transfer power between them. This converter is controlled to maintain a higher voltage across the UC than the battery; therefore, the diode is reverse-biased for most of the operation.

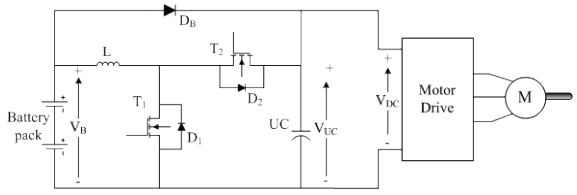

Figure 11: Single bi-directional converter architecture.

This converter has four different modes of operation: low-power, high-power, regenerative braking, and acceleration.

In low-power mode, it is assumed that the total power demand is less than the power capacity of the bi-directional converter. In this mode, since the UC/dc link voltage is higher than the battery voltage, the diode D_B is reverse-biased. Since the power demand is lower than the capacity of the bi-directional converter, there is not any power flow from the battery to the dc link. The battery only supplies power to the UC to keep its voltage at some pre-determined higher level.

Whenever the power demand of the vehicle is greater than the converter power capacity, the system operates in high-power mode. In this mode, the UC voltage cannot be maintained at that high value since the power from the battery to the UC is less than the power from the UC to the dc link. In this case, diode D_B is forward biased, and battery also directly supplies power to the dc link along with the UC.

In regenerative braking mode, since the UC is directly connected to the dc link, it is recharged by virtue of its position in the circuit, whereas diode D_B blocks the dc link power to prevent recharging of the battery directly. Some portion of the recaptured braking energy can be transferred to the battery through the bi-directional converter. Therefore, this mode provides controlled recharging for the battery; i.e., whenever the UC is fully charged but there is still regenerative energy available, the rest of the energy can be transferred to the battery so long as the regenerative current does not exceed the maximum battery charging current. In the latter case, mechanical brakes could be used to keep the battery current below the maximum limit.

When the vehicle first starts to accelerate, the voltage across the UC is higher than that of the battery and equal to that of the dc link. Power demand on the vehicle is high, and UC voltage therefore drops. During acceleration mode, the UC discharges through the dc link, and the battery supplies power to the dc link through the bi-directional converter. Whenever the dc link voltage decreases to the level of the battery voltage, D_B becomes forward biased and the system switches to high-power mode.

The advantage of this architecture is that it requires only one converter. However, although power is shared between the battery and UC during different modes, the battery current is not effectively controlled. This is especially the case in regenerative mode, with its potentially sharp transients.

Interleaved converter hybrid architecture

The combination of battery and UC can also be achieved by using interleaved converters. The interleaved converter configuration is composed of a number of switching converters connected in parallel as shown in Fig. 12.

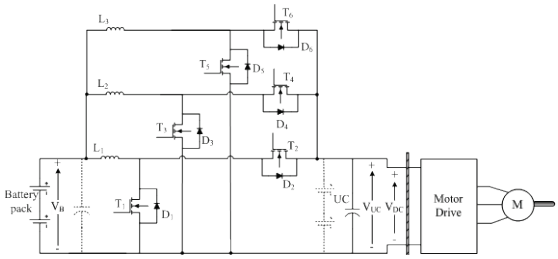

Figure 12: Parallel interleaved three-stage bi-directional converter.

When low current ripples or very tight tolerances are required, interleaved converters tend to be preferred. Interleaved converters offer much lower inductor current ripple compared with regular bi-directional converters, and the overall efficiency for a given power requirement is greater because each interleaved architecture has a smaller power rating and smaller overall loss. Interleaved converters also have faster transient response to load changes.

As shown in Fig. 12, the battery is interfaced to the UC terminals through the interleaved converters, with the UC directly connected to the dc link. Alternatively, UC and battery positions can be reversed as shown by the dashed lines in Fig. 12. In addition to these two configurations, the interleaved converters can be employed within other architectures presented in this section.

Switched capacitor converter hybrid architecture

Another bi-directional interface that combines battery and UC operation in a PEV is the switched capacitor converter (SCC). An SCC is basically a combination of switches and capacitors. By different combinations of switches and capacitors, these converters can produce an output voltage that is higher or lower than the input voltage. In addition, reverse polarity at the output can be provided if necessary. The capacitor can be charged or discharged through various paths formed by the controlled switches. Four switches, three diodes, and one switched capacitor can be used for a typical SCC. SCCs can have a large voltage conversion ratio with very high efficiency; therefore, they appear to be well suited for automotive applications.

An example of a battery/UC combination through an SCC is provided in Fig. 13.

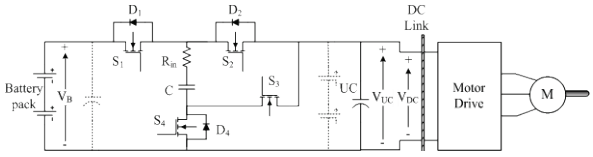

Figure 13: Switched capacitor converter configuration.

Based on the circuit configuration shown in Fig. 13, battery energy can be delivered to the load side by buck mode operation and the battery can be recharged by boost mode operation. In buck mode, switches S_1 and S_4 are turned ON until capacitor C is charged to some desired voltage level less than that of the battery. At that point C is disconnected from the battery terminal by turning switches $S1$ and $S4$ OFF, and connected to the load by turning switch $S2$ ON to transfer its stored energy through S_2 and diode D_4. In boost mode, C can be charged from the load side through D_2 and S_4. After this stage, S_3 and D_1 become the operating switches and the energy in C is discharged to the battery side. This control strategy offers control simplicity, continuous input current waveform in both modes of operation, and low source current ripple.

As shown in Fig. 13, the battery is interfaced to the UC terminals through the SCC, and the UC is directly connected to the dc link. Alternatively, UC and battery positions can be reversed, as shown by the dashed lines in Fig. 13. In addition to these two configurations, the SCC can be employed within other architectures as a bi-directional converter.

Multiple input converter–based hybrid architecture

In the architectures discussed previously, battery and UC energy storage devices were employed through their individual dc-dc converters. Unlike these configurations, the multiple input dc-dc converter has the flexibility of adding a number of inputs at the added cost of one switch and one diode (two switches and two diodes in the case of bi-directional operation). The multiple input dc-dc converter architecture schematic with battery and UC input sources is shown in Fig. 14.

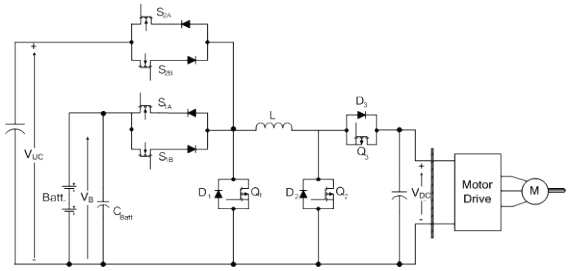

Figure 14: Multiple input dc-dc converter architecture.

In this converter architecture, the inputs share the same converter inductor and are connected through bi-directional switches. This converter is capable of operating in buck, boost, and buck-boost modes for power flow in both directions. The assumption of continuous inductor current requires that at least one input switch or diode be conducting at all times. The respective input diode is ON if all the input switches are OFF. If more than one switch is turned ON at the same time, the inductor voltage equals to the highest input voltage.

Under acceleration conditions, both sources deliver power to the dc link. Since the UC voltage varies in a wider range than that of the battery, battery voltage can be selected to be higher than UC voltage for simpler operation. Since the battery voltage is higher, S_{2A} is turned ON in boost mode. Switch Q_2 can be switched to control the inductor current, and power flow from the battery to the UC can be controlled by switch S_{1A}. Diode D_3 conducts when Q_2 is turned OFF. During deceleration, the braking energy is transferred from the dc link to the energy storage devices, and the converter is operated in buck mode. Since the UC voltage is less than the battery voltage, S_{1B} is always turned ON. Switch Q_3 can be used to control the inductor current. Power sharing between inputs is accomplished by controlling S_{2B}. Diode D_2 cannot conduct until switch Q_3 is turned OFF.

The main advantage of this architecture is that only one inductor is required for the whole converter even if more inputs are connected. This advantage can decrease the volume and weight of the converter significantly compared with multi-inductor or transformer architectures. Conversely, power budgeting in both boost and buck modes is very challenging and requires advanced control design.

Results

Three example hybridization architectures for the combined operation of batteries and UCs were modeled and simulated: (1) a passive parallel configuration architecture, (2) a battery/UC cascaded connected converters architecture, and (3) a parallel connected multi-converters configuration. The following discussion makes a case for the effectiveness and feasibility of each one. For the simulations, a representative portion of the UDDS was used for the time interval t=[690, 760]. This driving cycle period of 80 seconds includes acceleration, braking, and idling conditions. A typical mid-size electric vehicle was used for the analysis. For the UC, a Maxwell BMOD0165 module was used with a nominal capacitance of 165 F, rated voltage of 48.6 V, equivalent series resistance of 6.3 mΩ, and peak current of 1970 A. Since one of the test architectures calls for a passive-parallel connection, the UC voltage should be chosen so that it

is close to the battery voltage. Therefore, seven BMOD0165 modules were connected in series, resulting in 23.57 F capacitance, 340.2 V rated terminal voltage, and 44.1 mΩ of internal series resistance.

Simulation and analysis of passive parallel configuration

In this configuration, the battery and UC are connected directly in parallel without any interfacing converter between them, and the common battery/UC terminals are connected to the dc link through a bi-directional converter. The power demand for the vehicle was obtained through PSAT (Powertrain System Analysis Toolkit) simulations of a typical mid-size sedan vehicle configured as a PEV. Since the motor drive voltage is almost constant, the power demand of the vehicle can be divided by the dc link voltage to obtain the motor drive current; and the motor drive and load demand variation were therefore modeled and implemented as a controlled current source.

During the simulation, the reference dc link voltage was selected as 400 V, and the bi-directional converter was controlled through a double-loop voltage and current controller. A PI controller was used in the voltage loop, and a peak current mode controller was used in the current loop (Fig. 15).

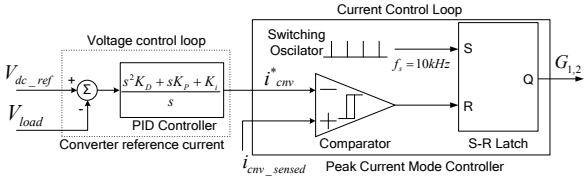

Figure 15: Control system for the passive parallel connection architecture.

The load current for the t=[690, 760] time interval varies, as shown in Fig. 16. The load current includes positive and negative current variations, simulating acceleration and braking conditions. Based on this load current variation, the bi-directional converter is controlled so that it maintains a constant dc link voltage while supplying power from sources during acceleration and recharging them during braking. The battery and UC current variations are shown in Figs. 17 and 18, respectively.

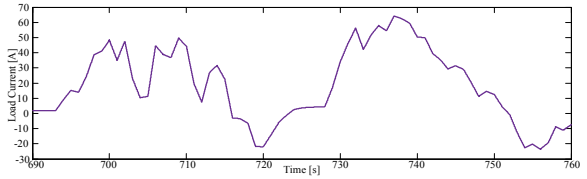

Figure 16: Load current variation.

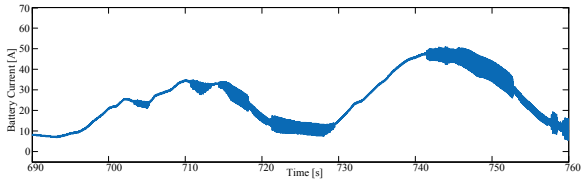

Figure 17: Battery current variation in passive parallel configuration.

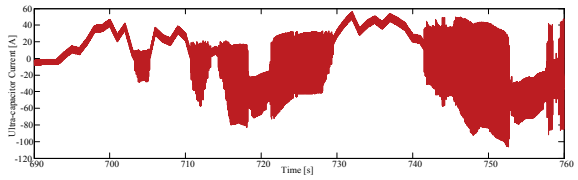

Figure 18: Ultracapacitor current variation in passive parallel configuration.

The battery inherently supplies a smoother current profile than does the UC because of its slower dynamics. However, since no interface controls the battery current, its current has some fluctuations that could likely be eliminated by other connection architectures. Because of the voltage balance between the battery and UC, battery current varies automatically to maintain a terminal voltage similar to that of the UC at all times. If the UC voltage were higher than the battery voltage as a result of a large braking energy recovery, the battery current would reverse direction; but here only the UC receives power from the application of regenerative braking.

The SoC variations of the battery and UC are shown in Figs. 19 and 20, respectively.

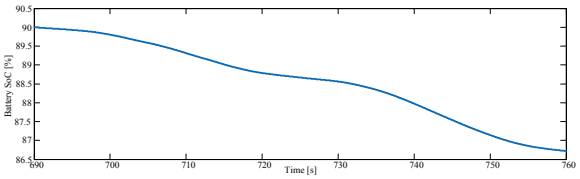

Figure 19: Battery SoC for passive parallel configuration.

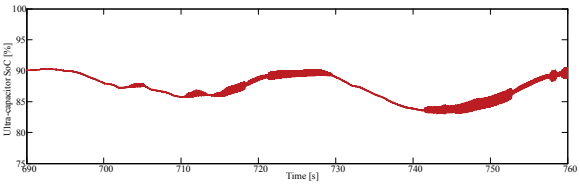

Figure 20: Ultracapacitor SoC for passive parallel configuration.

The initial SoCs for both battery and UC were selected as 90%. Since the battery voltage is higher than the UC voltage, the battery is always discharging, as was explained for the current variations. However, the SoC of the UC is sometimes increasing as it recharges during braking conditions, i.e., the negative current variations of the UC.

Finally, the dc link voltage variation, to which the motor drive inverter is connected, is shown in Fig. 21. As observed from Fig. 21, the dc link voltage varies steadily around the 400 V reference set point. During periods of high power demand and the operation mode changes of the bi-directional converter, voltage fluctuations increase. For this architecture and control strategy, the maximum voltage seen at the dc link is 405.3 V and the minimum is 395.2 V. Therefore, the maximum amplitude of the voltage fluctuation is 2.5% over the simulation period.

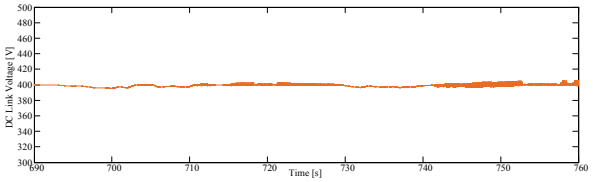

Figure 21: The dc link (load bus) voltage variation for the passive parallel configuration.

Simulation and analysis of cascaded converters configuration

In the cascaded converter configuration, the battery is connected to the UC through a bi-directional converter, and the UC is connected to the dc link through another bi-directional converter; therefore, the battery, converter 1, UC, and converter 2 are all in cascade connection. The same drive cycle over the same time interval used in the previous simulation was used for load modeling of this architecture. The dc link voltage reference was kept at 400 V. For the UC controls, a double-loop controller was employed for dc link voltage regulation; for the battery controls, only a peak current mode controller was used. The reference current for the battery can be obtained as

$$I^{*}_{batt} = \frac{V_{load} \times I_{load}}{V_{batt}} G_{LP}(s)$$

where I^{*}_{batt} is the battery reference current, V_{load} and I_{load} are the instantaneously measured dc link voltage and current, and V_{batt} is the battery terminal voltage, which is nearly constant during the whole drive cycle. The transfer function represented by $G_{LP}(s)$ is a low-pass Bessel filter that is applied to eliminate any spikes and fast transients from the battery reference current. A Bessel filter is a linear filter with maximally linear phase response and minimal flat group delay; it is characterized by almost constant group delay across the entire passband, thus preserving the waveform of the filtered signals with minimal delay. These fast transients come inherently from the variation in instantaneously measured load current. The Bessel filter can make the battery current smoother and reduce the stress on the battery because there is an additional converter regulating battery current. The battery current controller is depicted in Fig. 22.

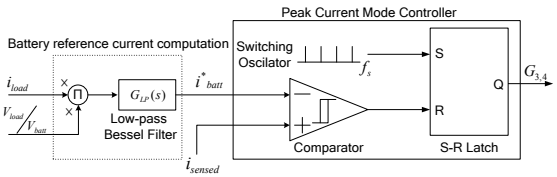

Figure 22: Battery current controller.

The load current drawn from the dc link varies as is shown in Fig. 16, and vehicle specifications and battery and UC parameters are the same as in the previous example. Based on this load current variation, the UC's bi-directional converter is controlled so that it maintains a constant dc link voltage. The bi-directional converter connected to the battery is controlled so that the battery supplies the average load demand to the converter output. Whenever the dc link sees a reference voltage greater than 400 V, both converters are controlled to change their operating modes from boost to buck so that braking energy can be recovered into the storage devices. Figures 23 and 24, respectively, show the battery and UC current variations.

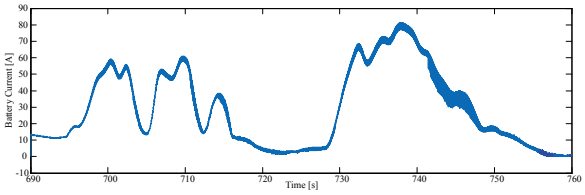

Figure 23: Battery current variation in cascaded converters architecture.

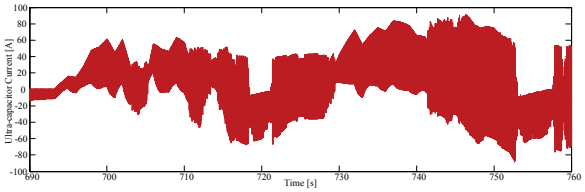

Figure 24: Ultracapacitor current variation in cascaded converters architecture.

From Figs. 23 and 24, the battery current ripples are reduced as a result of the control strategy employed. Moreover, the power contribution is greater compared with the previous architecture because the battery current is actively controlled, allowing it to slowly supply the actual load demands. A benefit of this configuration is that at any time, a limitation can be placed on the maximum allowable battery current to reduce the battery contribution and allow the UC to supply more power to the dc link to maintain the 400 V regulation. In this architecture, the current ripple of the UC is greater than in the simpler passive parallel connection, but since it can successfully supply these current variations without reducing its life span, this is not an issue for the UC.

The SoC variations of the battery and UC are given in Figs. 25 and 26, respectively.

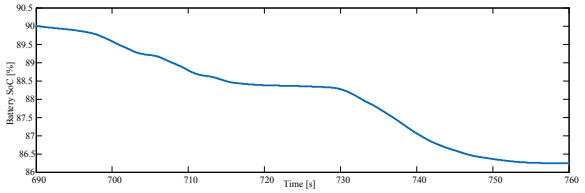

Figure 25: SoC of the battery for cascaded converters architecture.

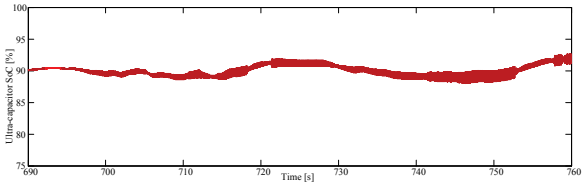

Figure 26: SoC of the UC for cascaded converters architecture.

In this configuration, the battery is used much as in the passive parallel case. Therefore, the SoC usage window for the UC is smaller because it continually receives charge from the battery. On the other hand, since the battery contributes more charge, its SoC decreases more quickly than in the passive parallel configuration.

The dc link voltage variation for the cascaded converters configuration is represented in Fig. 27. As seen in the figure, the dc link voltage varies around the 400 V reference set point. During periods of high power demand and changes in the operation modes of the bi-directional converters, voltage fluctuations become more apparent. For this architecture and control strategy, the dc link voltage reaches a maximum of 405.0 V and a minimum of 395.3 V. Therefore, the maximum amplitude of the voltage fluctuation was calculated as 2.4% over the simulation period.

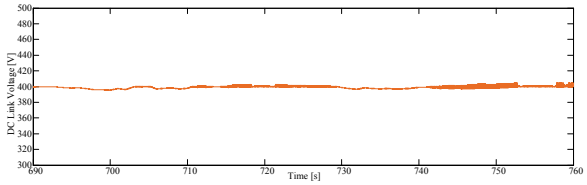

Figure 27: The dc link (load bus) voltage variation for the cascaded converters architecture.

Since this configuration employs an individual dc-dc converter for the battery, it has the built-in flexibility of tuning and manipulating battery current controls. Therefore, a rate limiter and a saturation limiter can be implemented within the battery current control loop: the rate limiter will limit the slope of the battery reference current, while the saturation limiter will limit the battery current magnitude. The implementation of rate and saturation limiters into the battery controller is shown in Fig. 28.

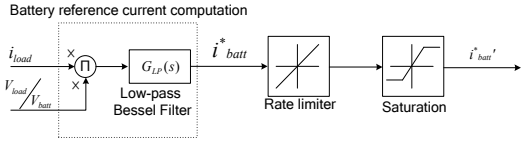

Figure 28: Battery reference current control modification manipulation.

The rate limiter applied in this work has a rising slew rate of +0.1 and a falling slew rate of –0.1 placed on the rising and falling rates of the battery current. At the same time, the saturation block limits the maximum battery reference current by +50 A and negative battery reference current by –50 A to ensure the further reduction of battery stress and maximum battery charge and discharge current. In this case, the current variations of the battery and UC are recorded as shown in Figs. 29 and 30.

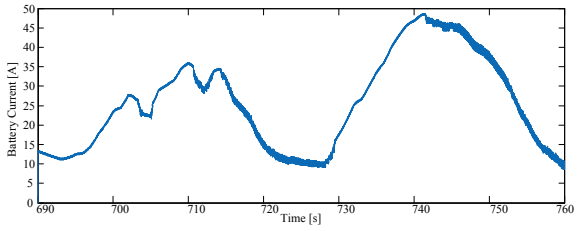

Figure 29: Battery current variation with modified controls.

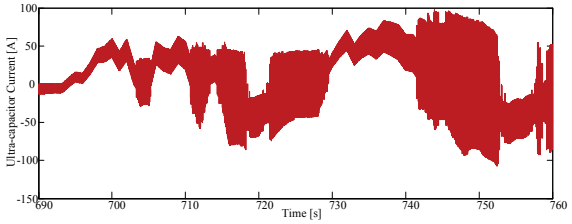

Figure 30: Ultracapacitor current variation with modified controls of battery.

The battery current given in Fig. 29 resulted from implementation of the rate and saturation limiters within the battery current control loop. This modification improves the battery current waveform by eliminating the natural high slew rates of the load current (see Fig. 23 vs. Fig. 29). Moreover, maximum charge and discharge current rates can be defined and battery protection can be realized. In this case, the UC tends to vary faster and with a larger amplitude (see Fig. 24 vs. Fig. 30); but again, the selected UC should be capable of supplying this type of current demand. Since battery usage is reduced and more power is supplied from the UC, the modified current controller affects SoC variations as shown in Figs. 31 and 32.

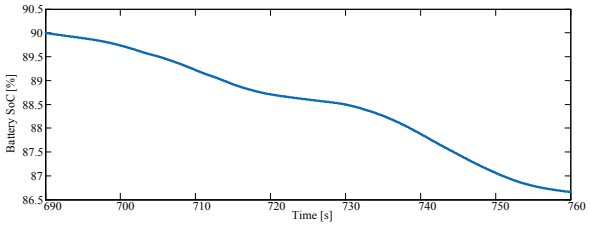

Figure 31: SoC of the battery for cascaded converters architecture with modified controls.

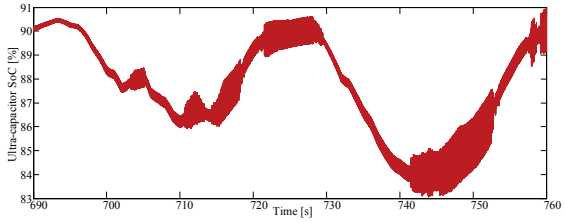

Figure 32: SoC of the ultracapacitor with modified controls of the battery.

Figures 31 and 32 show that the battery SoC remains higher (compare with Fig. 25) whereas the UC SoC drops more drastically (compare with Fig. 26). This occurs because the battery response to power throughput demands is reduced and the UC must deliver more power to the dc link to regulate its voltage during transients.

In any of the architectures discussed, whenever the UC SoC falls below a certain point, the battery controller should bring it back above a certain point while also supplying the load demands. A typical lower limit for the UC can be selected as 20%. Although a deep discharge typically is not a problem for

UCs, such a limitation would prevent an associated dc-dc converter from operating in extreme voltage conversion ratios. Moreover, a fully discharged UC would draw an excessively high current at initial charging if the charge current were not appropriately controlled.

The dc link voltage for this architecture with a modification allowing for current-limiting the battery is presented in Fig. 33. Since the UC supplies more power to maintain a constant dc link voltage, the resulting dc link voltage experiences slightly more voltage ripple than in the previous configurations. The maximum dc link voltage for this simulation was 405.2 V with a minimum of 395.2 V and therefore a max/min ripple percentage of 2.5%.

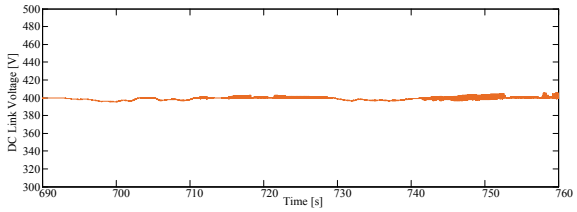

Figure 33: The dc link voltage variation after modified battery current controls.

Simulation and analysis of parallel connected multiple converters configuration

In this configuration, the battery is connected to the dc link through a bi-directional converter and the UC is connected to the same dc link through another bi-directional converter. The battery and UC are therefore connected to the common dc link in parallel through their individual converters. The same drive cycle was used for load modeling over the same time interval as in the previous simulations, the dc link voltage reference was kept the same, and the same strategies were applied for the battery and UC control loops.

The battery and UC current variations are given in Figs. 34 and 35, respectively.

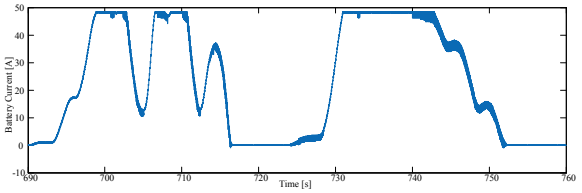

Figure 34: Battery current with parallel converters architecture.

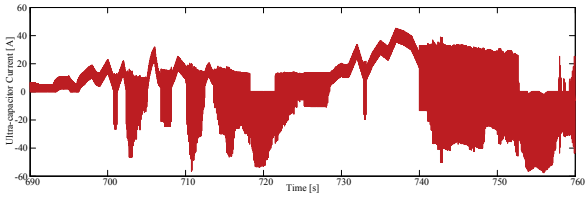

Figure 35: Ultracapacitor current with parallel converters architecture.

Because of the battery current control strategy used and the parallel-connected individual battery dc-dc converter, the battery current was further smoothed with reduced current ripples. Although the battery current was limited to ±50 A, the battery current remained at less than the maximum limit because of the Bessel reference current filter and rising-falling slew rate limiter controller. The only tradeoff for the lower distortion of the battery current is the huge fluctuations with the UC current. However, the UC is capable of supplying these types of current profiles without sacrificing lifetime and performance.

From Figs. 36 and 37, it can be observed that the battery is used less and maintains a higher SoC at the end of the drive cycle. Since the UC makes a greater contribution, another mode of operation could be employed so that the battery recharges the UC whenever the UC SoC drops below a certain lower limit. Figure 38 shows the final result for this architecture, the dc link voltage variation.

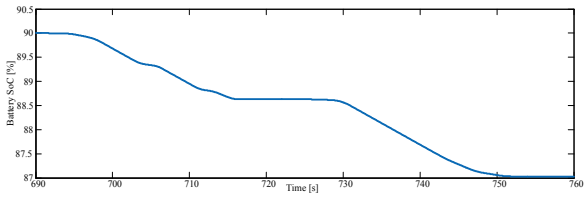

Figure 36: SoC of the battery with parallel converters architecture.

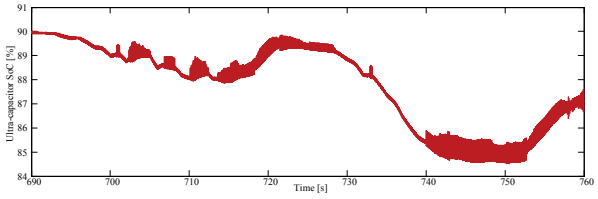

Figure 37: SoC of the ultracapacitor with parallel converters architecture.

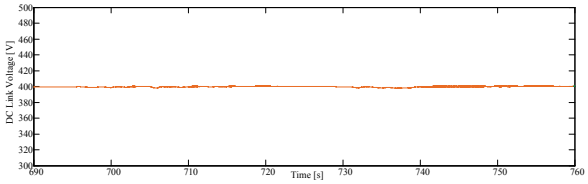

Figure 38: The dc link voltage variation with parallel converters architecture.

Since the UC and its individual parallel converter are both controlled to maintain a constant dc link voltage, the dc link voltage has a much smaller voltage ripple than in previous configurations. It has a maximum of 400.7 V and a minimum of 397.6 V, resulting in a maximum ripple percentage of 0.8%.

Conclusions and Future Directions

Different architectures offering the combined operation of several ESSs were reviewed. Twelve possible hybridization architectures were described for the combined operation of batteries and UCs. The advantages and drawbacks of the passive parallel connection, UC/battery, battery/UC, cascaded converters, parallel converters, multi-input converters, dual-active-bridge converters, dual-source converters, interleaved converters, and switched capacitor converters were highlighted. Although there is no commercially manufactured PEV powered by a battery/UC combination on the market thus far, the hybridization of these energy storage devices has been shown

academically and analytically to be beneficial in terms of battery life, vehicle performance, and fuel economy. However, the hybridization of energy storage devices is a challenging, multi-variable problem requiring appropriate sizing and control of power sharing strategies. Nontraditional forms of ESSs can be promising candidates for PEVs because of their longer lifetimes, higher efficiency, and high specific power and energy densities. Further R&D of these technologies may produce some unforeseen ideal combination of energy density, power availability, efficiency, and ease of implementation in the future when truly high-energy (low-power) RESS electrochemistries are available, such as lithium-air and others.

This project also modeled and simulated three different hybridization architectures and one of the architectures with a modified controller[dmc3]. The analysis results for these four different configurations are consolidated for comparison in Table 1. For some comparison criteria, these architectures were graded on a point scale with 1 indicating the best, 2 indicating better, and 3 indicating average.

Table 3: Comparisons of hybrid energy storage system configurations.

Criteria	PP	CC	CCMC	PC
Control simplicity	1	2	3	3
Structure complexity	1	2	2	2
Number of converters	1	2	2	2
Number of inductors	1	2	2	2
Total inductor mass	2	3	3	2
Number of transducers	5	6	6	6
Cycle-end battery SoC	86.72%	86.24%	86.66%	87.03%
Cycle-end ultracapacitor SoC	89.90%	91.91%	90.45%	87.10%
Maximum battery current ripple	~7 [A]	~9 [A]	~1.7 [A]	~1.8 [A]
Cycle based architectural energy efficiency	95.24%	90.34%	%90.72	%95.25
Maximum dc link voltage variation percentage	2.52%	2.42%	2.51%	0.77%

PP= passive parallel; CC = cascaded converters; CCMC is cascaded converters with modified controls; and PC = parallel converters.

As seen in Table 1, the control system is the simplest for the passive parallel architecture because there is only one converter current to be regulated. Control of the cascaded converters is more complex because there are two converter currents to be controlled, and the addition of current and slew rate limiters into the cascaded converters controller is obviously more complicated still. Parallel converters have a similarly high level of complexity but with a bit more freedom in control of current magnitude and direction.

The passive parallel configuration has the most basic structure. The other converters have a similar level of structure complexity, as they have a larger number of converters and therefore switches, inductors, bus bars, and so on. The total inductor mass of the passive parallel architecture and of the cascaded converters architecture is higher than that of the parallel converters architecture. In the passive parallel case, 100% of the UC and battery current must pass through a single inductor, requiring inductor wiring with a high current rating. In the cascaded converter architecture, the battery converter carries only the battery current, but the UC converter carries the sum of both the battery and UC current. Although the parallel converters configuration requires two inductors, they are relatively smaller than the inductors in the other architectures because each converter carries the current of one source, not two.

If the architectures are compared in terms of end-of-cycle battery SoC, the parallel converters case is superior because of the battery current profile. However, the UC is used more in this case, which results in less end-of-cycle SoC. In the cascaded converters case, the battery sustainably recharges the UC; i.e., the battery power is transferred to the UC continually. Therefore, the UC's end-of-cycle SoC is greater. The highest battery current ripple occurs in either the cascaded converter or the passive parallel converters architecture because they do not effectively control and limit the battery current. The cascaded converters with manipulated controls and the parallel converters inherently provide fewer battery current ripples and therefore prolong battery life.

The cycle-based energy efficiencies are calculated by numerically integrating the battery power, UC power, and load power over the drive cycle to obtain the total energy flow from each source to the load. Once the energy levels are obtained, the output energy and input energy relationship defines the cycle-based efficiency. In this case, the cascaded converter architecture was the least efficient because there are two cascaded converters and one of them should carry all of the current (again, battery current must pass through two converters). In the passive parallel case, there is only one converter, which improves the efficiency. But the most efficient architecture is that of the parallel converters, since each energy storage device has its own converter, and power from a single device never has to pass through multiple converters. The parallel converters architecture is also the best in terms of dc link voltage variation because one of the converters is always used to independently regulate the dc link voltage.

FY 2013 Publications/Presentations

1. O. C. Onar, J. Kobayashi, and A. Khaligh, "A fully directional universal power electronic inverter face for EV, HEV, and PHEV applications," *IEEE Transactions on Power Electronics* **28**(12), 5489–5498, September 2013.

4.1 Traction Drive Electric Motor Development

John M. Miller (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 2012
Projected End Date: September 2013

Objectives: Overall

- Develop efficient, low-cost non–RE electric motors that take advantage of lower-loss materials enabled by new processing methods.
- Meet DOE 2020 cost and performance targets for electric motors.

Objectives: FY 2013

- Develop candidate non-RE, motor (induction and switched reluctance, and eventually synchronous reluctance) designs suited to 55 kW peak, 30 kW continuous power.
- Deliver electrical models to APEEM TDS team for computer simulation and performance validation.
- Employ material and process innovations that facilitate meeting DOE 2020 motor efficiency goal.

Technical Barriers

Cost is an overarching concern for electric traction motors. Traction motors for PEVs are on an approximate 3.5% progress curve and their attendant PE on an approximate 7% progress curve. This means that the DOE 2020 TDS cost target of $8/kW will not be met until 2028 or later unless revolutionary changes occur. Furthermore, instability in RE magnet pricing will continue to pace future cost reductions. There is also a pressing need for a consistent definition of efficiency.

Technical Targets

- Improve system efficiency above the DOE 2020 target of 94% for the TDS. Efficiency computations rely on a harmonic average of motor line efficiency at 20% rated torque from 10 to 100% speed.

Accomplishments

- Completed identification of motor R&D candidates.
- Completed comparisons based on DOE 2020 targets for specific power, power density, specific cost, and efficiency (as defined in Technical Targets).
  - Candidate designs include the IM, switched reluctance motor (SRM), and eventually synchronous reluctance motor.
  - Package-efficient (i.e., smaller) motor designs are more challenging thermally. This challenge prompted closer collaboration with the NREL, which was achieved in the complementary task 1.2.
- Developed a more package-efficient traction motor that analysis shows can meet DOE 2020 targets:
  - minimizes material content
  - benefits from low-loss, affordable electrical steels
  - promotes operation at higher continuous power using improved thermal management materials
- Completed mass and cost calculations that show the selected, and commercially available, baseline IPM traction motor will be challenged to meet DOE 2020 targets because
  - RE magnets are a small fraction of the total mass but a very large fraction of cost.
  - IPM designs are close to or at their rotor structural stress limits; therefore, moving to much higher speeds will be challenging.
- Achieved success in a new process for low-loss, potentially cost-effective electrical steel that is suitable for high-volume manufacturing.
  - In FY 2012, this project validated the performance benefits of low-loss electrical steel and demonstrated, in static testing, substantial improvement in core loss reduction in the baseline IPM test motor (temperature rise at the same operating point was 22°C lower than in the comparator).
  - Subsequent dynamic testing of the same IPM stators in FY 2013 validated earlier findings and showed core loss was reduced by 86% for commercial high-Si steel at a 7000 rpm test condition (speed at which the resultant electrical frequency matches that of the earlier static tests).
  - The new metallurgical process for 6.5% Si steel (Fe 6.5 wt. % Si-500 ppmB) with trace amounts of boron was successfully demonstrated at ORNL using successive strain softening during warm deformation (first reported by Fu et al. [1]) that leads to ease of cold formation, i.e., rolling into thin sheets.

- Completed the design of a high-speed IM that analysis shows can meet DOE 2020 targets for performance and cost. Efficiency will be challenging and requires the use of low-loss steel.

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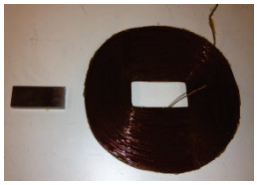
Introduction

The DOE VTO APEEM program has the charter to develop alternatives to RE PM motors. Alternatives to RE magnets, such as enhanced Alnico, are being developed at Ames Laboratory under the aegis of the Beyond Rare Earth Magnets (BREM) program for application to automotive traction motors and other industrial and commercial motors. The ORNL PEEM group supports the VTO APEEM mission through electric motor research on non-PM motors that lessen dependence on critical materials, specifically dysprosium (Dy) and neodymium (Nd). To facilitate the quest for alternatives to non-PM traction motors, this project explores in considerable depth the application of novel materials and their processing as enablers for better performance, efficiency, and cost. This report summarizes APEEM electric motor research for FY 2013 with emphasis on high-speed IM and SRM candidates. Both IM and SRM designs require very low-loss electrical steels to minimize core heat generation and higher thermal conductivity (TC) coating and potting materials that facilitate more rapid heat removal. Low-loss lamination electrical steel and coatings are essential because the absence of RE magnets means that the motor core and working air gap(s) may be magnetized only by an externally applied magnetizing current, either as a component of the stator current in the case of an IM, or phase current injection in the case of the SRM. Figure 1 highlights the mass and volume challenges of replacing the magnetizing strength of a typical RE magnet with that of a current-carrying Cu coil. In Fig. 1 the NdFeB+Dy magnet (N35SH) has a nominal coercivity of 15.4 kOe (1.22×10^6 A/m) and a length of 7.163 mm for an equivalent strength of 8800A. A Cu wire bobbin having the same face areas as the magnet is wound with 1,760 turns of #22 AWG magnet wire. When the Cu bobbin is excited with a 5 A current (15.3 A/mm^2), an equivalent 8800A strength is realized.

The purpose of Fig.1 is to quantify the challenge this project faces when it comes to non-RE alternative motor architectures. The challenge is very significant, including the attendant heat removal burden that injection of external magnetizing current has on the motor's thermal management system. The coil, for example, requires a 100 V_{dc} supply to drive 5 A of excitation current with an attendant 500 W of heat dissipation and rapid temperature rise. The Fig. 1 inset (1) defines an equivalent current sheet for the coil, since this current is spread over an approximately 50 mm quasi-annular region. Above this current sheet (the coil), an expected flux density (2), B(z=0)=110 mT, is in fair agreement with the measured flux density over the coil window. Similarly, taking the coil as an equivalent magnetic dipole moment (3), m, and calculating the flux density at z=100 mm above the coil window area shows fair agreement with measured data. The discrepancy can be accounted for by noting the coil is not an infinite current sheet (2), and in (4), z>>a is necessary to satisfy the dipole moment field, which is not the case here.



Magnet dimensions: L49.35xW17.88xH7.163 mm
Coil dimensions: OD150xH15.9 mm

	Magnet	Coil	Units
Core area	882	882	(mm^2)
Mass	52	999	(g)
Mmf	8800	8800	(A)
B(z=0)	260	74	(mT)
B(z=100)	1.53	7.8	(mT)

$H_x = \frac{K}{2}\left(A/m\right), where\ K = \frac{8800A}{0.05m}$ (1)

$B_x = \mu_0 H_x = 110\ mT$ (2)

$m = \pi a^2 I = 172.5 Am^2, given\ a = 79mm$ (3)

$B(z = 100mm) = \frac{\mu_0 m}{2\pi d^3} = 3.45\ mm$ (4)

Figure 1: Comparison of NdFeB magnet to copper coil of same magnetomotive force rating.

This illustration of replacing a high-energy PM with a Cu winding puts into perspective why RE magnet traction motors have such high performance metrics. This also illustrates why wound field alternatives to PM motors are challenged in meeting specific power and power density.

Approach

- Develop performance and cost assessment for candidate electric traction motors.
- Use the 2012 NISSAN LEAF AEV traction motor as the baseline IPM motor comparator.
- Present analysis to show present traction motor, PE, and TDS will not meet the 2020 target until ~2028 (given 2010 metric initial conditions).
- Project RE-based motor designs out to higher speeds, using optimized RE content at ~$77/kgRE, to show that potential benefits of higher speed are lost when RE content dominates motor cost.

Results

This project includes four experimental test stators that have been fabricated to be as nearly identical as possible to the baseline IPM motor, a 2010 Prius hybrid 60 kW peak power design.

A. Experimental IPM stator thermal and magnetic material characterization

Figure 2a shows the comparison stators that were static tested in FY 2012 with a laboratory 3-phase ac source set at 60V_{rms} line to neutral, and subsequently dynamic tested in FY 2013 using the commercial transaxle case as a dynamometer fixture for FY 2013 characterization work.

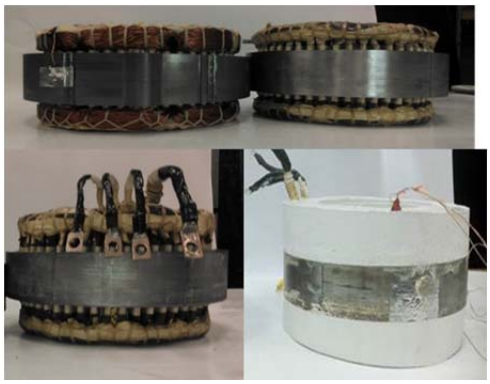


Figure 2a: Comparison stators for static testing at 3-phase, 400 Hz excitation (top: 29M19C5 and 10JNEX900; bottom: 2010 Prius and potted M19 cores).

Figure 2b shows the resultant temperature rise at the applied excitation (~22 A_{rms} line current) for the winding end turns at steady state (20,000 s), relative to the Prius baseline stator, was –7.24°C for the 29M19C5 core, –18°C for the 10JNEX900 Super Core™, and –22.6°C for the potted M19 core. Note also that the core with Cotronics epoxy molding compound (EMC) having a TC of 3.2 W/mK registers a lower temperature at 20,000 s because of the higher thermal mass.

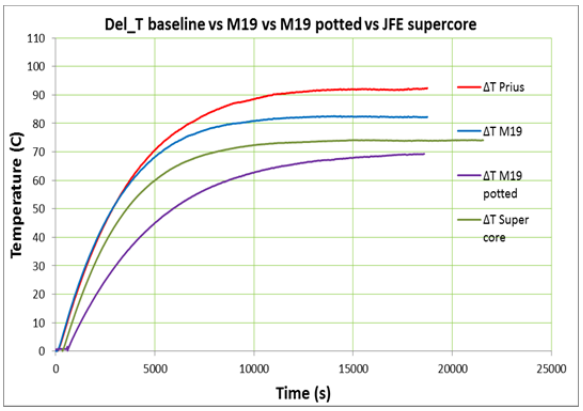


Figure 2b: Chart shows resultant experimental temperature rise data.

Figure 3 is a compilation of core loss comparisons of the M19 and 10JNEX900 cores with the production Prius stator. These are all 48-slot, 8-pole, 3-phase IPMs, so testing at 6,000 rpm results in 400 Hz ac phase voltages that increase to 467 Hz at 7000 rpm. The shaft torque necessary to spin the JFE Super Core 10JNEX900 high-Si steel is virtually identical to spin power for an inert rotor (diamonds).

Characterization testing performed on the experimental stators does confirm that the phase resistance, ac resistance, and back electromotive force (bemf) are virtually identical, as expected. However, the short circuit current and d-axis phase inductance are somewhat different compared with the baseline Prius stator, even though the windings are as uniform as is possible. Figure 4 compares the expected change in phase resistance for the NIH (number in hand) 12 of #20 AWG, N_c=11 turn coil from its dc value to operation at 400 Hz and maximum of 900 Hz when rotating at 13,500 rpm. From short circuit testing of the experimental stators, the d-axis inductance values compute to L_{ds}(Prius)=1.74 mH; L_{ds} (M19)= 1.91 mH; L_{ds}(Super Core)=1.96 mH. The error source is most likely the speed signal, since the magnet flux linkage given in Fig. 4 is virtually identical (i.e., 0.7% error).

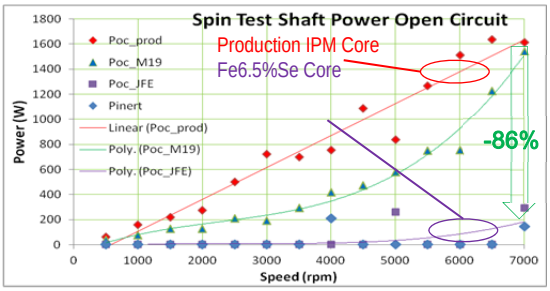
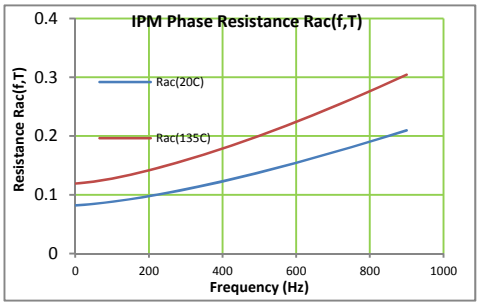


Figure 3: Test fixture for prototype stator spin testing (top). Comparison of experimental phase voltages (bottom).



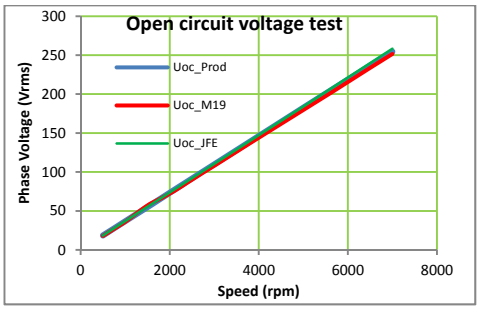


Figure 4: Prototype IPM stator characterization data. Top: dc phase resistance R_{ph}(mΩ) Prius 80.3; M19 82.9; Super Core 83.5 and R_{ac} plot at 20°C and 135°C. Bottom: stator bemf test data in V_{rms}/phase (lambda=0.1287; 0.127; 0.1296 Wb, same order).

B. New processing method for Fe 6.5 wt. % Si-500 ppmB electrical steel

Commercial 6.5% Si steel processed by chemical vapor deposition (CVD) has low loss, as Fig. 3 shows, but is very expensive—on the order of 20 times the cost of M19 steel. ORNL has pursued an alternative process based on strain softening during warm deformation (first reported by Fu et al. [1]) that effectively destroys lattice ordering (B2 phase), leading to restoration of ductility and subsequent ease of cold formability. This process leads to low-cost Fe-6.5%Si steel sheet for motor laminations with equal or better magnetic properties compared with the CVD processed steel. Scaleup and commercialization of the process is important to industry and motor manufacturing because of the major beneficial impact. More development is needed, specifically in the optimization of boron content and thermomechanical process parameters. ORNL is exploring superimposed ultrasonic vibration during deformation to eliminate the need for warm rolling (Fig. 5). Other researchers are doing so, also. [2,3].

With the recent addition of a Walker scientific hysteresis graph, the APEEM group has a facility to characterize lamination steel before embarking on the fabrication of experimental electric machines. In prior electric machine fabrication, a significant difference was observed between prototype results and computer modeling and simulation based on the manufacturer's steel characteristics or model library parameters. Procedures for lamination steel characterization are well documented [4–13] and available to guide APEEM group characterization work. These characterization procedures will be applied to any lamination stock that is processed by strain softening at ORNL.

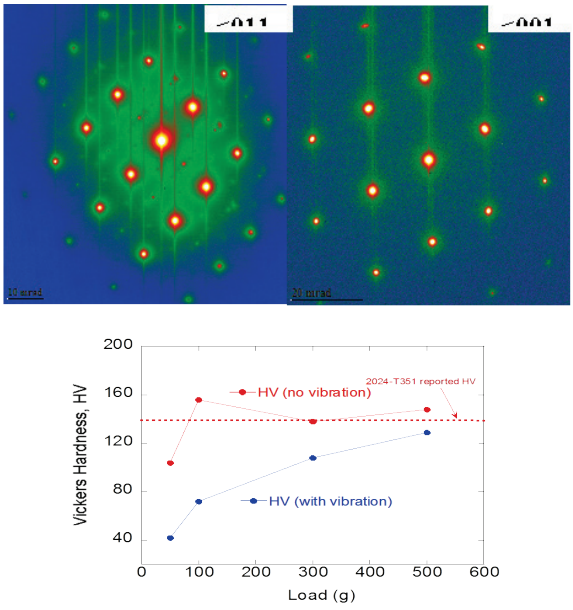


Figure 5: ORNL testing confirms prior work [1] and now extends it with trace boron and ultrasonic vibration. Top: superlattice observed <011> BCC and after 44% deformation superlattice eliminated <001> BCC. Bottom: illustration of ultrasonic vibration during strain softening to reduce hardness.

To determine the full benefit of 6.5% Si steel processed by strain softening, it is necessary to continue this work in FY 2014. In particular, it is necessary to accomplish the following:

- Optimize the boron content for maximizing room-temperature ductility without impacting magnetic properties. This may prove challenging because boron has low solubility in iron and tends to entrain into grain boundaries, which may limit ductility reduction.
- Demonstrate formation into thin sheets by cold rolling in size ranges sufficient for traction motors (e.g., 0.20 to 0.35 mm).
- Conduct analytical modeling and simulation to better understand the effect of boron on the stability of ordered precipitates (B2 phase) and the acoustic plasticity in B2 and DO3 ordered Fe-Si domains. ORNL will employ ultrasonic vibration to aide boron solubility.
- Validate the processed sheet magnetic properties as described.

C. Thermal coating materials

Industrial and automotive electric machines use 0.25 mm thick aramid paper as a slot liner in the stators to prevent contact between magnet wires and the slot walls and core edges. Aramid paper has a TC of 0.05—0.1W/mK. In this project, certain EMCs have been explored for application in electric machines, including processing and application methods such as an electrostatic powder coating process (for conformal coating stator slots) and thermally setting the material in place. Heating converts the deposited powder to a continuous thin EMC coating that has 0.7 < TC < 0.8 W/mK. The 3M paper used in prior project work had a TC of 0.2 W/mK. It is anticipated that powder coating the stators to replace the slot liner paper should increase the TC of the winding bundle to the stator core by some 300%, substantially improving heat transfer. Figure 6 shows one of several 60° segments cut from an experimental 29M19C5 core described earlier but stacked to only 25 mm. The photo in the upper right shows a stator segment that was heated to 200°C for 1 h and then sprayed with SolEpoxy DK15-0984. This process was found to result in a nonuniform, "orange peel" appearance. It was rejected and the coating changed to a 2905-102B material following the same process. The final coating method consisted of the same preheat schedule followed by dipping into a fluidized bed of SolEpoxy DK15-0984 material and then curing at 200°C for 15 min. The fluidized bed process appears viable but may be problematic in thickness control. The sample using the fluidized bed dipping process was wound for high-potential insulation resistance (IR) testing.

The dip-coated stator segment with individually wound coils was tested for high potential by continuous application of 1 kVdc in a thermal chamber with controlled up and down ramp. Figure 7 shows the results of the IR for temperature ramp-up and ramp-down from room temperature to 145°C. An interesting phenomenon occurs at approximately 70°C, where a sharp transition in IR occurs having approximately 2 orders of magnitude. This test was repeated for Nomex paper-lined slots using the uncoated segment; and very similar IR results were found in the 55 to 70°C range, indicating some Arrhenius behavior (i.e., related to activation energy) in the insulating materials.

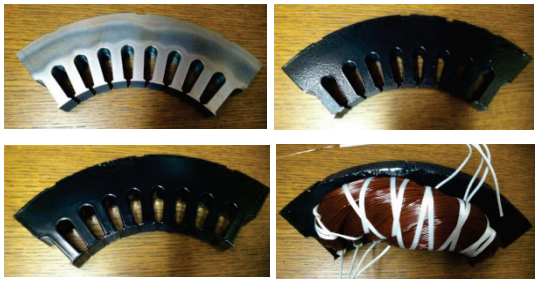


Figure 6: Illustration of stator segment. Top: uncoated core sample (left); coated with SolEpoxy 2905-102B (right). Bottom: preheated segment dipped in fluidized DK15-0984 and lap wound with 19 AWG magnet wire (right).

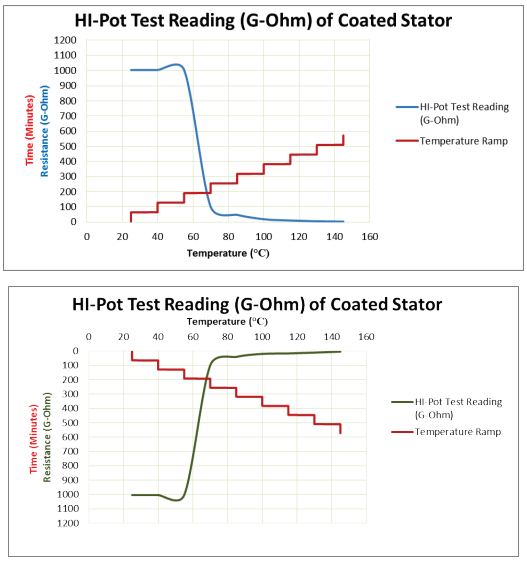


Figure 7: IR test results for coated stator segments during temperature testing. Ramp up (top) and down (bottom).

ORNL quantified the thermal properties of the coating materials described. Figure 8 summarizes the laboratory tests for TC, diffusivity, and heat capacity for both the DK15-0984 and the MgO–loaded 2905-102B materials that confirm TC in the expected range. Based on the densities (i.e., 2.025 g/cc for the Al_2O_3-filled coating, and 1.934 g/cc for the MgO-filled coating), note that since MgO and Al_2O_3 have similar densities, the volume fraction in the Al_2O_3-filled coating would be higher, so better thermal performance would be expected.

In these characterization tests, the two samples are the (SolEpoxy standard) tabular-alumina-filled coating (DK0984) and the development MgO-filled coating (2905102B). This information is useful because with the quantified thermal diffusivity (lambda) and heat capacity (Cp), the thermal conductivity (kappa) can be calculated as kappa = Cp × density × lambda. The advantage of knowing all the thermal parameters, versus only TC, is that any and all transient and steady-state thermal modeling cases can be considered that use these coatings.

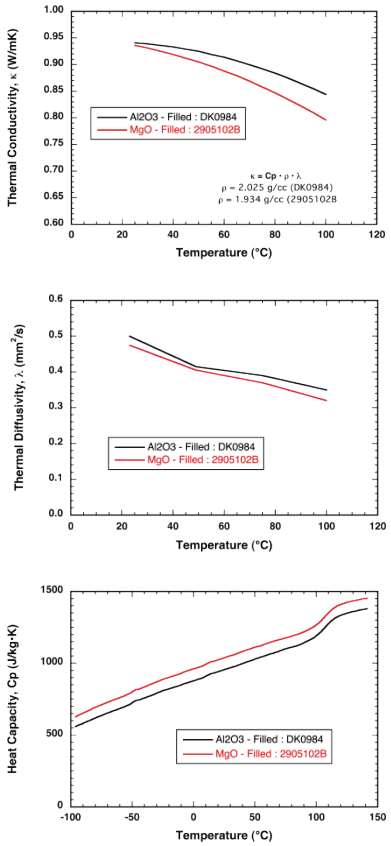


Figure 8: Characterization of thermal coating materials used on stator core samples. Top to bottom: TC, diffusivity, and heat capacity

D. Input requirements for a high-speed induction motor

This project accepts the existing DOE 2020 technical targets for HEVs and concentrates on the design actions required for a non-RE traction motor to meet them, while acknowledging upfront that no electric motor can compete directly against a motor using high-energy magnets, as was illustrated in Fig.1. Therefore, a non-RE traction motor must rely on higher speed to achieve these goals and thereby minimize material content. Higher-speed traction motors may require an additional gear stage to match them with the existing gearboxes of conventional all-electric vehicles. This section discusses the ramifications of adding in-line gearing, such as an epicycle (i.e., planetary, or "rotissmo") stage. It summarizes the highlights of the case for an IM operating at speeds above 14,000 rpm and with a high-conductivity Cu rotor in an effort to meet or exceed DOE's 2020 technical targets.

To meet this aggressive set of goals, a cascade of cost reduction actions must be undertaken in TDS design to reduce the cost from the 2012 metric of $17/kW to the 2020 goal of $8/kW. For electric motors, this means not using RE magnets—because of politically instigated price volatility and future uncertainty, using alternative magnet materials, and using less

material overall. The goal of reducing the total material content can be partially achieved by operating at higher speeds and higher voltages, which are complementary in electric motors. To develop the attendant PE needed to drive a higher-speed motor and achieve these goals requires a similar minimization of material usage, primarily semiconductors. Lower semiconductor content in the traction inverter is realized by operating at higher voltages that lead to a reduced inverter switching current and, consequently, lower motor line current magnitudes. Input requirements are summarized in Table 1 and details of the laminations are shown in Fig. 9.

Table 1: Electric traction motor input requirements

Requirement	Symbol, (Unit)	Target
Peak power at corner speed for 18 seconds and at nominal dc link voltage and temperature representative of prior continuous duty power	P_{pk}, (kW)	55
Continuous power at nominal voltage & temperature	P_{cont}, (kW)	30
Electromagnetic mass (per BOM)	M_{em}, (kg)	<35
Electromagnetic volume (per BOM)	Vol_{em}, (dm^3)	<9.7
Unit cost @ 100,000 APV (annual production volumes)	C, ($)	258
Operating voltage, nominal	U_{d0}, (V_{dc})	720
Maximum operating speed	n_{mx}, (rpm)	>14,000
Ambient temperature outside housing	T_a, (^{0}C)	-40 to +140
Coolant inlet temperature	T_{inlet}, (^{0}C)	
Winding insulation resistance, any phase to stator iron at continuous operating temperature	IR, (MΩ)	>1
Peak ripple torque at any speed and any power	δm_{pk}, (%m_{pk})	<5

BOM = bill of materials based on electromagnetic design content
Electromagnetic torque is "m" for moment and no subscripts for derivations except peak.
Elsewhere in this report "m_x" refers to number for phases, x=1 for stator and 2 for rotor.

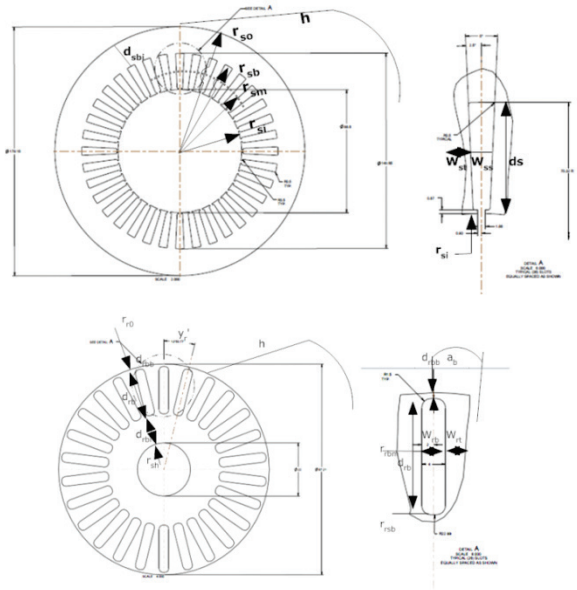


Figure 9: High-speed copper rotor, closed-slot IM. Top: stator lamination design and slot detail; bottom: rotor lamination design and slot detail.

Details of this motor design are provided in an ORNL report (see publications list) and supported by related literature on dealing with frequency effects on windings, especially the Cu bar rotor [11, 14]. Motor parameter evaluations are supported by related literature [15–16] and much of the detailed stator and rotor electrical and magnetic design follows refs [17–19]. The resulting design is a 23,000 rpm motor developed to match the axle torque at 1,600 rpm axle speed. Table 2 lists the full set of motor parameters (see also ORNL/TM-2013/60 in publications list). The parameter values shown in Table 1 are defined by the 4-pole IM equivalent circuit shown as Fig. 10 along with its slip characteristic vs. frequency.

Table 2: Electric traction motor parameter values

n_r	8846	(rpm)		L_m	2.367	(mH)
f_s	295	(Hz)		U_{ll}	485	(V_{rms})
ω_s	1852	(rad/s)		U_s	280.7	(V_{rms})
r_1	87.6	(mΩ)		I_r	-	(A_{rms})
r_2'	36.14	(mΩ)		m_{bd}	196	(Nm)
r_c	-	(Ω)		m_r	59.4	(Nm)
L_{ls}	150.6	(uH)		s_{bd}	0.076	(#)
L_{lr}	114.86	(uH)		s_r	-	(#)

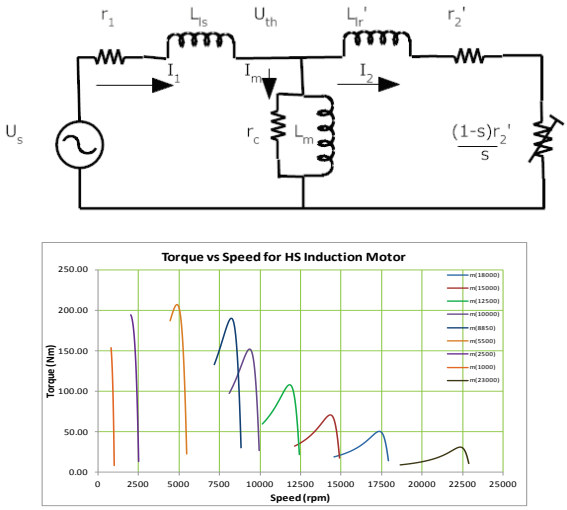
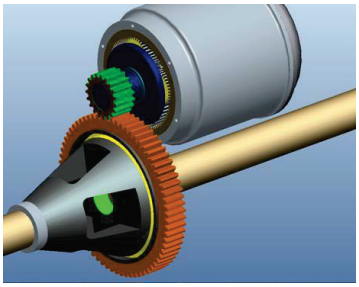


Figure 10: High-speed IM model and matching to vehicle axle using in-line planetary gear. Top: Equivalent circuit model for 4-pole, 3-phase IM. Bottom: Slip characteristics at various speeds

Gear design is based on an in-line planetary shown in Fig. 11 at the motor output shaft end, and the overall reduction ratio is 1.917 in the planetary stage and an additional 7.9:1 in the final drive for a total ratio of 15:1. This effectively translates the IM 59 Nm of rated shaft torque into 885 Nm and 8850 rpm into 590 rpm at the axle. Peak shaft torque is 2.5 times higher, developing 2,200 Nm of axle torque at the same speed, sufficient to meet grade requirements.



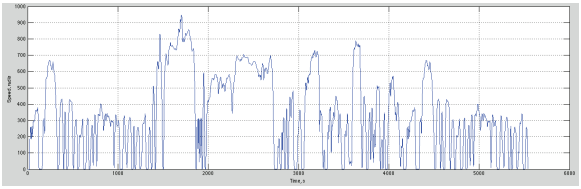
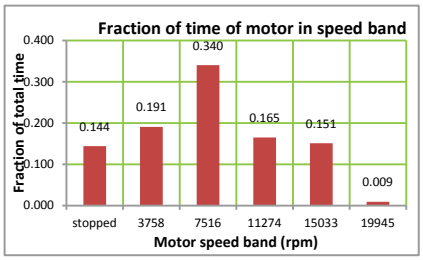
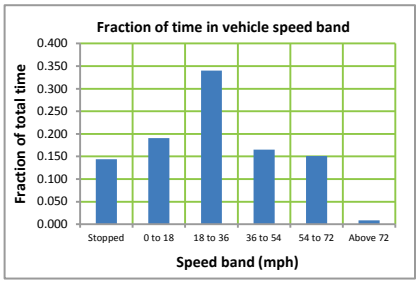


Figure 11: High-speed IM with in-line planetary gear. Top: Architecture of in-line planetary to driven axle. Bottom: Combined drive cycle=UDDS+US06+HWFET+ LA92+UDDS.





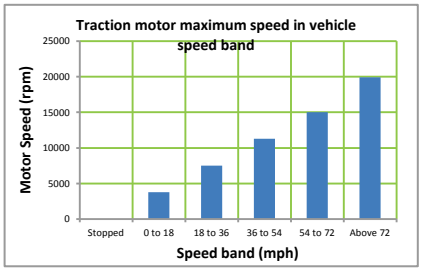


Figure 12: Vehicle application: combined drive cycle schedule results. Top: fraction of total time spent in motor speed band. Center: fraction of time spent in vehicle speed band. Bottom: Maximum traction motor speed by vehicle speed band.

It is evident from Fig. 12 that this high-speed traction motor will spend very little time operating in the band above 15,000 rpm (0.9%), which, mapped to vehicle speed, is in the region above 72 mph. The bulk of operation is in the 3,758 to 15,033 rpm range, 84.7%, and 14.4% stopped. This bodes well for the in-line planetary gear lubrication and gear teeth meshing velocity.

Conclusions

High-speed traction motors are the subject of considerable debate in automotive circles, even though traction motor speeds in both hybrid and battery electric vehicles have steadily increased over the past two decades. It is well known that a low-speed, high-torque traction motor requires low values of gear ratio to match vehicle propulsion needs. At the same time, it is recognized that an electric motor of equivalent power operating at 40,000 rpm for intermittent boosting duty in race cars requires very low torque but high gear ratios. The conundrum is determining where between these two extremes in motor speed is the optimum. This project was designed to explore that space and to identify R&D gaps in motor technology. It is also well established that more compact electric machines have a much more demanding thermal management burden. To mitigate the thermal challenge, this project researched the use of lower-loss mild steel for laminations and higher-TC coating and potting materials. The benefits have been quantified and show 86% lower core loss with 6.5% Si steel and over 300% better TC with MgO-loaded epoxy matrix coatings. Table 3 summarizes the performance metrics of electric motors typical of industrial applications, automotive traction, and racing. The distinction between these application classes is motor speed.

Table 3: Electric motor comparison by speed

Vendor	Motor Type	Mass (kg)	Peak Power (kW)	Speed (rpm)	SP (kW/kg)
Baldor	IM	238	75	1800	0.315
NISSAN	IPM	56	80	10,300	1.43
MTS	SPM	4.0	60	40,000	15

In Table 3, SPM is a surface PM design suited to high speed and ease of control. This project was motivated by the fact that the optimal specific cost ($/kW) and, by the same token, the specific power and power density of electric traction motors for PEVs remain largely unknown. Figure 13 puts this into perspective by noting the major contributors to specific cost—electromagnetic materials and the bearings and gears needed to match commercial gearboxes.

Industrial motors are designed to operate continuously for 20 years at rated power, and at a peak power 2.5 times the continuous power for short periods. EV traction motors are designed to operate intermittently for 7,500 h (13.3 year life of vehicle) and have rated power equal to their peak design power. Racing applications, such as kinetic energy recovery systems, are designed for the highest possible specific power. This project recognizes that reduction of heat generation, rapid heat removal, and adequate thermal management are on the path to the optimized electric traction motor.

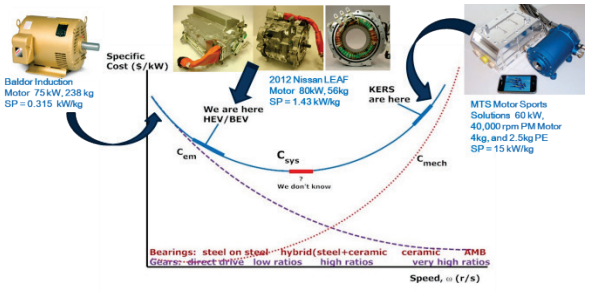


Figure 13: Electromagnetic and mechanical contributors to finding the optimal specific cost of electric traction motors

Future Directions

- Continue design iteration on the high-speed IM stator design, specifically stator slot geometry, and update bill of materials mass and cost breakdown.
- Exercise the same IPM stators fabricated with different materials under PE inverter excitation and compare the core loss results with static and dynamic test results.
- Share the updated IM model parameters with the TDS simulation leader for validation over drive cycles. Share loss data with NREL colleagues for assistance on thermal design and request feedback regarding any concerns relevant to optimizing the motor design.
- Continue design iteration on the SRM and scale it to AEV power levels.
- Proceed into the next phase of Fe 6.5 wt. % Si+B low-loss lamination material and optimize the boron content for the best warm deformation processing, which includes the use of ultrasonic vibration during alloy processing and elimination of ordering phases [20].
- Coordinate the development of a next-generation traction inverter based on WBG semiconductor materials that best match motor designs.
- Perform TDS simulation of motor designs in an AEV simulation environment over combined drive cycles (e.g., UDDS+HWFET+US06+LA92+UDDS) and compare the resulting TDS efficiency with an IPM comparator.
- Address critical assumptions and issues found during FY 2013 program execution.
- Address the cost of currently available low-loss steels, such as JFE Corp. SuperCore™ 10JNEX900 (Fe 6.5% Si):
  - Develop a cost model for the new metallurgical process and compare it with commercial 29M19C5 grade steel.
  - Identify a commercialization partner and initiate technology transfer.
- Seek EMCs with higher TC, 2<TC<5, to promote more rapid heat removal from the traction motor core and windings.
  - Powder-coated cores must meet thermal cycling demands and retain electrical insulation properties in addition to high TC.
  - Consider such high TC EMCs as coating alternatives in higher-temperature motor wires.

FY 2013 Publications/Presentations

1. B. Radhakrishnan, A. Shyam, C. M. Parish, and J. M. Miller, "Development of Fe 6.5% Si-B steels for motor core laminations," presented to DOE VTO propulsion materials program manager Jerry Gibbs, August 21, 2013.
2. R. Wiles, A. Wereszczak, C. Ayers, and J. M. Miller, *Powder Coating Motor Stators with Epoxy Molding Compounds (EMCs) to Eliminate Aramid Paper and Increase the Thermal Conductivity of the Winding Slots*, ORNL/TM-2013/44895, August 2013.
3. John M. Miller, "Game changing technologies in power conversion for electrification of vehicles (air, sea, ground)," panel presentation to IEEE International Transportation Electrification Conference, ITEC2013, Adoba Hotel, Dearborn, MI, June 17, 2013.
4. J. M. Miller, C. Ayers, B. Ozpineci, A. Wereszczak, and R. Wiles, *Design and Development of an Asynchronous Traction Motor to Meet DOE 2020 Targets*, ORNL/TM-2013/60, March 2013.
5. J. M. Miller, "Plug-in electric vehicle (PEV) traction motor and traction drive systems," IEEE Industry Applications Society Distinguished Lecture, Dayton PEAL Chapter, University of Dayton Research Institute, March 27, 2013.
6. J.M. Miller, "Tutorial on traction drive system, power electronics and electric motors," presented at DOE Headquarters to Vehicle Technology Program APEEM sponsor and US DRIVE leads, January 17, 2013.
7. J.M. Miller, "Electric traction motors and EV Everywhere initiative," presented at BREM-VII Workshop, Ames Laboratory, Ames, IA, October 30, 2012.
8. J. M. Miller and R. L. Smith, *Vehicle Performance Metrics Applied to Electric Drive Vehicle System Research—Interim Report*, ORNL/TM-2012/305, September 2012.
9. R. Kisner, A. Melin, T. Burress, D. Fugate, D. Holcomb, J. Wilgen, J. M. Miller, D. Wilson, and F. Peretz, *Embedded Sensors and Controls to Improve Component Performance and Reliability: Conceptual Design Report*, published at www.osti.gov/servlets/purl/1056391/ and ORNL/TM-2012/433, September 2012.
10. J. M. Miller, Traction Drive System breakout session (facilitator) for EV Everywhere Chicago Workshop, July 24, 2012.
11. John M. Miller, "Alnico and ferrite hybrid excitation electric machines," APE043, US DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, Crystal City, VA, May 15–17, 2012.
12. John M. Miller, "Motor packaging with consideration of electromagnetic and material characteristics," APE035, US DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, Crystal City, VA, May 15–17, 2012
13. John M. Miller, "Alnico and ferrite excitation electric machines," Electrical and Electronics Technical Team, US Council for Automotive Research, Southfield, MI, April 26, 2012

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FY 2013 Patents/Disclosures

1. B. Radhakrishnan, J. M. Miller, A. Shyam, and C. M. Parish, "Process for Making Fe-6Si Steel Laminations for Electric Motors," IDSA#3160, September 2013.
2. J. M. Miller, C. W. Ayers, and R. H. Wiles, "Cross-field Weakened Surface Permanent Magnet Generator," application S-124,492, disclosure #20120918, August 2013.

4.2 Electric Motor Architecture R&D

C. W. Ayers (Principal Investigator)

Oak Ridge National Laboratory
National Transportation Research Center
2360 Cherahala Boulevard
Knoxville, TN 37932
Phone: 865-946-1342; Fax: 865-946-1210
Email: ayerscw@ornl.gov

John M. Miller, ORNL Program Manager
Phone: 865-946-1469; Fax: 865-946-1262
Email: millerjm@ornl.gov

Susan A. Rogers, DOE Program Manager
Phone: 202-586-8997; Fax: 202-586-1600
Email: Susan.Rogers@ee.doe.gov

Start Date: October 1, 2012
Projected End Date: September 30, 2013

Objectives

Overall Objectives

- Support overall driveline system modeling (TDS efficiency and cost)
- Design matching driveline components for ORNL concept motors for test bed demonstration
- Provide modeling to validate speed/dynamics capability of ORNL concept motors, including gearing

FY 2013 Objectives

- Study evolution of driveline systems to benchmark industry direction, determine what changes are needed to reach DOE goals
- Provide study results, finite element analysis (FEA) data, and gear design concept(s) to the APEEM team
- Partner with the motor and gearbox industry to produce advanced concept of integrated gear/motor system for ORNL TDS design

Technical Barriers

- Bearing speeds
- Bearing quality and cost needed to meet speed requirements
- High-speed gear design manufacturing methods and cost
- Mass effect of additional gearing on power density

Technical Targets

- Motor (2020 target)
  - Cost: $4.7/kW
  - Specific power: 1.6 kW/kg
- TDS (2020 target)
  - Cost: $ 8/kW
  - Specific power: 1.4 kW/kg

Accomplishments

- Prepared technical assessment report evaluating benchmarked TDSs and selected state-of-the-art starter motors for high-speed operation
  - 2012 Nissan LEAF®, 2004 and 2010 Prius, 2011 Sonata, 2007 Camry, 2008 Lexus
  - 2010 Camry starter, Dixie Electric starter, Denso starter (planetary gears, gear manufacturing)
- Performed FEA modal analyses on several traction drive rotors, benchmarked units and ORNL concept rotors
  - 2012 LEAF
  - 2010 Prius
  - ORNL multiple isolated flux path (MIFP) SRM
  - ORNL outer rotor generator
  - ORNL IM design
- Performed FEA stress and thermal analysis for concept motors
- Designed gearing for ORNL concept motor(s)

✧ ✧ ✧ ✧ ✧

Introduction

Hybrid vehicle traction driveline gearing has evolved over the last decade to match ever-increasing speeds for HEV motors and generators. Auto manufacturers are using increased speed as a means to increase the power density of their electric traction motors in vehicles. ORNL is also pursuing traction motor designs that have much higher maximum rotor speeds, in the range of 15,000–25,000 rpm.

Improved gearing is needed to reduce the higher rotor speeds to match the final drive and wheel speed requirement, which does not change. Speeds for starters and alternators are also increasing in auto designs, so high-speed rotors and gearing for speed reduction are being developed in that automotive area as well. These efforts focus on increasing power density, making motors and generators smaller, reducing or eliminating the need for magnet material, and reducing the overall amount of materials required to produce these products (e.g., Cu, Si, steel). Accomplishments in those areas can reduce the cost of HEVs as well as reduce their weight.

Replacing conventional oversized motors with smaller motors using speed-reduction gearing has inherent design and cost tradeoffs. ORNL benchmarked drives are being examined, gear designs proposed, and gear manufacturers consulted to

develop a concept that supports the ORNL goal of smaller, higher-speed motors. This effort strives to find the best means of matching new higher-speed motors to existing drivelines in the gear trains of automotive traction drives.

No present technology can be extrapolated to meet DOE 2020 targets. Increasing speeds can enable motors to meet the targets.

Approach

- Assess the evolution of traction and starter motors as designs move from conventional to high-speed
- Analyze state-of-the-art rotors and ORNL rotors, conduct FEA modeling of structural stresses and modal behavior and their impact on high-speed operation
  - Rotor bending modes
  - Centrifugal stresses
  - Bearing loads
- Evaluate material limits for high-speed concept motor(s) and compare them with benchmarked commercial traction motor design limits
  - Cu rotor bar stresses
  - Lamination bridge stresses
  - Rotor end-ring retention
- Develop and deliver driveline designs for ORNL TDS high-speed concept motors to the APEEM team

Results

Rotor modal analysis

Four rotors were analyzed and compared for modal response to see how rotor geometry affects design and speed limitations. The 2010 Prius, the 2012 LEAF, the ORNL MIFP 15,000 rpm SRM, and the ORNL 23,000 rpm IM rotors were examined.

A 23,000 rpm version of the ORNL MIFP is currently being developed, and results from that design are shown as well. The rotor diameter will decrease somewhat to the approximate size of the ORNL IM, and the rotor will stretch axially from its present design.

The two rotors shown in Fig. 1 are the commercial rotors that were initially modeled to provide baseline information on these mode shapes. Models of the ORNL concepts were analyzed as the designs progressed.

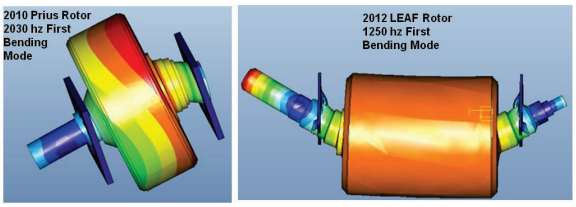

Figure 1: Rotor first bending mode analyses for 2010 Prius and 2012 LEAF.

Figure 2 shows an analysis of the ORNL IM model and the first bending mode of that rotor design.

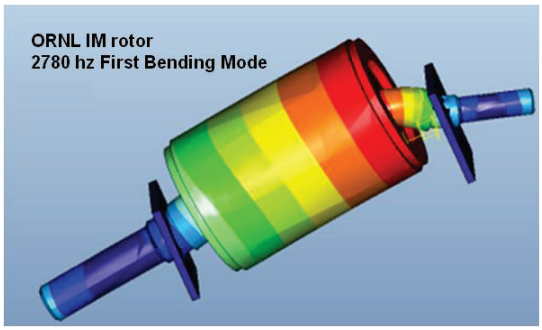

Figure 2: ORNL induction machine (Cu rotor) concept machine modal analysis.

Similar bending mode analyses are shown for the first- and second-generation ORNL MIFP SRMs. The first-generation unit was built and tested in FY 2012 at ORNL. The second-generation unit is under design and analysis for operation at 23,000 rpm, similar to the ORNL IM. Figure 3 shows the results of the modal analyses for those rotors.

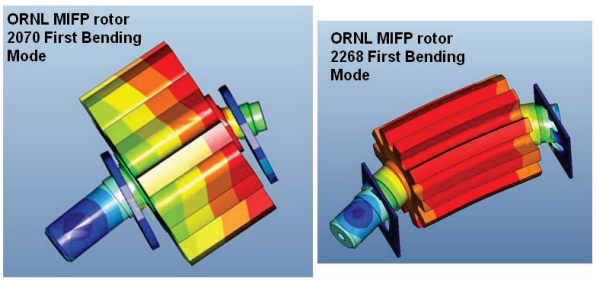

Figure 3: ORNL MIFP SRMs. Left: first-generation prototype (built and tested); right: second-generation prototype rotor (concept).

It was found that all the first bending mode frequencies in these various designs were extremely high compared with operating speeds. The results are tabulated in Table 1.

Table 1: Modal analysis results for several commercial and concept motor rotors

Rotor	Max Operating Speed	First Bending Mode Frequency
2010 Prius	14000 rpm	122000 rpm
2012 LEAF	10400 rpm	75000 rpm
ORNL MIFP	15000 rpm	124000 rpm
ORNL IM	23000 rpm	167000 rpm
ORNL MIFP	23000 rpm	136000 rpm

An important observation based on these analyses is that the first bending resonance of these shafts is not the limiting factor in high-speed capability. The bending modes are all six to eight times higher than the maximum operating frequency. Speed capability is also typically limited by bearing speeds, magnet retention, rotor bar retention, and other factors; so one or more of these factors will be the major contributors to speed limitations, as opposed to magnet or rotor bar retention strength.

Rotor /lamination centrifugal stresses were studied on the ORNL concept motors. These rotors do not have the magnet retention stress problem typically found in common IPM motors. The ORNL MIFP has an extremely simple rotor—stamped laminations with rotor pole radial extensions. This rotor has a speed capability of at least 30,000 rpm based on the lamination stress, as seen in Fig. 4 for the first- and second-generation units.

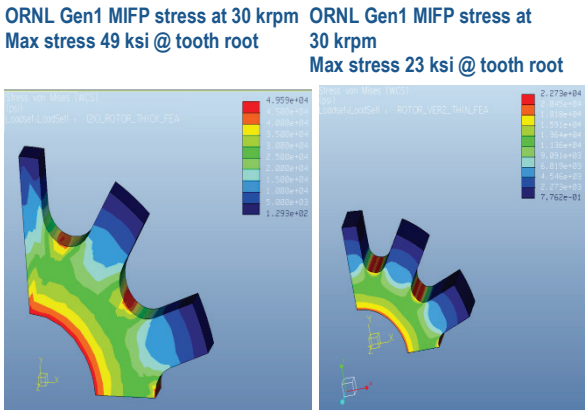

Figure 4: Lamination simulated stresses for the generation 1 and 2 ORNL MIFP SRMs.

The rotor in the ORNL IM is somewhat more complex because of the Cu rotor bars inserted through the laminations. This geometry creates a thin area (bridge) in the outer perimeter of the lamination that is similar to the design of PM rotors. The bridge area is the weak link in this design, and FEA simulations (Fig. 5) show that the stress is highest at the bridge but still acceptable at 23,000 rpm. More information can be obtained for this design in Miller et al. [1].

Figure 5: Lamination bridge stress from copper rotor bar for the ORNL IM concept.

Driveline matching design work

Gear design is key in the matching of the new higher-speed motor to a generic automobile drive train. The high-speed motor concept includes applying an in-line planetary gear set (sun gear, 3–4 planet gears, planet carrier, and ring gear) and matching the ratio of this set to the remaining gears in the drive train. It has been calculated that a total reduction of about 14:1 or 15:1 will be required for a 23,000 rpm motor to match a 1,600 rpm maximum axle speed. A first-cut design completed by MagnaPowertrain uses a planetary reduction of 4.6:1 and a final gear reduction of 3.7:1. This design for the gear system from motor to axle (represented in Figs. 12–15 later in this section) is based primarily on the geometry of the 2007 Toyota Camry.)

Gear losses are related to the power transferred through a gear train. Calculations for gear power and losses were based on data from one of the ORNL concept motors.

Representative torque and power curves for the ORNL IM are shown in Fig. 6. Calculations for gear power and losses are based on these data and can be linearly adjusted based on any final adjustments to this concept motor performance or curves from a similarly designed ORNL concept motor.

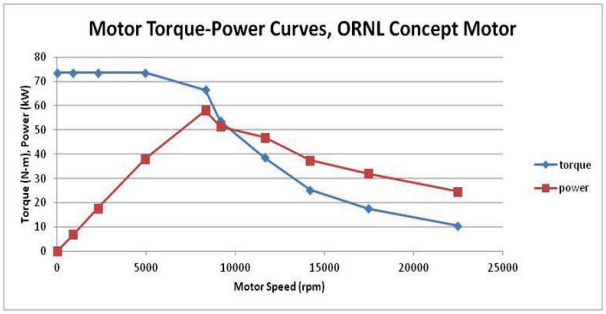

Figure 6: Torque/power vs. speed for an ORNL high-speed concept motor.

In a final design, speed and torque range will be interconnected with shaft sizes and thus with available bearing sizes for a given design choice. The graph in Fig. 7 shows a curve developed from standard bearing inner diameters and the highest speed rating of each size. Overlaid on this graph is another curve based on the torque capability calculation from torsion in the shaft.

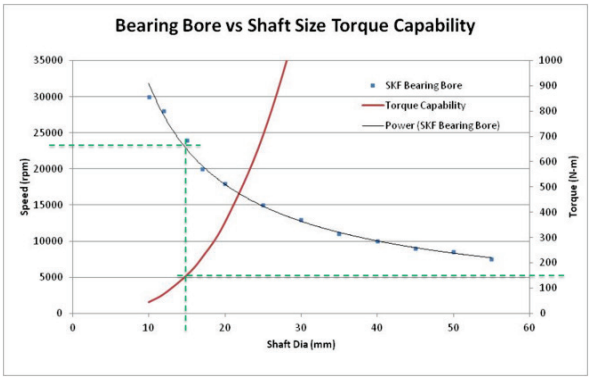

Figure 7: Relationship among bearing bore, shaft size, and torque capability for motors.

Shaft diameter for a given torque is based on the equation

$d^3 = (16 * T) / (\mathrm{Pi} * \tau_{max})$,

where d = shaft diameter

T = shaft torque

τ = shear strength of the material

The material used for the example represented in Fig. 7 was AISI 4340 steel, σ_{yield} = 100,000 psi and τ_{max} = 50,000 psi.

The two curves in Fig. 7 can be used to deduce the torque capability and speed range a particular shaft design can handle. The example shown by the green dashed line is a 23,000 rpm shaft of 15 mm diameter; it can handle about 150 N-m torque. As speed is increased for a given traction motor application, the

torque requirement at the motor output shaft is reduced. This reduction allows the motor shaft size to be reduced, allowing the bearing diameters to decrease and thus increasing the bearing speed range.

To further examine an application for a high-speed concept motor, the gear design and the losses associated with it should be addressed. For high-ratio gear reductions, potential power (apparent power) can be used to determine losses associated with a gear design across the speed range of the system.

Potential power (similar to reactive power in electronic circuits) is based on the product of pitch line force and pitch line velocity for each gear mesh in a gear train (Fig. 8). Losses can simply be estimated by applying a rule-of-thumb loss percentage to the potential power at each individual gear mesh (1% at each gear mesh is a typical number—this can be adjusted based on empirical testing of the actual motor and gear train). The *shape* of the potential power curve (and the loss curves) will be the same as for the motor power curve, but with varying absolute values depending on the nature of the gear mesh for which it is calculated. Figure 9 shows estimated gear losses in watts for each gear mesh in the concept design (based on Fig. 6 data). These data can be used in the system model to see what impacts gear issues have on overall system losses. A related ORNL task is developing models for the overall system using a drive cycle and inputs from the various parts of the TDS. From this task, a couple of inputs for the overall system model can be the gear losses vs. speed, and an estimate of churning losses vs. temperature in the gearbox lubricant.

The ORNL combined drive cycle (CDC) is a close approximation of real world driving. The cycles used are UDDS, HWFET (Highway Fuel Economy Test), US06, and LA92, which are combined in series to form the ORNL CDC. Based on the CDC, calculations were performed to estimate the dwell time for vehicle operation in each of several speed bands. The band stops are 17.9, 35.8, 53.7, and >71.7 mph. Figure 10 shows the time fraction in each band and the maximum speed a traction motor would reach in those bands. Only about 1.2% of time is actually spent above 15,000 rpm in reality, and the vehicle is stopped for around 14% of the time. Most of the time is spent at motor speeds in the 3,500 to 15,000 rpm range.

To get a feel for how gear losses impact the system over a CDC, an overlay was made using the gear loss graph and the speed bands dwell time, seen in Fig. 11. It is interesting to note that the dwell times follow the shapes of the power curves fairly well.

Approximate gear losses can be calculated using potential power methods. Losses are highest for the first (highest-speed) gear mesh at the motor shaft.

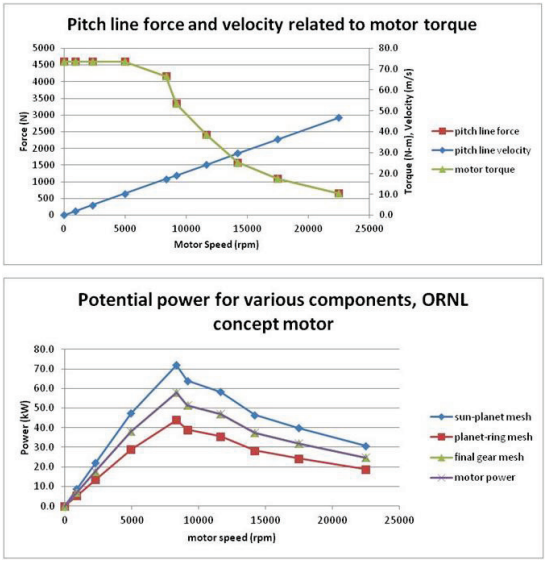

Figure 8: Pitch line force/velocity (upper), potential power for components (lower).

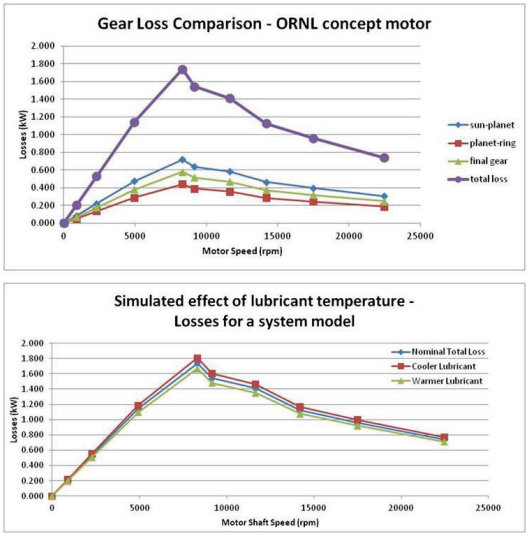

Figure 9: Losses for gear mesh locations (upper) and estimated losses due to lubricant temperature (lower).

A couple of observations can be made from the analysis of gears and the system geometry.

1. Trading a high-speed, high-reduction planetary for some of the existing conventional gears (as seen in the benchmark drives) can be evaluated. It appears to be a good efficiency and cost tradeoff based on findings.
2. It is possible that this new layout (assuming gears/bearings can be removed) could be as efficient as or more efficient than existing designs. The gear diagrams indicate that *two gears, one gear mesh, and at least one bearing* can be removed from a typical system.

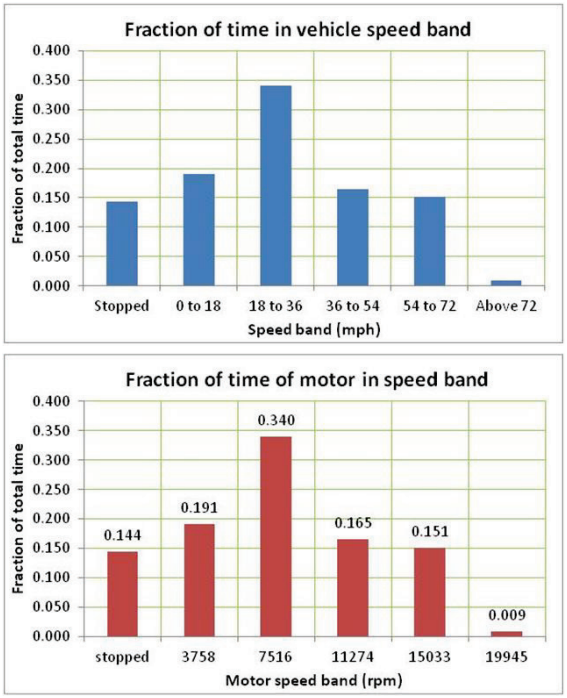

Figure 10: Relative fraction of time a 15:1 ratio traction drive system will spend in different speed bands.

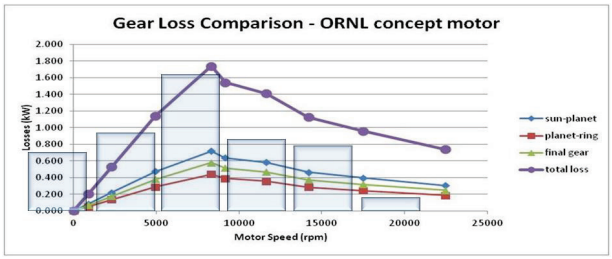

Figure 11: Overlay of dwell time estimates (translucent bars) over the gear loss curves.

Based on observation and study of existing systems, and combining this information with the specifications of the ORNL concept motors, a gearing philosophy was chosen to match the higher-speed motor to existing drivetrain speeds for conventional sedans. An in-line planetary was chosen to mount adjacent to the motor output shaft; it would reduce the speed to a reasonable level to drive a pinion and main drive gear at the vehicle axle differential.

MagnaPowertrain calculations provided a gear set design to ORNL, and the resulting specifications were used to assemble a conceptual design for the drivetrain connecting a 23,000 rpm motor to a 1,600 rpm axle. Figure 12 shows the overall modeled concept of the motor connected to the differential with an axle.

The ORNL concept motor has a higher L/D ratio than those used by today's typical HEV traction drives. This allows the motor to lie in closer proximity to the axle centerline and enables the simpler high-speed driveline.

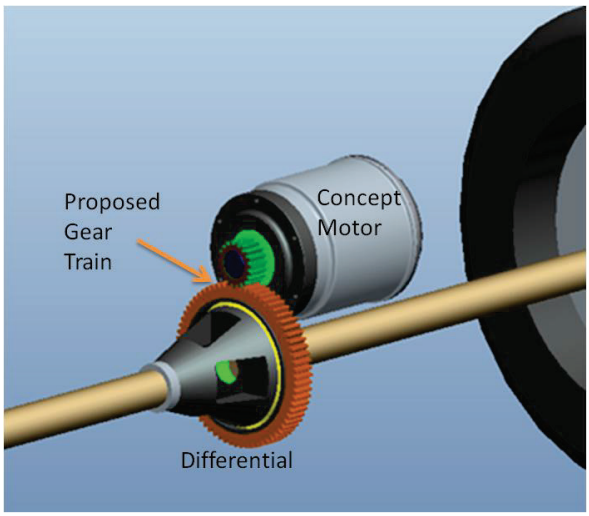

Figure 12: ORNL concept matched driveline, 23,000 rpm motor.

Figure 13 is an exploded view of the concept driveline showing the internal parts and how they assemble to one another. Lubrication and cooling are remaining issues that need to be addressed for this design, and they are part of the next steps as this project continues. This work could be done as an integral part of a housing design that contains the motor, gears, and bearings.

Figures 14 and 15 show additional views giving more detail on the internals of the ORNL driveline concept.

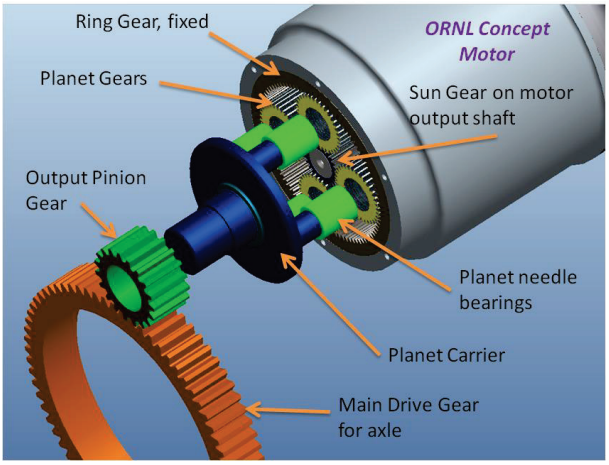

Figure 13: Exploded view of ORNL concept driveline with MagnaPowertrain calculated gears.

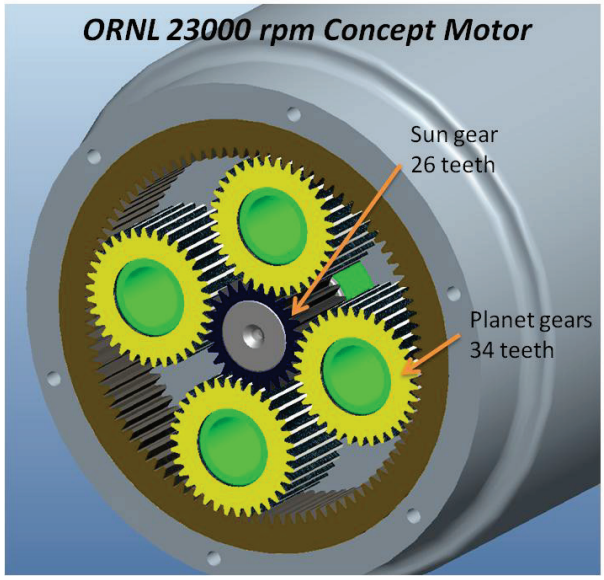

Figure 14: Close-up view of in-line planetary at motor shaft.

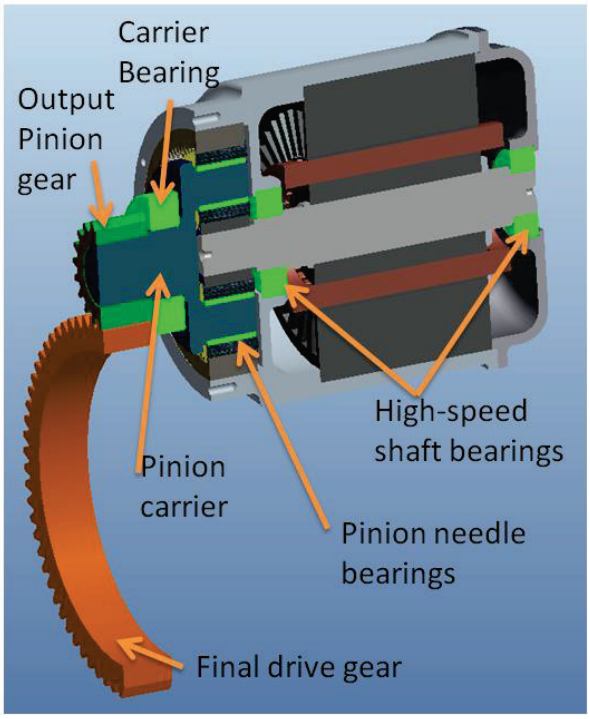

Figure 15: Section view of 23,000 rpm ORNL matched driveline concept.

Earlier in the year, consultations with Regal Beloit yielded interest in our high-speed motor, SRM concepts, and high-speed gearing for the traction drive application. Regal Beloit performed some initial calculations to evaluate the concept and determined that it was achievable with reasonable gear designs. Their calculations, using their gear software, for the in-line planetary gear set to be mounted to the ORNL concept motor are shown in Fig. 16.

KISSSOFT
Calculation programs for machine design

KISSsoft - Release 03-2012F
Milwaukee Gear Division of Regal Beloit Corp

File
Name : 28NDP-4 planet KissSoft fine size
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Important hint: At least one warning has occurred during the calculation:
1-> Transverse contact ratio is < 1 !

2-> Mounting in radial direction at
the assembly is not possible!

3-> Notice concerning gear 1:
Dimension over balls is not measurable (facewidth is too small)!

4-> Notice concerning gear 3:
Dimension over rollers is probably not measurable (facewidth is a bit too short)!

CALCULATION OF A HELICAL PLANETARY GEAR

Drawing or article number:
Gear 1: 0.000.0
Gear 2: 0.000.0
Gear 3: 0.000.0

Calculation method AGMA 2001-D04

		Gear 1	Gear 2	Gear 3
Number of planets	[p]	(1)	3	(1)
Power (hp)	[P]		73.75	
Transmitted power (hp)	[P]		73.75	
Transmitted power (ft*lb/s)	[P]		40562	
Speed (1/min)	[n]	23000.0		0.0
Speed difference for planet bearing calculation (1/min)	[n2]		12197.9	
Speed planet carrier (1/min)	[nSteg]		4344.4	
Torque (ft*lbf)	[T]	16.8	0.0	72.3
Torque Pl.-Carrier (ft*lbf)	[TSteg]		89.158	
Overload factor	[Ko]		1.00	
Power distribution factor	[Kgam]		1.00	
Required service life	[H]		20000.00	
Gear driving (+) / driven (-)		+	-/+	-

Gearbox type: Standard gearing in closed housing

1. TOOTH GEOMETRY AND MATERIAL

(geometry calculation according to ISO 21771:2007)

		Gear 1	Gear 2	Gear 3
Center distance (in, mm)	[a]		1.2000, 30.480	
Centre distance tolerance			ISO 286:2010 Measure js7	
Normal Diametral Pitch (1/in)	[Pnd]		19.00003	
Normal module (in, mm)	[mn]		0.05263, 1.3368	
Pressure angle at normal section (°)	[alfn]		20.0000	
Helix angle at reference circle (°)	[beta]		18.0000	
Number of teeth	[z]	17	26	-73
Facewidth (in)	[b]	0.42	0.42	0.42
Hand of gear		right	left	left
Planetary axles can be placed in regular pitch.:			120°	
Accuracy grade (AGMA 2015)	[Q-AGMA2015-1-A2001]	A6	A6	A6
Inner diameter (in)	[di]	0.00	0.00	
External diameter (in)	[di]			0.00
Inner diameter of gear rim (in)	[dbi]	0.00	0.00	
Outer diameter of gear rim (in)	[dbi]			0.00

Material
Gear 1: 18CrNiMo7-6, Case-carburized steel, case-hardened
ISO 6336-5 Figure 9/10 (MQ), core strength >=25HRC Jominy J=12mm<HRC28
Gear 2: 18CrNiMo7-6, Case-carburized steel, case-hardened
ISO 6336-5 Figure 9/10 (MQ), core strength >=25HRC Jominy J=12mm<HRC28
Gear 3: 18CrNiMo7-6, Case-carburized steel, case-hardened
ISO 6336-5 Figure 9/10 (MQ), core strength >=25HRC Jominy J=12mm<HRC28

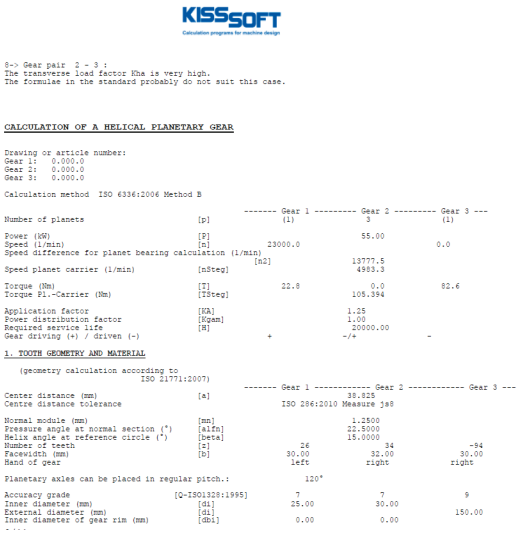
		Gear 1	Gear 2	Gear 3
Surface hardness		HRC 61 (lb/in²), (N/mm²)	HRC 61 (lb/in²), (N/mm²)	HRC 61 (lb/in²), (N/mm²)
Allowable bending stress number	[sat]	62366, 430.0	62366, 430.0	62366, 430.0
Allowable contact stress number	[sac]	217557, 1500.0	217557, 1500.0	217557, 1500.0
Tensile strength (lbf/in²)	[Rm]	174046.02	174046.02	174046.02
Yield point (lbf/in²)	[sigs]	123282.60	123282.60	123282.60
Young's modulus (lbf/in²)	[E]	29877900	29877900	29877900
Poisson's ratio	[ny]	0.300	0.300	0.300
Mean roughness, Ra, tooth flank (mil)	[RAH]	0.02	0.02	0.02
Mean roughness height, Rz, flank (mil)	[RZH]	0.19	0.19	0.19
Mean roughness height, Rz, root (mil)	[RZF]	0.79	0.79	0.79

Tool or reference profile of gear 1 :
Reference profile 1.25 / 0.38 / 1.0 ISO 53.2:1997 Profil A

Figure 16: Gear software calculations from Regal Beloit for ORNL's early in-line planetary concept.

Later in the year, and after more complete designs were developed for the ORNL concept motors, we met with MagnaPowertrain to discuss an overall matched driveline. This company has the capability to manufacture the entire unit from motor to axle, and its representatives expressed interest in working with ORNL to produce a prototype. They provided some effort at no cost to look into the driveline matching and high speed in-line planetary idea for ORNL concept motors. Using a conceptual description of our needed gear system, MagnaPowertrain conducted some preliminary design/calculations for ORNL. Data from its calculations for the design, showing some of the gear information, are shown in Fig. 17. Figures 12–15 are geometrically correct 3-dimensional (3D) models derived from MagnaPowertrain's calculations.

In the effort to look at the entire driveline, MagnaPowertrain looked at the final drive gears in addition to the planetary section (Figs. 12–15). Figure 18 shows the calculations from that work by MagnaPowertrain.



KISSSOFT

8-> Gear pair 2 - 3 :
The transverse load factor Kha is very high.
The formulae in the standard probably do not suit this case.

CALCULATION OF A HELICAL PLANETARY GEAR

Drawing or article number:
Gear 1: 0.000.0
Gear 2: 0.000.0
Gear 3: 0.000.0

Calculation method ISO 6336:2006 Method B

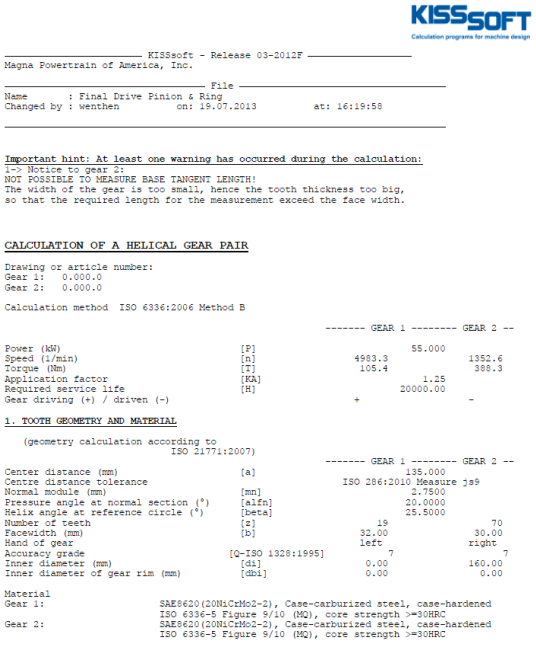
		------- Gear 1 ---------	Gear 2 ---------	Gear 3 ---
Number of planets	[p]	(1)	3	(1)
Power (kW)	[P]		55.00	
Speed (1/min)	[n]	23000.0		0.0
Speed difference for planet bearing calculation (1/min)	[n2]		13777.5	
Speed planet carrier (1/min)	[nSteg]		4983.3	
Torque (Nm)	[T]	22.8	0.0	82.6
Torque Pl.-Carrier (Nm)	[TSteg]		105.394	
Application factor	[KA]		1.25	
Power distribution factor	[Kgam]		1.00	
Required service life	[H]		20000.00	
Gear driving (+) / driven (-)		+	-/+	-

1. TOOTH GEOMETRY AND MATERIAL

(geometry calculation according to ISO 21771:2007)

		------- Gear 1 ----------	Gear 2 ----------	Gear 3 ---
Center distance (mm)	[a]		38.825	
Centre distance tolerance			ISO 286:2010 Measure js8	
Normal module (mm)	[mn]		1.2500	
Pressure angle at normal section (°)	[alfn]		22.5000	
Helix angle at reference circle (°)	[beta]		15.0000	
Number of teeth	[z]	26	34	-94
Facewidth (mm)	[b]	30.00	32.00	30.00
Hand of gear		left	right	right
Planetary axles can be placed in regular pitch.:			120°	
Accuracy grade	[Q-ISO1328:1995]	7	7	9
Inner diameter (mm)	[di]	25.00	30.00	
External diameter (mm)	[di]			150.00
Inner diameter of gear rim (mm)	[dbi]	0.00	0.00	

Figure 17: Gear software calculations from MagnaPowertrain for ORNL's latest in-line planetary concept.



KISSSOFT

KISSsoft - Release 03-2012F
Magna Powertrain of America, Inc.

File
Name : Final Drive Pinion & Ring
Changed by : wenthen on: 19.07.2013 at: 16:19:58

Important hint: At least one warning has occurred during the calculation:
1-> Notice to gear 2:
NOT POSSIBLE TO MEASURE BASE TANGENT LENGTH!
The width of the gear is too small, hence the tooth thickness too big,
so that the required length for the measurement exceed the face width.

CALCULATION OF A HELICAL GEAR PAIR

Drawing or article number:
Gear 1: 0.000.0
Gear 2: 0.000.0

Calculation method ISO 6336:2006 Method B

		------- GEAR 1 --------	GEAR 2 --
Power (kW)	[P]	55.000	
Speed (1/min)	[n]	4983.3	1352.6
Torque (Nm)	[T]	105.4	388.3
Application factor	[KA]	1.25	
Required service life	[H]	20000.00	
Gear driving (+) / driven (-)		+	-

1. TOOTH GEOMETRY AND MATERIAL

(geometry calculation according to ISO 21771:2007)

		------- GEAR 1 --------	GEAR 2 --
Center distance (mm)	[a]	135.000	
Centre distance tolerance		ISO 286:2010 Measure js9	
Normal module (mm)	[mn]	2.7500	
Pressure angle at normal section (°)	[alfn]	20.0000	
Helix angle at reference circle (°)	[beta]	25.5000	
Number of teeth	[z]	19	70
Facewidth (mm)	[b]	32.00	30.00
Hand of gear		left	right
Accuracy grade	[Q-ISO 1328:1995]	7	7
Inner diameter (mm)	[di]	0.00	160.00
Inner diameter of gear rim (mm)	[dbi]	0.00	0.00

Material
Gear 1: SAE8620(20NiCrMo2-2), Case-carburized steel, case-hardened ISO 6336-5 Figure 9/10 (MQ), core strength >=30HRC
Gear 2: SAE8620(20NiCrMo2-2), Case-carburized steel, case-hardened ISO 6336-5 Figure 9/10 (MQ), core strength >=30HRC

Figure 18: Gear software calculations from MagnaPowertrain for the final drive gears for ORNL's matched driveline concept.

Shaft speeds for vehicles benchmarked by ORNL have increased from the 2004 Prius at 6,000 rpm to the 2007 Camry at 14,000 rpm (Table 2). In addition, a non-benchmarked vehicle, the Tesla, boasts a 15,000 rpm motor with a direct driveline from motor to axle. The 2010 Prius motor maximum speed is at 13,500 rpm, and a couple of the others are around 10,000 rpm. The industry appears to have stopped at around 14,000–15,000 rpm, and indications from ORNL studies are that most of the bearings chosen (conventional choices) appear to be near or at design speed limits for their specific applications. Ayers [2] has additional information on this subject.

Table 2: Vehicle speeds and related gearing information

Vehicle (Make/year)	ω_{Motor} (rpm)	Gear Ratio $\omega_{mot}/\omega_{whl}$	# of Clutch Sets	# of Gears mtr-diff'l
2004 Prius	6000	4.11	0	6
2010 Prius	13500	8.61	0	7
2007 Camry	14000	8.78	0	7
LEAF	10400	7.93	0	4
Sonata	6000	6 spd trans.	5 sets	7 (plus idle gears)
2008 Lexus	10200	2 spd trans	2 sets	?
Tesla	15000	8.275	0	?

Conclusions and Future Directions

- Driveline matching for an ORNL high-speed (23,000 rpm) concept motor has been successful. ORNL has two concept motor designs using no PMs that will perform well in this high-speed traction driveline concept.
- A conceptual design was completed showing the concept motor and in-line planetary and main drive gears in conjunction with a drive axle system to demonstrate the geometry of the system and the fit of the motor, gears, and axle. Precise modeling of the final concept system was performed using ProEngineer 3D modeling software based on design models of all the individual components and various calculations.
- Discussions with Regal Beloit early in the year indicated the company's interest in this design and the ORNL MIFP SR concept motor. Regal Beloit provided a potential gear design for the driveline matching gear set (primarily the planetary reduction at the motor). Its research indicated gear speeds were high but not exorbitant.
- Design study and discussions with MagnaPowertrain show strong interest in this area of work and confirm that this design is viable. The company looked further into the gear reduction requirements with ORNL and agreed that the concept using our suggested planetary and two main gears was workable. MagnaPowertrain provided a design for all the gears from the motor shaft to the axle (differential), and those data were used to produce the motor-to-axle 3D model shown in Figs. 12–15.
- Losses are on the order of 3% for the whole ORNL concept gear train from the motor output shaft up to the main differential carrier gear. This loss number is based on rule-of-thumb estimation and potential power calculations for the proposed gear train. Follow-on work will confirm exact losses via modeling and ultimately dynamometer testing in the ORNL laboratory using the ORNL concept motor and prototype gear train.
- High-speed motors enable the following:
  - Smaller, lighter, higher-power-density designs (lower cost)
  - Smaller diameter and a thinner structure that allows closer packaging to the axle (enabling elimination of some gears/bearings)

Future

- Downselect TDS matching architecture
- Continue collaboration with Regal Beloit and MagnaPowertrain
- Continue support of APEEM team with design/modeling

FY 2013 Publications/Presentations

1. "Electric motor and driveline matching," presented at the DOE VPT 2013 Kickoff Meeting, November 2012.
2. "Electric motor architecture R&D," presented at DOE VPT Annual Merit Review poster session, Washington, D.C. May 2013.
3. "Electric motor architecture R&D," presented at the Electrical and Electronics Technical Team meeting, Dearborn, Mich., June 2013.

References

1. J. M. Miller, C. Ayers, A. Wereszczak, B. Ozpineci, R. Wiles, *Design and Development of an Asynchronous Traction Motor to Meet DOE 2020 Targets,* ORNL/TM-2013/60, March 2013.
2. C. W. Ayers, *Traction Drive and Gearing Design Comparisons*, ORNL/TM-2013-482 September 2013.