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Oak Ridge National Laboratory Annual Progress Report for the Power Electronics and Electric Machinery Program

Mitch Olszewski, Program Manager

October 2010

Prepared by
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Oak Ridge National Laboratory Annual Progress Report for the Power Electronics and Electric Machinery Program

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Oak Ridge National Laboratory

Mitch Olszewski, Program Manager

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Energy Efficiency and Renewable Energy
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Susan A. Rogers, Technology Development Manager

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Acronyms and Abbreviations

3-D	three-dimensional
3G	third generation
A/C	air conditioning
ac	alternating current
Al	aluminum
AlN	aluminum nitride
APEEM	Advanced Power Electronics and Electric Machines (ORNL)
AWG	American wire gauge
BJT	bipolar junction transistor
Cds	drain-to-source capacitance
CF-trans-qZSI	current-fed trans-quasi-ZSI
CF-trans-ZSI	current-fed trans-ZSI
CFM	cubic feet per minute
Cgd	gate-to-drain capacitance
Cgs	gate-to-source capacitance
CMOS	complementary metal-oxide semiconductor
CSI	current source inverter
CTE	coefficient of thermal expansion
Cu	copper
DBA	direct bonded aluminum
DBC	direct bonded copper
dc	direct current
DMOS	double diffused metal-oxide semiconductor
DOE	U.S. Department of Energy
DPT	double pulse test
DUT	device under test
ECU	electronic control unit
ECVT	electronically controlled continuously variable transmission
EETT	Electrical and Electronics Technical Team
EV	electric vehicle
EVSE	electric vehicle supply equipment
FEA	finite element analysis
FSCW	fractional slot concentrated winding
FSM	front surface metallization
f_{sw}	switching frequency
GaN	gallium nitride
GCD	greatest common devisor

GUI	graphical user interface
HV	high voltage
IC	integrated circuit
ICE	internal combustion engine
IGBT	insulated gate bipolar transistor
IMMD	integrated modular motor drive
JFET	junction field-effect transistor
LCM	least common multiple
Ld	direct axis inductance
Lq	quadrature axis inductance
LED	light emitting diode
LVDS	low voltage differential signaling
MG	motor-generator
MMF	magnetic motive force
MOSFET	metal-oxide semiconductor field-effect transistor
mph	miles per hour
Nm	Newton meter
OEM	original equipment manufacturer
op-amp	operational amplifier
ORNL	Oak Ridge National Laboratory
PCU	power converter unit
PE	power electronics
PEV	plug-in electric vehicle
PF	power factor
PM	permanent magnet
PMSM	permanent magnet synchronous motor
PSIM	Powersim (circuit simulation software)
PWM	pulse width modulation
R&D	research and development
R-C	resistance-capacitance
R-L	inductor-resistor
RB	reverse-blocking
regen	regeneration
rms	root mean square
SAE	Society of Automotive Engineers
SCP	short circuit protection
Si	silicon
SiC	silicon carbide

SMC	soft magnetic composite
SOA	state-of-the-art
SOI	silicon-on-insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
SPM	surface permanent magnet
SPP	slot/phase/pole
SRM	switched reluctance motor
T_{amb}	ambient temperature
TCIL	thermal conductive insulation layer
TIM	thermal interface material
$T_{initial}$	initial temperature
T_{inlet}	inlet temperature
Tj	junction temperature
TPM	transfer-molded power module
UVLO	undervoltage lockout
Vdc	volts of direct current (operating voltage)
Vgs	gate-source voltage
VSATT	Vehicle Systems Analysis Technical Team
VSI	voltage source inverter
VTP	Vehicle Technologies Program
Wb	weber (SI unit of magnetic flux)
WBG	wide bandgap
WEG	water-ethylene glycol
ZCSI	Z-source current source inverter
ZSI	Z-source inverter

1. Introduction

The U.S. Department of Energy (DOE) and the U.S. Council for Automotive Research (composed of automakers Ford, General Motors, and Chrysler) announced in January 2002 a new cooperative research effort. Known as FreedomCAR (derived from "Freedom" and "Cooperative Automotive Research"), it represents DOE's commitment to developing public-private partnerships to fund high risk, high payoff research into advanced automotive technologies. Efficient fuel cell technology, which uses hydrogen to power automobiles without air pollution, is a very promising pathway to achieve the ultimate vision. The new partnership replaces and builds upon the Partnership for a New Generation of Vehicles initiative that ran from 1993 through 2001.

The Oak Ridge National Laboratory's (ORNL's) Advanced Power Electronics and Electric Machines (APEEM) subprogram within the DOE Vehicle Technologies Program (VTP) provides support and guidance for many cutting-edge automotive technologies now under development. Research is focused on developing revolutionary new power electronics (PE) and electric motor technologies that will leapfrog current on-the-road technologies. The research and development (R&D) is also aimed at achieving a greater understanding of and improvements in the way the various new components of tomorrow's automobiles will function as a unified system to improve fuel efficiency.

In supporting the development of advanced vehicle propulsion systems, the APEEM subprogram has enabled the development of technologies that will significantly improve efficiency, costs, and fuel economy.

The APEEM subprogram supports the efforts of the FreedomCAR and Fuel Partnership through a three phase approach intended to

- identify overall propulsion and vehicle related needs by analyzing programmatic goals and reviewing industry's recommendations and requirements and then develop the appropriate technical targets for systems, subsystems, and component research and development activities;
- develop and validate individual subsystems and components, including electric motors and PE; and
- determine how well the components and subsystems work together in a vehicle environment or as a complete propulsion system and whether the efficiency and performance targets at the vehicle level have been achieved.

The research performed under this subprogram will help remove technical and cost barriers to enable the development of technology for use in such advanced vehicles as hybrid electric vehicles (HEVs), plug-in HEVs (PHEVs), battery electric vehicles, and fuel-cell-powered automobiles that meet the goals of the VTP.

A key element in making these advanced vehicles practical is providing an affordable electric traction drive system. This will require attaining weight, volume, and cost targets for the PE and electrical machines subsystems of the traction drive system. Areas of development include

- novel traction motor designs that result in increased power density and lower cost;
- inverter technologies involving new topologies to achieve higher efficiency, with the ability to accommodate higher temperature environments while achieving high reliability;
- converter concepts that use methods of reducing the component count and integrating functionality to decrease size, weight, and cost;
- new onboard battery charging concepts that result in decreased cost and size;

- more effective thermal control through innovative packaging technologies; and
- integrated motor/inverter concepts.

ORNL's Power Electronics and Electric Machines Research Program conducts fundamental research, evaluates hardware, and assists in the technical direction of the VTP APEEM subprogram. In this role, ORNL serves on the FreedomCAR Electrical and Electronics Technical Team, evaluates proposals for DOE, and lends its technological expertise to the direction of projects and evaluation of developing technologies.

ORNL also executes specific projects for DOE. The following report discusses those projects carried out in FY 2010 and conveys highlights of their accomplishments. Numerous project reviews, technical reports, and papers have been published for these efforts, and they are indicated at the end of each section for readers interested in pursuing details of the work.

Major Accomplishments for Technical Projects

Wide Bandgap Materials

- Acquired, tested, and characterized silicon carbide (SiC) junction field-effect transistors (JFETs), metal-oxide semiconductor field-effect transistors, bipolar junction transistors, and diodes.
- Developed a SPICE model for a 1200 V, 10 A, SiC JFET.
- Developed a traction drive model to simulate the performance of wide bandgap devices over different drive cycles.

Direct Water-Cooled Power Electronics Substrate Packaging

- Finalized a design and performed finite element analysis simulations.
  - — Validated results by comparing to experimental results.
  - — Achieved agreement between 10% and 15%.
- Confirmed through simulations and tests that the maximum junction temperature could be maintained below 165°C using 105°C coolant at 30 kW continuous power.

High Temperature, High Voltage Fully Integrated Gate Driver Circuit

- Designed, fabricated, and packaged a silicon-on-insulator chip for operation at 200°C. The device completed this year incorporates the following features.
  - — On-chip voltage regulator.
  - — Undervoltage lockout, short circuit, desaturation, and thermal shutdown protection.
  - — Gate current monitoring.
  - — Low voltage differential signaling circuit.
  - — Drive current capability greater than 5 A at 200ºC.
  - — Switching frequency greater than 100 kHz.
  - — 100% high side duty cycle with charge pump.

Inverter Using Current Source Topology

- Developed two new Z-source current source inverters (ZCSIs) with a reduced component count, a current-fed trans-Z-source inverter (CF-trans-ZSI) and a current-fed trans-quasi-ZSI (CF-trans-qZSI). The new ZCSIs have a higher voltage boost ratio of 3 vs 2 for the previous ZCSIs.

- Completed a design for a 55 kW ZCSI based on the CF-trans-qZSI using first generation reverse blocking (RB) insulated gate bipolar transistor (IGBT) technology. The design yields a specific power of 4.89 kW/kg and a power density of 15.5 kW/L.
- Confirmed through simulation the feasibility of using the ORNL V-I converter-based current source inverter (CSI) topology in series and power-split series-parallel HEV configurations. The CSI dual-motor-drive using RB-IGBTs provides significant performance improvements over the Camry PE:
  - 49% increase of specific power (6.4 vs 4.3 kW/kg),
  - 60 % increase of power density (9.9 vs 6.2 kW/kg), and
  - 34% reduction of cost ($15.4/kW vs $23.2/kW).

Segmented Drive Inverter Topology with a Small dc Bus Capacitor

- Designed, built, and successfully tested a 55 kW segmented inverter prototype achieving a 60% reduction in direct current (dc) bus capacitance with an inductor-resistor load and an induction motor. Test results show significant reductions of
  - 55%~75% in capacitor ripple current,
  - 70%~90% in battery ripple current, and
  - 60%~80% in motor ripple current.

Novel Packaging to Reduce Stray Inductance in Power Electronics

- Developed a new packaging method based on P- and N-cells to reduce the stray inductance between the active switch (IGBT) and diode.
- Completed electromagnetic and circuit simulations showing the reduction of parasitic inductance (20% reduction) and resistance and corresponding improvement in overshoot voltage in a proposed package module (15% reduction).
- Developed a 10 kW phase leg power module that incorporates the novel circuit layout.

High Temperature Air-Cooled Traction Drive Inverter Packaging

- Completed a parametric study to determine the feasibility and boundary conditions required for an air-cooled 55 kW peak/30 kW continuous power rated inverter.
- Performed simulations for steady state and under drive cycle conditions to determine design and junction temperature effects with varying parameters.

Power Device Packaging

- Benchmarked multiple state-of-the-art commercial packaging technologies and assessed advanced packaging approaches.
- Developed and simulated an innovative device module packaging concept.
- Designed and outfitted a state-of-the-art packaging laboratory.

New Class of Switched Reluctance Motors Without Permanent Magnets

- Verified through simulations that the design meets 2015 performance targets with less than 5% torque ripple.

- Designed entire assembly, prepared drawings for fabrication, received all parts, and began assembling prototype motor.

Novel Flux Coupling Motor Without Permanent Magnets

- Finalized a mechanical design which will allow the rotor to safely operate at 14,000 RPM.
- Initiated fabrication of the prototype motor.

Benchmarking Competitive Technologies

- Completed evaluation of the 2010 Prius, including
  - efficiency mapping of subcomponents and system,
  - packaging and manufacturing analysis, and
  - component performance assessment.

High-Power-Density Integrated Traction Machine Drive

- Identified a six-phase, 10-pole permanent magnet (PM) machine as the most promising configuration.
- Investigated a heterarchical control architecture for achieving fault tolerant operation.
- Characterized high temperature static and switching behaviors of candidate silicon devices.
- Designed and simulated performance of a baseline 10 kW phase leg power module with 105°C cooling.

Assessment of Motor Technologies

For the past several years, the interior PM (IPM) motor has been considered the obvious choice for electric traction drive systems. However, with the rapidly increasing costs of magnets and the possibility of a future shortage of rare earth metals, the IPM motors may not continue to be the economic or technical favored option. Because of this it is timely to consider other options for motor types.

To provide a basis for deciding which research topics should be pursued, an assessment of motor technologies has been undertaken to determine which, if any, of various motor technologies is *potentially* capable of meeting FreedomCAR 2015 and 2020 targets. Input to the assessment was obtained primarily from interviews with experts and follow-on technical briefs that focused on critical topics identified during the interviews. The list of experts includes original equipment manufacturers, automotive suppliers, leading researchers in academia, and consultants. In addition, past ORNL reports, previous assessments, and magnet literature were reviewed. For each technology, discussions focused on the current state-of-the-art performance and cost, recent trends in the technology, inherent characteristics of the motor that either limit the ability of the technology to meet the targets or aid in meeting the targets, the R&D that would be needed to meet the targets, and the potential for the technology to meet the targets.

The motor technologies considered in the assessment are all brushless and include both PM motors and motors without PMs.

Four types of PM motors were considered. *IPM motors* were treated in detail and form the baseline against which other types of motors were compared. *Surface-mounted PM motors* were treated only briefly because they have no apparent advantage over IPM motors. *Wheel motors* were treated only briefly because they are not a high priority among the automotive manufacturers and are not a major emphasis in the FreedomCAR program. *Multiple-rotor motors* also were treated only briefly because

previous research indicated that there are significant challenges that would require extensive R&D with a questionable probability of success.

Three types of motors without PMs were considered. Although inferior to IPM motors in performance and being a relatively mature technology, *induction motors* were treated in detail because they are relatively inexpensive and they were considered seriously before the introduction of IPM motors. If rare earth PMs become unavailable or too expensive in the future, induction motors may be the preferred option for many applications. Although there are problems with torque ripple and noise with *switched reluctance motors*, they were considered in detail because they are rugged and relatively inexpensive. *Motors with external excitation* were considered in detail because it is a relatively new technology with unknown but possibly exciting potential.

No new concepts emerged during the interviews conducted in FY 2010.

During FY 2010 interviews were conducted with Chrysler, Ford, GM, five suppliers, four consultants, and various researchers at Ames Laboratory and ORNL. Several additional interviews will be conducted early in FY 2011, and then a final report will be prepared.

Plug-In Hybrid Electric Vehicle Assessment

More battery powered electric vehicles (EVs) and PHEVs will be introduced to the market in 2011 and beyond. Because these vehicles have large batteries that need to be charged from an external power source or directly from the grid, their batteries, charging circuits, charging stations/infrastructures, and grid interconnection issues are garnering more attention. This report summarizes information regarding the batteries used in PHEVs, different types of chargers, charging standards and circuits, comparing different topologies. It also includes a list of vehicles that are going to be in the market soon together with a list of different charging stations and manufacturers. A summary of different standards governing charging circuits and charging stations concludes the report.

There are several battery types that are available for PHEVs, but the most popular ones have nickel-metal hydride and lithium ion (Li ion) chemistries. The former one is being used in current HEVs, but the latter will be used in most of the PHEVs and EVs because of its higher energy densities and higher efficiencies.

The chargers that can be used to charge these vehicles can be classified based on the circuit topologies (dedicated or integrated), location of the charger (either on or off the vehicle), connection (conductive, inductive/wireless, and mechanical), electrical waveform [dc or alternating current (ac)], and direction of power flow (unidirectional or bidirectional). The first PHEVs typically will have dedicated onboard unidirectional chargers that will have conductive connections to the charging stations and will be charged using either dc or ac. In the near future, bidirectional chargers might also be used in these vehicles once the benefits of practical vehicle to grid applications are realized.

The terms charger and charging station cause terminology confusion. To prevent misunderstandings, the more descriptive term of “electric vehicle supply equipment” (EVSE) is used instead of charging station. The charger is the power conversion equipment that connects the battery to the grid or another power source, while EVSE refers to external equipment between the grid or other power source and the vehicle, and it might include conductors, connectors, attachment plugs, microprocessors, energy measurement devices, transformers, etc. Currently there are around a dozen companies that are producing EVSEs.

There are several standards and codes regarding conductive and inductive chargers and EVSEs from the Society of Automotive Engineers (SAE), Underwriters Laboratories, the International Electrotechnical Commission, and the National Electric Code. The two main standards from SAE describe the

requirements for conductive and inductive coupled chargers and the charging levels. Three levels are specified for inductive coupled charging: Level 1 (120 V and 12 A, single phase), Level 2 (208–240 V and 32 A, single phase), and Level 3 (241–600 V and 400 A, three phase). The standard for the conductive coupled charger also has similar charging levels for Levels 1 and 2, but it allows higher current levels for Level 2, charging up to 80 A. Level 3 charging for this standard is still under development and considers dc charging instead of three phase ac.

More details in these areas and related references can be found in the upcoming ORNL report on PHEV assessment.

2. Power Electronics Research and Technology Development

2.1 Wide Bandgap Materials

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Objectives

- To keep up-to-date with the state-of-the-art wide bandgap (WBG) power devices and acquire, test, and characterize newer WBG power devices.
- To assess the system level impact of WBG semiconductor devices on hybrid electric vehicles.

Approach

- Evaluate device performance: Acquire, test, and characterize newer WBG power devices, including
  - static characteristic tests,
  - dynamic characteristic tests, and
  - behavioral modeling.
- Develop behavioral SPICE (Simulation Program with Integrated Circuit Emphasis) models for packaging projects.
  - Specific device tests will be performed to extract the parameters required for behavioral SPICE models.
  - These models will be used to study the parasitic parameters in a package.
- Perform inverter simulations with selected device models. The inverter simulations will be performed to evaluate the impact of the device performance at system level.
- Prepare a summary report for incorporation in the Vehicle Technologies Program annual report that includes the device test results and SPICE modeling results.

Major Accomplishments

- Acquired, tested, and characterized silicon carbide (SiC) junction field-effect transistors (JFETs), metal-oxide semiconductor field-effect transistors (MOSFETs), bipolar junction transistors (BJTs), and diodes.
- Developed SPICE model for a 1,200 V, 10 A, SiC JFET.
- Developed a traction drive model to simulate the performance of the WBG devices over different drive cycles.

Future Direction

- Acquire, test, and characterize state-of-the-art and newer technology WBG power devices.

- Develop SPICE models of the devices.
- Continue to optimize drive model for determining system level performance of devices.

Technical Discussion

1. Device Testing

The WBG devices acquired this year are "normally off" SiC JFETs, SiC BJTs, SiC MOSFETs, and SiC junction barrier Schottky (JBS) diodes. On-state characteristics and switching energy losses of the devices were obtained, and the voltage blocking capability of the devices over a wide temperature range was tested. The test results for these devices will be presented in the following sections. All the devices obtained were experimental samples.

1.1 Normally Off 1,200 V, 50 A, SiC JFET

Static characteristics of a 1,200 V, 50 A, normally off SiC JFET at different operating temperatures are shown in Fig. 1. Normally off devices are the preferred type of device in power converters for fail-safe operation. The forward characteristics were obtained for a gate voltage of +3 V. The forward voltage drop of the device at 15 A increased from 0.7 V at 25°C to 2.2 V at 175°C. This shows that the power dissipation of the device would limit the device operation to 15 A at higher temperatures. The leakage current of the device was obtained over the temperature range of 25°C to 150°C and up to 600 V (Fig. 2).

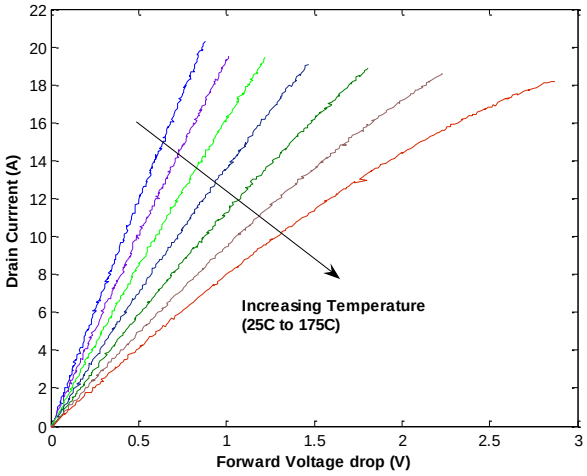

Fig. 1. i-v curves of a 1,200 V, 50 A, SiC JFET.

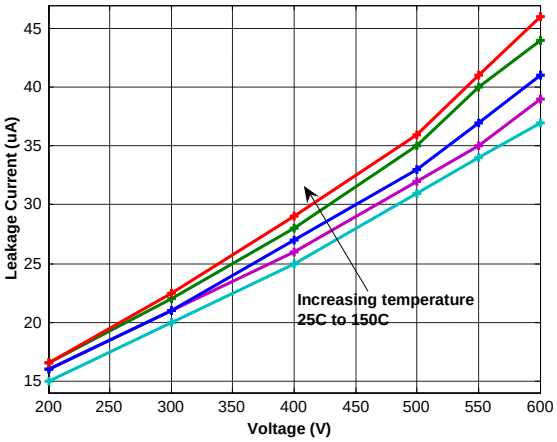

Fig. 2. Leakage current vs voltage of 1,200 V, 50 A, JFET.

The "turn-on" and "turn-off" energy losses of the JFET were obtained using the double pulse circuit with a load inductance of 360 µH, and a 1,200 V, 30 A, SiC JBS diode was used as the clamping diode in the circuit. The gate driver used for this testing was a commercial gate driver board SGDR600P1. The device requires constant current for the device to remain switched on, and this features demands more power from the gate driver. The data were obtained at 600 V and 400 V dc for various currents at 25°C and 175°C. The total energy losses increase with increase in current; however, not significantly (Figs. 3 and 4).

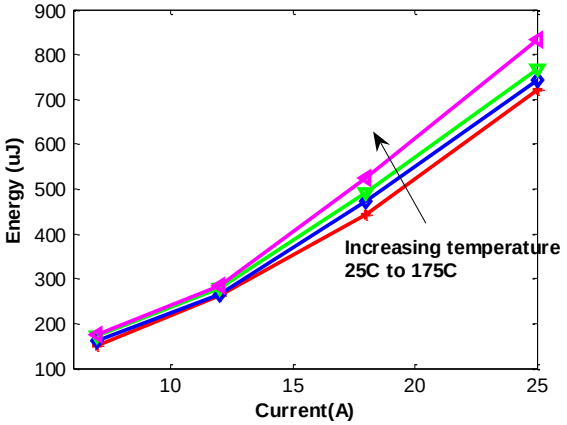

Fig. 3. Total switching energy losses of a 1,200 V, 50 A, SiC JFET at 600 V.

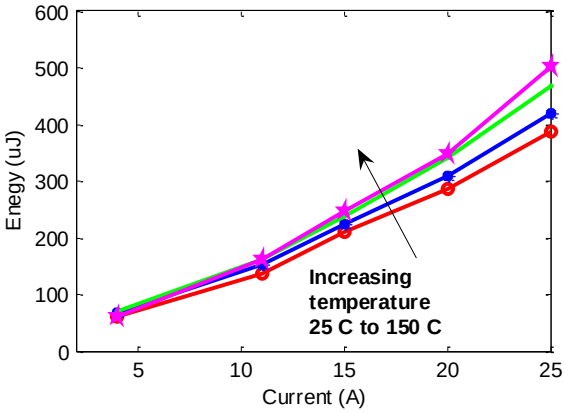

Fig. 4. Total switching energy losses of a 1,200 V, 50 A, SiC JFET at 400 V.

1.2 Normally Off 1,200 V, 100 A, SiC JFET

A 1,200 V, 100 A, normally off SiC JFET in an experimental half bridge module was tested. The on-state characteristics were obtained at +3 V gate-source voltage (Vgs). Static characteristics of the JFET are shown in Fig. 5 for different operating temperatures. The leakage current of the JFETs in the module was measured over the temperature range of 25°C to 150°C. The measured leakage current did not change with temperature (Fig. 6). It should be noted that the module had a snubber across the dc link inside the module and part of the current could be driving the capacitor in the snubber.

The module had a wire bonding issue and the gate of the upper device could not block at high voltages. However, the devices in the module were still functional. The turn-on and turn-off energy losses of the JFET were obtained using the double pulse circuit with a load inductance of 110 µH. An external 600 V, 75 A, Schottky diode was used as the clamping diode in the circuit. The gate drive used for the test was a commercial IDD409 IXYS chip with 35 V, 9 A, output drive capability similar to the single JFET device. The data were obtained at 600 V dc for various currents and for 25°C and 175°C. The total energy losses increase with increase in current; however, not significanltly. (Fig. 7).

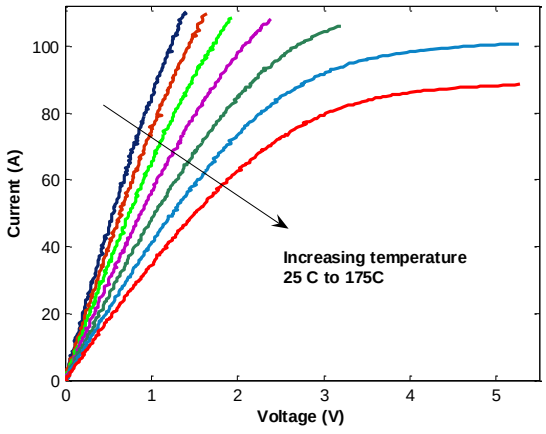

Fig. 5. i-v curves of a 1,200 V, 100 A, SiC JFET.

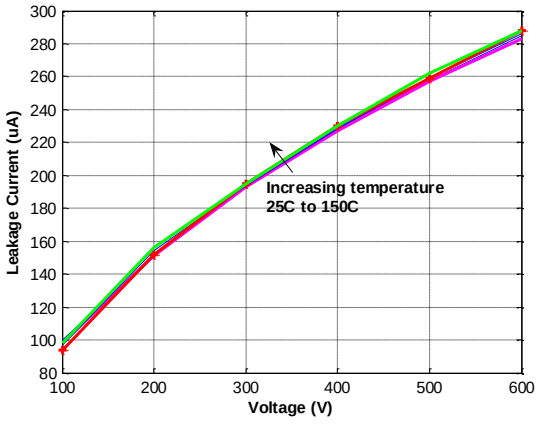

Fig. 6. Leakage current vs voltage of a 1,200 V, 100 A, JFET.

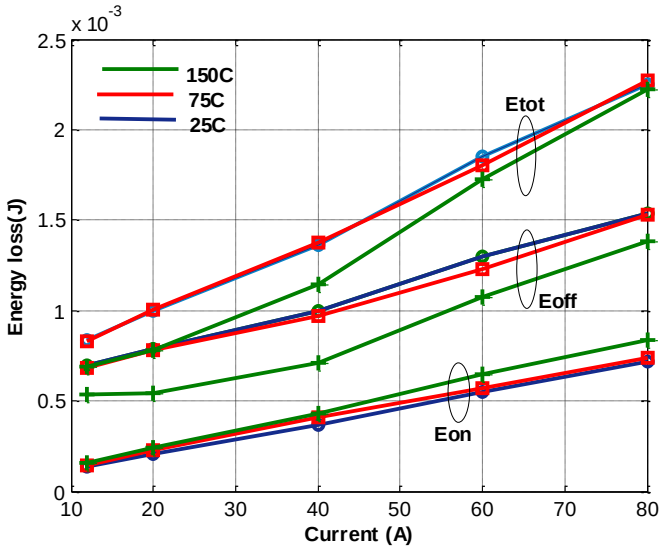

Fig. 7. Switching losses of 1,200 V, 100 A, SiC JFET.

1.3 SiC BJT (1,200 V, 6 A)

The SiC BJT is a current controlled device unlike the voltage controlled FET devices. Experimental samples (1,200 V, 6 A) were obtained and tested. The static characteristics of the SiC BJT were obtained at 350 mA of base current and over a temperature range of 25°C to 175°C (Fig. 8). The low forward voltage drop at 6 A shows that this device could be operated up to 10 A at 175°C. The leakage current at different voltages over a temperature range of 25°C to 150°C is shown in Fig. 9. The leakage current at 600 V increases from 1.5µA at 25°C to 3.6 µA at 150°C. Because the gate drive requirements are very similar, the BJT was tested with the same gate driver as the normally off SiC JFET. The BJT was tested with the 1,200 V, 8 A, SiC JBS diode in the chopper circuit. The total switching energy losses of the BJT at 400 V and 600 V at different temperatures are shown in Fig. 10. The losses do not change much with temperature.

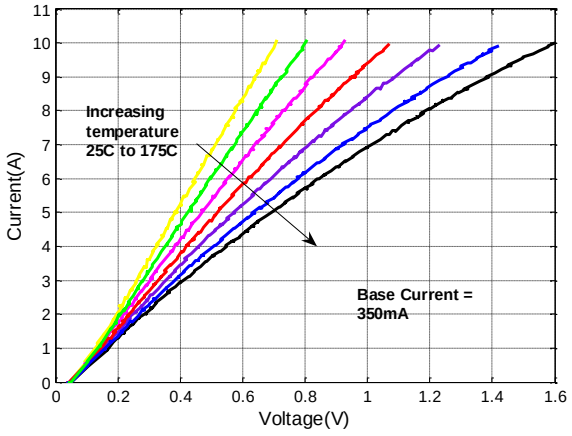

Fig. 8. i-v curves of a 1,200 V, 6 A, SiC BJT.

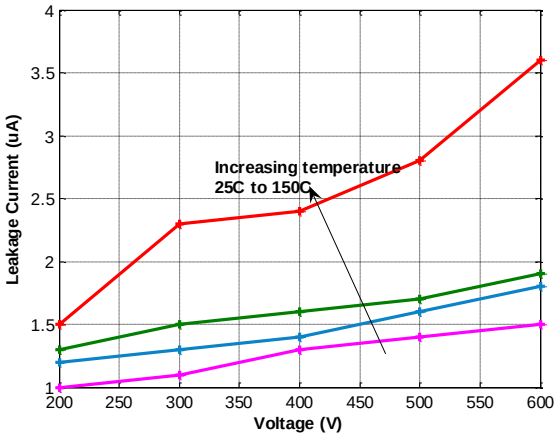

Fig. 9. Leakage current vs voltage of a 1,200 V, 6 A, SiC BJT.

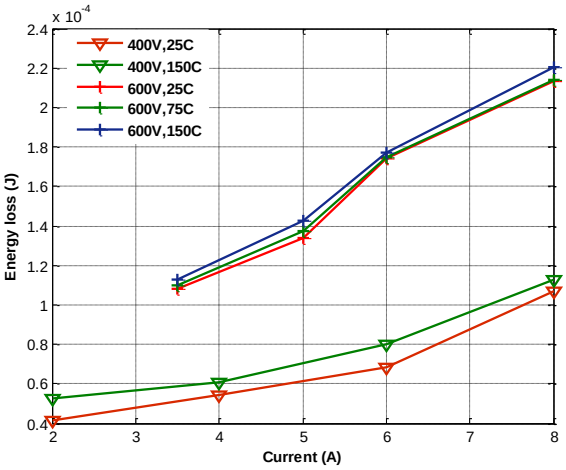

Fig. 10. Total switching energy losses of 1,200 V, 6 A, SiC BJT at 400 V and 600 V.

1.4 SiC JBS Diode (1,200 V, 30 A)

The static characteristics of a 1,200 V, 30 A, SiC JBS diode were obtained over a wide temperature range (25°C–225°C) (Fig. 11). The diodes were specifically designed for high temperature operation. The leakage current of the diode at a blocking voltage of 600 V is about 0.5 µA at 25°C and increases to 3.7 µA at 200°C (Fig. 12). This clearly shows that the device can block higher voltages at higher temperatures. The SiC JBS diode was tested in the same chopper circuit as the SiC 50A normally off SiC JFET with double pulse switching to obtain its dynamic characteristics. The turn-off energy losses of the JBS diode at 200 V, 400 V, and 600 V over a wide temperature range are shown in Fig. 13. The turn-off losses do not change much with temperature or current, exhibiting temperature independent switching loss behavior. However, the loss increases as the voltage increases.

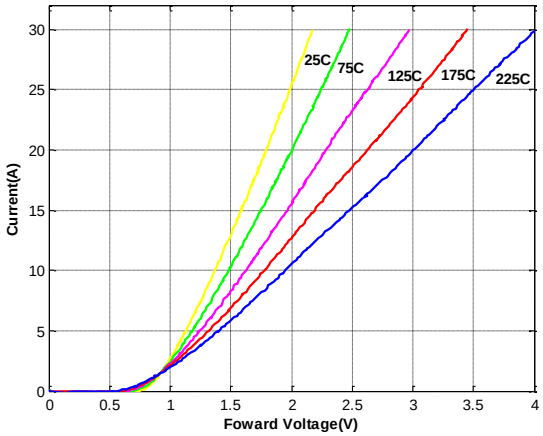

Fig. 11. I-v curves of a 1,200 V, 30 A, SiC JBS diode.

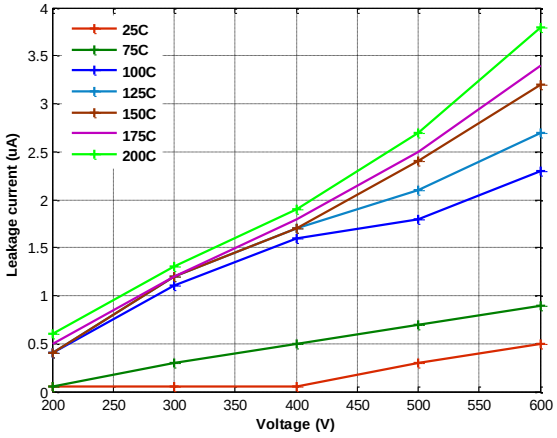

Fig. 12. Leakage current vs voltage for a 1,200 V, 30 A, SiC JBS diode.

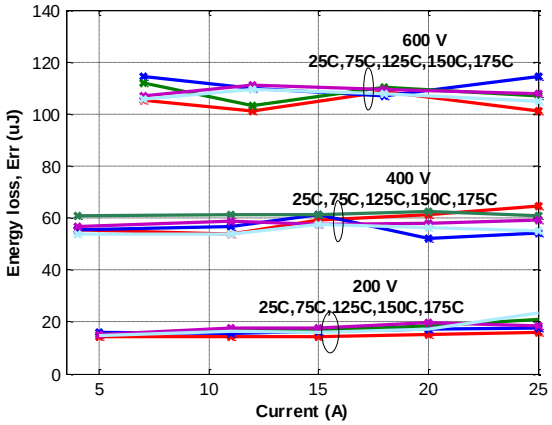

Fig. 13. Switching energy losses of 1,200 V, 30 A, SiC JBS diode at 200 V, 400 V, and 600 V.

1.5 SiC JBS Diode (1,200 V, 8 A)

The static characteristics of a 1,200 V, 8 A, SiC JBS diode were obtained over a wide temperature range (25°C–225°C) (Fig. 14). The diodes were specifically designed for low leakage currents at high temperaturesn. The leakage current of the diode at a blocking voltage of 600 V is about 0.05 µA at 25°C and increases to 4.3 µA at 200°C (Fig. 15). This clearly shows that the device can block higher voltages at higher temperatures. The SiC JBS diode was tested in the same chopper circuit as the 1,200 V, 6 A, SiC BJT with double pulse switching to obtain its dynamic characteristics. The turn-off energy losses of the JBS diode at 400 V and 600 V at different temperatures are shown in Fig.16. The turn-off losses do not change much with temperature or current, exhibiting temperature independent switching loss behavior. However, the loss increases as the voltage increases.

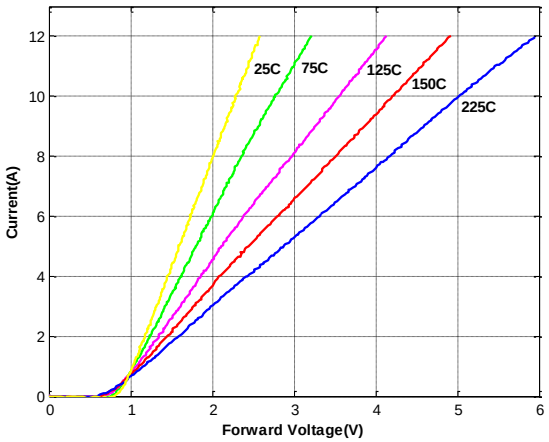

Fig. 14. i-v curves of a 1,200 V, 8 A, SiC JBS diode.

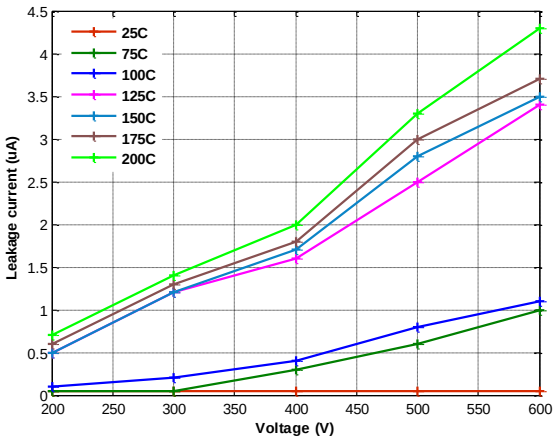

Fig. 15. Leakage current vs voltage of a 1,200 V, 8 A, SiC JBS diode.

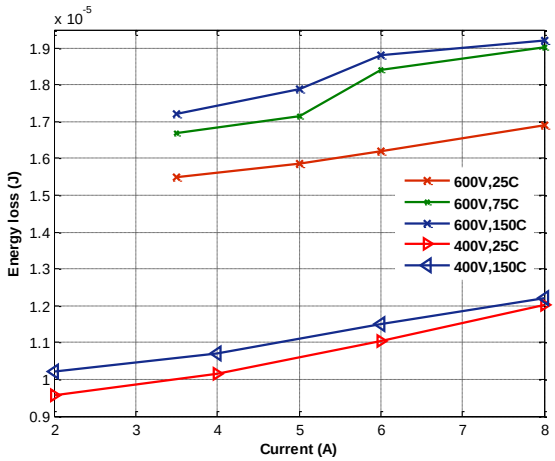

Fig. 16. Switching energy losses of a 1,200 V, 8 A, SiC JBS diode at 400 V and 600 V.

1.6 SiC MOSFET (1,200 V, 100 A)

Static characteristics of a 1,200 V, 100 A, SiC MOSFET in a half bridge module for different operating temperatures at 20 V Vgs are shown in Fig. 17. This module was built using the commercial Si CM100DY-24A half bridge module package. The SiC MOSFET was tested in a chopper circuit with double pulse switching to observe its dynamic characteristics. The gate driver used for obtaining the dynamic characteristics is a commercial gate driver (HCPL 316J). The gate voltage was switched from +15 V Vgs to −5V. The diode in the half bridge module was used as the clamping diode with a 110 µH inductor as the load. The total switching energy losses of the MOSFET at 600 V and 400 V are shown in Fig.18. The switching losses increase with an increase in current and do not change much with temperature.

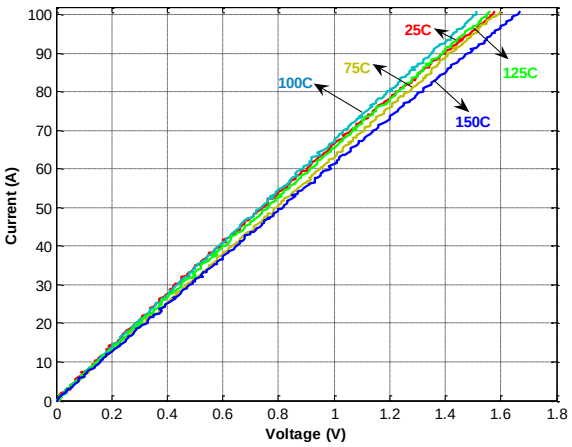

Fig. 17. i-v curves of a 1,200 V, 100 A, SiC MOSFET.

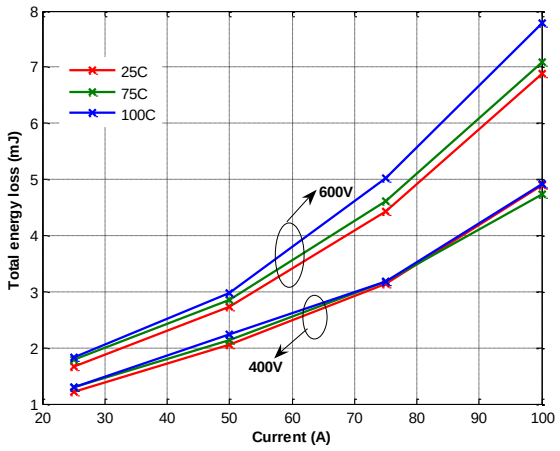

Fig. 18. Switching energy losses of a 1,200 V, 100 A, SiC MOSFET at 400 V and 600 V.

1.7 SiC JBS Diode (1,200 V, 100 A)

The static characteristics of a 1,200 V, 100 A, SiC JBS diode in the SiC MOSFET module were obtained across a wide temperature range (25°C–150°C) (Fig. 19). The diode has negative temperature coefficient below 10 A current and positive temperature coefficient above 10 A. The SiC JBS diode was tested in the

same chopper circuit as the SiC MOSFET with double pulse switching to observe its dynamic characteristics. The turn-off energy losses of the JBS diode at 600 V and 400 V are shown in Fig. 20. The turn-off losses do not change much with temperature, exhibiting temperature independent switching loss behavior. Also, the turn-off losses do not change much with an increase in current; however, the losses increase with increasing voltage.

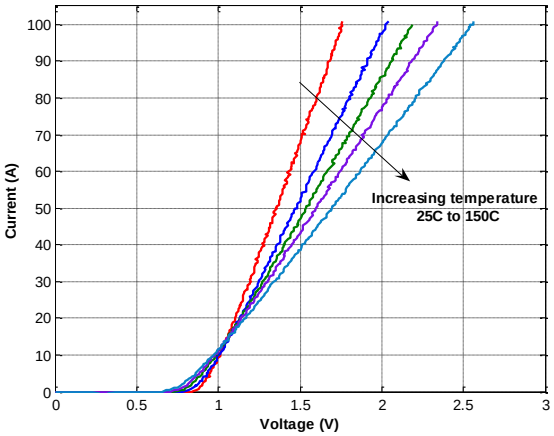

Fig. 19. i-v curves of a 1,200 V, 100 A, SiC JBS diode.

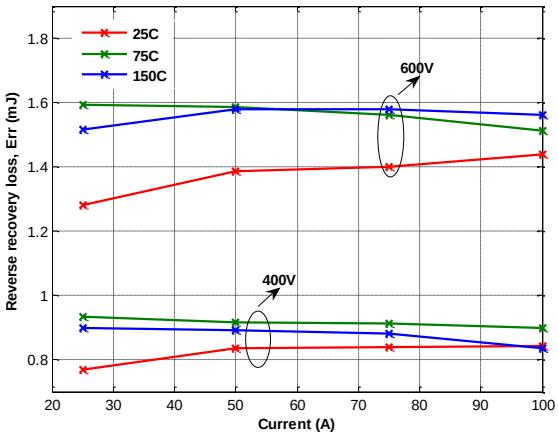

Fig. 20. Switching energy losses of a 1,200 V, 100 A, SiC JBS diode at 400 V and 600 V.

2. Traction Drive Model

The model consists of two parts: (1) an electric motor/generator model that computes the current, voltage, and phase angle that will optimally produce 100% of the torque required at each time step and (2) an inverter loss model that computes the temperature dependent device losses associated with the voltages, currents, and frequencies demanded by the motor.

For this study, the speed and power required for the drive were generated using Camry-like reference vehicle characteristics. The driving profile followed by the vehicle was the standard US06 Supplemental Federal Test Procedure—a 20 minute, 8-mile-long combination of urban and highway driving with 80 miles per hour (mph) peak and 52 mph average moving speeds. Assuming a flat terrain and no atmospheric wind, the average and peak road-power demands placed on the vehicle's motor were 25.1 kW/100 kW for propulsion and 19.7 kW/68.6 kW for braking.

2.1 Internal Permanent Magnet Motor Model

The motor model emulates a typical Camry-like eight-pole internal permanent magnet machine, characterized by parameters extracted from testing done at ORNL. The motor model follows the classic d-q (direct-quadrature) transformation approach. The model allows for regenerative recovery of the vehicle's excess kinetic energy that is conventionally wasted in the brakes by friction. When the vehicle's power demand is negative, the motor acts as a generator. The motor model takes all or part of the road-power demand as input and computes the frequency, current, voltage, and phase angle that will optimally produce the torque required at each time step. In a pure electric power mode the full road-demand is placed on the electric motor. In a hybrid configuration the fraction of power allocated to the motor can vary from 0% to 100% of the required road power depending on the hybridization power sharing scheme.

In this study it is assumed that most of the power demand of the drive cycle will be supplied by the electric drivetrain, and in the regions where the demand is more than the maximum power of the motor, the engine will generate the power. The available maximum terminal voltage limits the output power of the motor, which is dependent on the dc bus voltage with maximum boost. The terminal voltage is calculated assuming a six-step inverter mode of operation. The maximum current and voltage demands on the motor are 240 A and 300 V.

2.2 Inverter Model

The inverter loss model was implemented with a conduction loss model developed using averaging techniques described in [1] and switching loss equations derived based on switching energy loss data. The temperature dependent conduction loss parameters, on-state resistance and voltage drop, and switching losses were obtained from testing the 1,200 V, 100 A, SiC MOSFET module. The module test data were presented in Sects. 1.6 and 1.7. In addition to the power, current, power factor, and voltage demands computed by the motor model, the conduction loss model requires the modulation index as input. This index was calculated as the ratio of the terminal voltage required by the motor and the dc-link voltage provided by the boost converter. The boost factor as a function of torque and speed was empirically derived from test data for a Camry drive system following the US06 drive cycle. The boost function shown in Fig. 21 was obtained by curve fitting the test data. The test data were provided by Argonne National Laboratory. The battery voltage and the bus voltage are shown in Fig. 22.

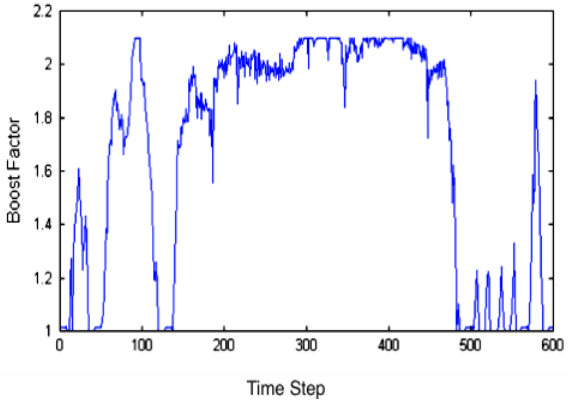

Fig. 21. Boost factor calculated from vehicle test data.

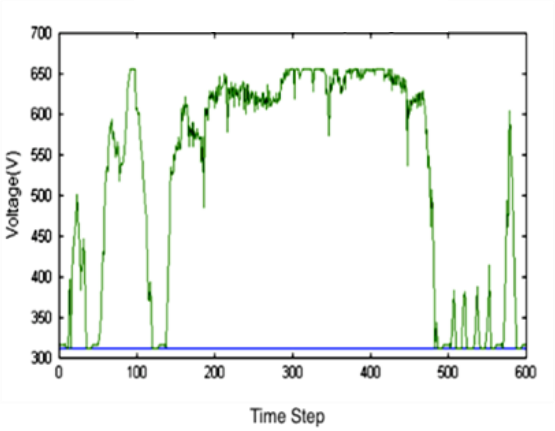

Fig. 22. Bus voltage (green) and battery voltage (blue).

The maximum boost factor is about 2.1 for the US06 drive cycle. The computation of the temperature dependent power losses in switches and diodes iterates with a thermal model that computes the junction temperatures from the power losses assuming a constant heat sink temperature. The devices tested were a MOSFET and a JBS diode in a 1,200 V, 100 A, half bridge SiC module prototype. The SiC module has two SiC MOSFETs and two JBS diodes. The inverter for this study was simulated with three switch–diode pairs (300 A rating) per phase in a full bridge configuration to accommodate the maximum current of 240 A for the drive cycle.

2.3 Simulation Results

The drive model was simulated for the US06 drive cycle with SiC MOSFET and diode models at switching frequencies of 10 kHz and 20 kHz and two different coolant temperatures: 70°C and 105°C. The drive model outputs time dependent, cycle average, and cumulative values of interest for all pertinent parameters. The simulated efficiencies of an all-SiC (SiC MOSFET/SiC Schottky diode) inverter are

shown in Table 1. The table shows the average inverter efficiency and inverter losses over the drive cycle for 10 and 20 kHz operation with both 70°C and 105°C cooling .

Table 1. Simulation Results of Traction Drive for US06 Drive Cycle

Coolant temperature (°C)	Operating frequency	
	10 kHz	**20 kHz**
Inverter efficiency (%)		
70	97.43	95.41
105	97.39	95.34
Inverter energy loss (kJ)		
70	338.9	617.6
105	344.3	626.7

The inverter efficiency corresponds to the switching and conduction losses of devices in the inverter only, and the losses in the boost converter are not included. For 10 kHz operation, the efficiency of the SiC inverter decreased by only 0.1% from 70°C to 105°C coolant temperature condition because of the temperature independence of its switching losses. However, when the switching frequency was increased from 10 kHz to 20 kHz the efficiency of the SiC inverter decreased by 2.02% and 2.05%, respectively, at 70°C and 105°C coolant temperatures.. This illustrates that the low losses and high temperature capability of SiC devices will certainly improve the system efficiency and increase the power density of the inverter.

3. SPICE Model

In FY 2010, one of the tasks was to develop behavioral SPICE models of WBG devices. The device chosen this year was a 1,200 V, 10 A, normally on SiC JFET. The model was developed using the parameters obtained using the test data. The forward and dynamic behavior of the device was simulated and compared to the measured data. The details of the modeling are described below.

3.1 Equivalent Circuit of JFET

The equivalent circuit of the JFET is shown in Fig. 23. The circuit elements include gate resistance and inductance (Rg, Lg); drain series inductance (Ld); source series inductance (Ls); and the junction capacitances between the three terminals, gate-to-source (Cgs), gate-to-drain (Cgd), and drain-to-source (Cds). The values of Rg, Lg, Ld, and Ls were obtained from the device manufacturer [2] (Rg = 6 Ohms, Lg = 5 nH, Ld = 1nH, and Ls = 1 nH). The junction capacitance values were extracted from the test data as shown in Figs. 24, 25, and 26. The data were curve fitted and the equations were derived as shown below.

$$C_{gd} = 10^{-12} * (72.61 * exp(-0.05 * V_{ds}) + 45.2 * \exp(-0.002648 * V_{ds})) \quad . \tag{3.1}$$

$$C_{gs} = 10^{-12} * (0.005 * V_{gs}^4 + 0.3321 * V_{gs}^3 + 7.543 * V_{gs}^2 + 78.13 * V_{gs} + 1082) \quad . \tag{3.2}$$

$$C_{ds} = 10^{-12} * (587.9 * exp(-0.105 * V_{ds}) + 159.1 * \exp(-0.0051 * V_{ds})) \quad . \tag{3.3}$$

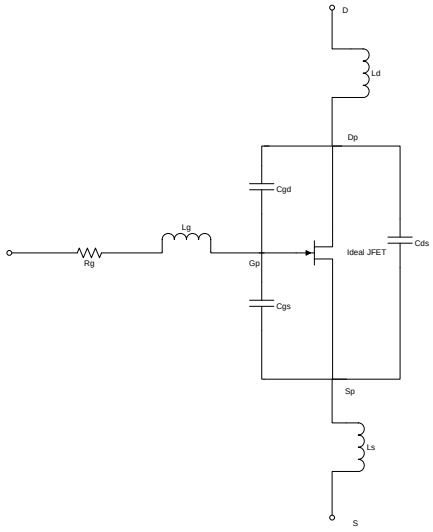

Fig. 23. Equivalent circuit of a SiC JFET.

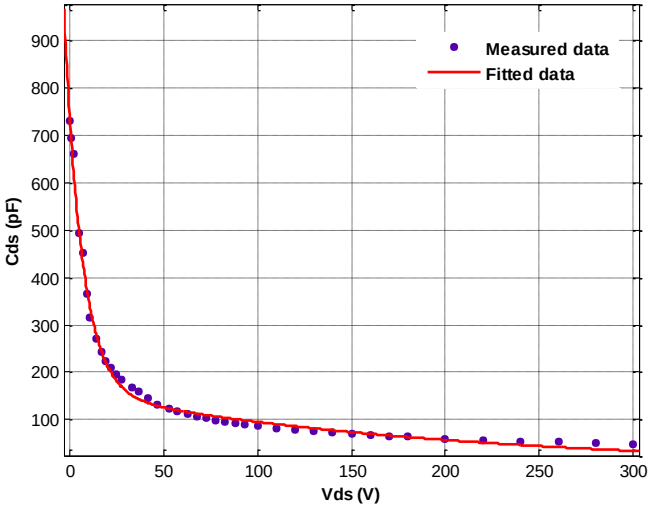

Fig. 24. Drain to source capacitance (Cds) vs drain to source voltage (Vds).

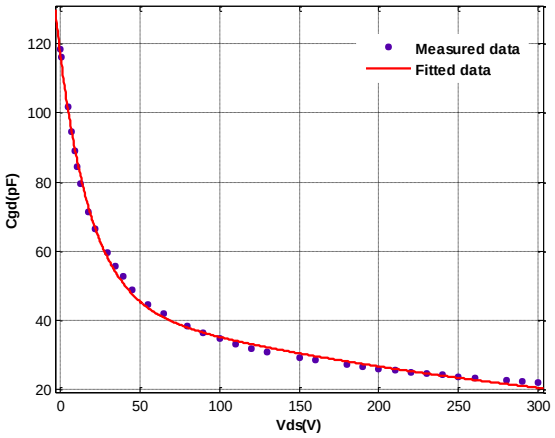

Fig. 25. Gate to drain capacitance (Cgd) vs Vds.

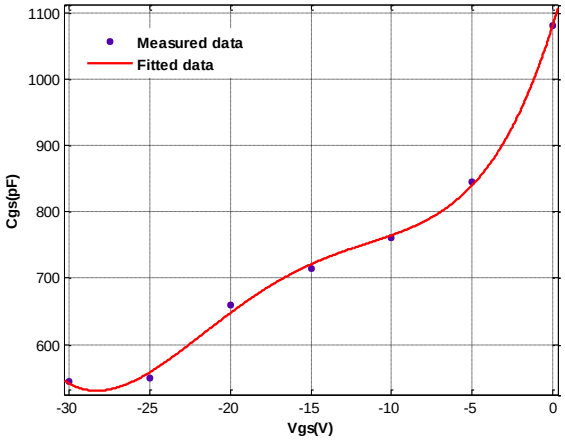

Fig. 26. Gate to source capacitance (Cgs) vs gate-source voltage (Vgs).

The current through the device can be represented as

$$I_D(T,Vgs,Vds) = I_S(T,Vgs) * (1 - e^{-c(T,Vgs)*Vds}) \quad , \tag{3.4}$$

where I_D is the current going through the device, *Is* is the saturation current, and *c* is the speed at which the current reaches its saturation value. The temperature dependence of the current was modeled using the forward characteristics obtained over the range of temperatures. *Is* and *c* are a function of both gate-to-source voltage (Vgs) and the junction temperature (T). The equations for forward characteristics over different temperatures can be described as follows.

$$I_S(T,Vgs) = I_{S0}(T) + I_{S1}(T) * Vgs + I_{S2}(T) * V_{gs}^2 \quad . \tag{3.5}$$

$$I_{S0}(T) = 0.000512 * T^2 - 0.1832 * T + 37.65 \quad . \tag{3.6}$$

$$I_{S1}(T) = 0.0001467 * T^2 - 0.04011 * T + 4.278 \ . \quad (3.7)$$

$$I_{S2}(T) = -0.0005475 * T + 0.09581 \ . \quad (3.8)$$

$$C(T, Vgs) = C_2(T) * V_{gs}^2 + C_1(T) * V_{gs} + C_0(T) \ . \quad (3.9)$$

$$C_2(T) = 5.829 * 10^{-8} * T^2 - 1.117 * 10^{-8} * T - 0.001683 \ . \quad (3.10)$$

$$C_1(T) = 1.039 * 10^{-6} * T^2 - 0.0002609 * T - 0.01116 \ . \quad (3.11)$$

$$C_0(T) = -0.1211 \ . \quad (3.12)$$

3.2 Validation of the Model

The SPICE model of the SiC JFET was validated using two different test circuits, one for static characteristics and one for dynamic characteristics. The static characteristics of the device were obtained using a 371B curve tracer, and the simulation results were obtained by sweeping the current to saturation at different gate voltages and different temperatures. The forward characteristics obtained from simulation at 25°C are shown in Fig. 27. The comparison of simulation and tests results for a gate voltage of −10 V at different temperatures is shown in Fig. 28. The device current in the saturation region and the linear region matches the test results very closely. The dynamic characteristics of the test data were obtained from the double pulse test circuit at 300 V and 5 A using a 600 V, 6 A, Schottky diode. The SPICE model of the diode was obtained from Cree for a similar diode and used in the simulation. The switching curves in Figs. 29 and 30 show an excellent match between the simulation and test results for both the current and the voltage.

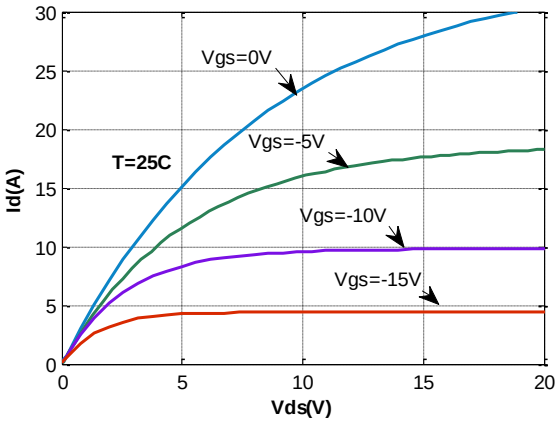

Fig. 27. Simulated forward characteristics of the SiC JFET.

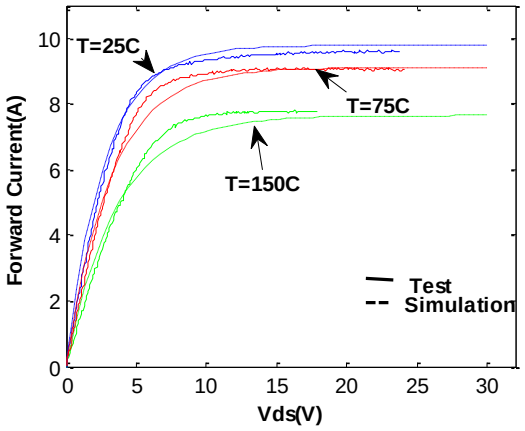

Fig. 28. Comparison of simulation and test results for forward characteristics at various temperatures and −10 V Vgs.

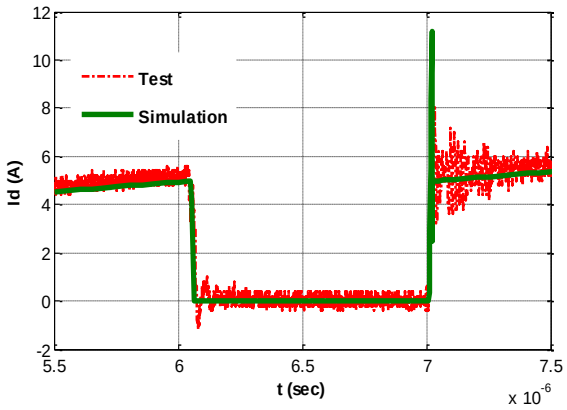

Fig. 29. Comparison of current waveforms of the JFET.

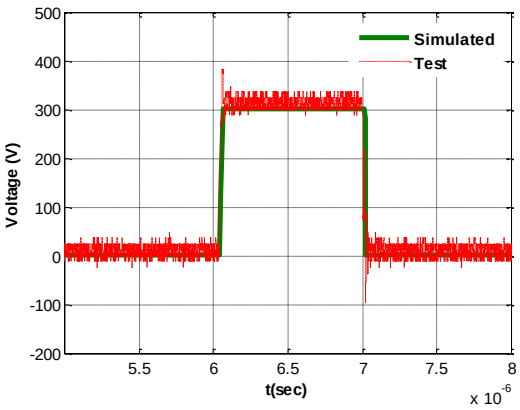

Fig. 30. Comparison of voltage waveforms of the JFET.

Conclusion

Several new SiC JFETs, MOSFETs, Schottky diodes, and JBS diodes were acquired, tested, and modeled. The traction drive model was sucessfully completed and the simulation results for the SiC inverter, developed based on 1,200 V, 100 A, SiC MOSFET testing, were presented. A behavioral SPICE model of a 1,200 V, 10 A, normally on SiC JFET was developed by obtaining the critical model parameters from testing the device. The SPICE model was validated with the actual test data.

Publications

1. M. S. Chinthavali, et al., "High Power SiC Modules for HEVs and PHEVs," IEEE International Power Electronics Conference 2010 (IPEC), June 21–24, 2010, Sapporo, Japan.
2. M. S. Chinthavali, P. J. Otaduy, and B. Ozpineci, "Performance Comparison Study of SiC and Si Technology for an IPM Drive System," International Conference on Silicon Carbide and Related Materials (ICSCRM) 2009, October 11–16, 2009, Nurnberg, Germany.

References

1. B. Ozpineci, et al., "Effects of Silicon Carbide (SiC) Power Devices on PWM Inverter Losses," *The 27th Annual Conference of the IEEE Industrial Electronics Society*, November 29–December 2, 2002, Denver, Colorado, pp. 1061–1066.
2. http://siced.com/download/CY11cb9072X1225e4d14d8X3eae/JFET_INF06_1200V_V1a.lib.

2.2 Direct Water-Cooled Power Electronics Substrate Packaging

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Objectives

- Achieve a reduction in the size and weight of power electronic inverters while operating with a high temperature coolant.
  - — Volume reduction—the proposed ORNL structure allows for the maximum cooling surface area to be used within the smallest geometrical volume.
  - — Weight savings—Weight reduction of about 17% as compared to the 2007 Toyota Camry by the removal of the traditional baseplate and heat sink.
- Achieve system cost reductions through
  - — elimination of auxiliary cooling loop,
  - — removal of the baseplate and heat sink, and
  - — use of silicon switches with high temperature coolant.
- Achieve a reliable substrate design while using 105°C water-ethylene glycol (WEG) coolant.

Approach

The strategy of this research effort was to reduce the size and weight of the power electronic inverter by

- directly cooling the substrate package,
- eliminating the cold plate and the heat spreader, and
- removing the thermal interface material (TIM).

Major Accomplishments

- Completed metallization of the second generation ceramic substrate.
- Evaluated metallization, which was shown to have excellent bond strength.
- Selected and fabricated an octagonal design containing eight coolant channels. This design produced the following results.
  - — Inverter design volume of 3.6 L.
  - — Coolant temperature of 105°C WEG with a copper cladding thickness of 0.012 in.
  - — Projected power density of 15 kW/L.
  - — Maximum steady state temperatures for 30 kW continuous loads as follows.
    - ► Insulated gate bipolar transistor (IGBT)—164.5°C
    - ► Diode—154.2°C
    - ► Coolant fluid—127.8°C

- Completed flow header finite element analysis (FEA) and achieved a balanced coolant flow design to supply the substrates.
- Optimized buss structures within the design inverter performance.

Future Direction

- This project will conclude in FY 2010.

Technical Discussion

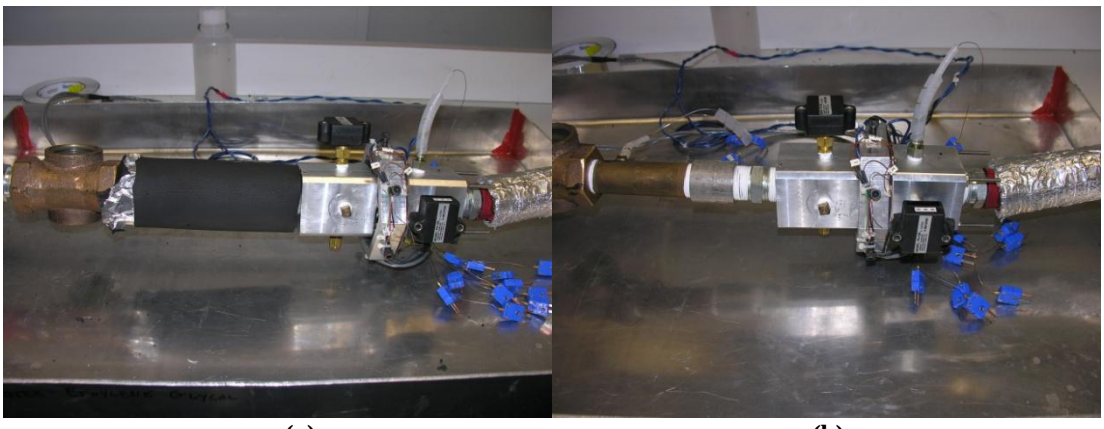
The scope of this project for FY 2010 was to complete the second generation half leg module and test this module's copper plating process. The testing results were then compared to the final FEA results to see whether any improvement in thermal conductivity was achieved with the new plating. Additionally, the complete inverter design was to be finalized, including any module modifications that may have been required, and the necessary components for a complete inverter package fabricated.

Component fabrication consisted of fabricating the alumina substrates; having the substrates metalized, plated, and chips sintered/soldered into position; and wire bonding the completed module. The gate cards and their associated hardware were to be designed and fabricated. The capacitor with its specific direct current (dc) connection points was to be fabricated, and the flow headers and any additional miscellaneous components were to be completed this year.

Completing and Testing Second Generation Module

The second generation half lag module was completed using the new copper plating process. To ensure consistency between FY 2009 and FY 2010 test and model validation, the setup contained power resistors just as in FY 2009. Figures 1 and 2 show the several layers of insulation material and how this insulation was built up, in stages, to isolate the module from the outside environment.

Figure 3 shows the assembled module and the new configuration of the thermocouples. A groove the same size as the diameter of the thermocouple was cut in the ceramic base of the power resistor. Once the thermocouples were installed in this groove, the resistors were then installed in position on the module holder. This assembled configuration provided a more accurate junction temperature reading between the power resistor and the copper base.



(a) **(b)**

Fig. 1. Beginning (a) and intermediate (b) stages of module insulation.

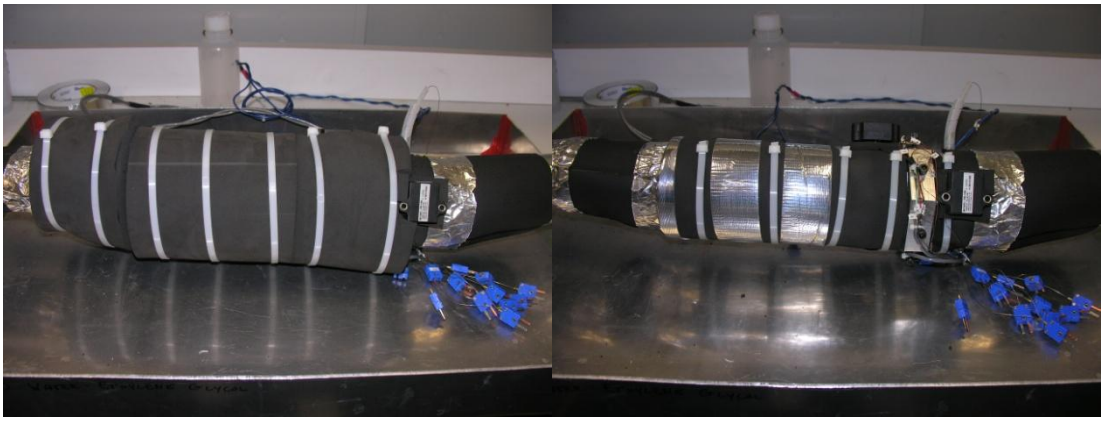
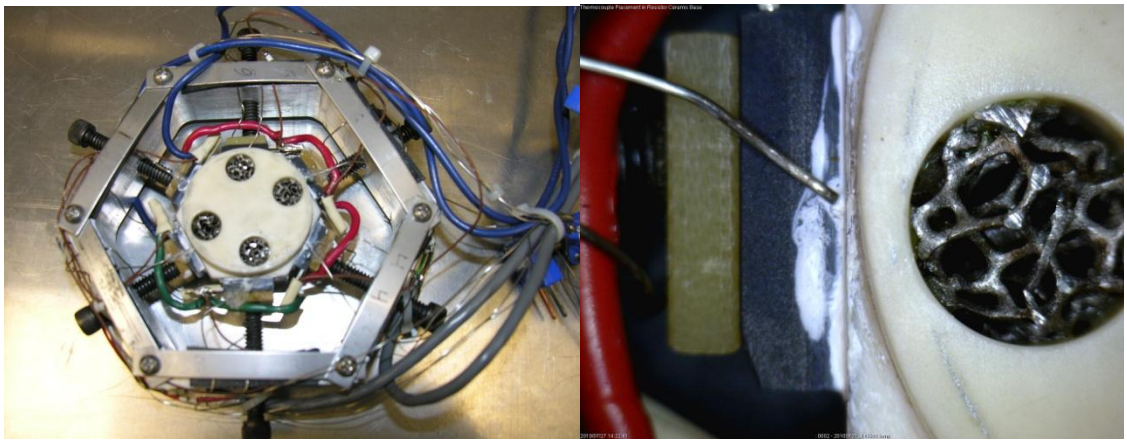


Fig. 2. Final stages of module insulation.



(a) **(b)**

Fig. 3. Assembled module (a) and new configuration of the thermocouples (b).

Figure 4 shows the FEA output for the four-hole design and the locations where the temperature data were taken. As stated previously, the power resistors contained a thermocouple groove cut into the ceramic base for installation of the thermocouple. This placed the measurement device at the closest point to the junction temperature as possible. Table 1 shows a comparison of the test data to the FEA data with the results matching within a 10–15% margin of error.

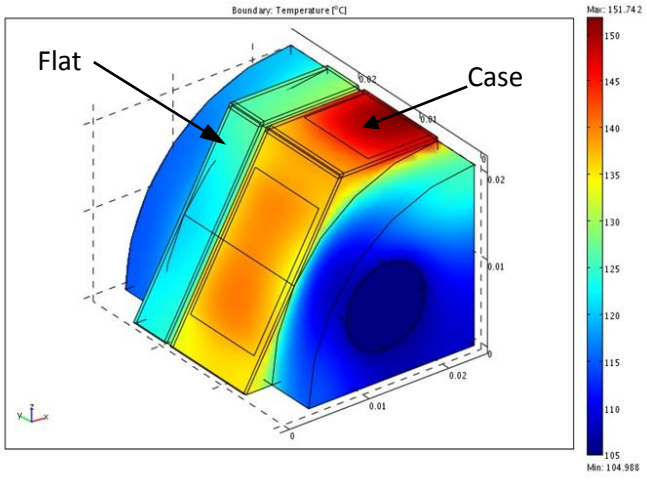


Fig. 4. FEA output for four-hole design.

Finalizing Design Requirements for a Complete Inverter

Results from FY 2009 tests indicated that IGBT and diode temperatures would only rise between 2° and 3°C when operated at the peak performance values of 55 kW from the steady state performance value of 30 kW for 18 s. Taking into account this temperature rise information, a two-

chip-deep octagonal substrate design was produced and FEA results obtained. This design required fewer ceramic modules, produced a more compact design, and allowed for minimal buss connection points. Each octagonal module could operate as a phase of the three phase system; thus the final design only needed three modules. This two-chip-deep octagonal design contained eight coolant channels, each channel located directly under the chips. This arrangement provided the best cooling structure for chip heat dissipation.

Table 1. Comparison of Experimental and Simulated Data for Four-Hole Structure

Nominal inlet temperature (°C)	Electrical power (W)	Heat added to fluid (W)	Results	Average case temperature (°C)	Average flat temperature (°C)
50	331.3	250	Experimental	72.3	37.5
			COMSOL[a]	63.5	32.6
			Error	-12.20%	-13.10%
75	332.25	253.3	Experimental	73.6	35.6
			COMSOL	62.8	30.5
			Error	-14.60%	-14.30%
90	294.9	238.8	Experimental	68.9	29.9
			COMSOL	59.2	25.9
			Error	-14.10%	-13.50%
105	210.4	186.5	Experimental	43.9	21.5
			COMSOL	39.1	19.1
			Error	-10.90%	-11.20%

[a]Simulation software used.

The inverter volume was projected to be 3.6 L with this design. Using a WEG coolant temperature of 105°C and a copper cladding thickness of 0.012 in., the design was projected to achieve a power density of 15 kW/L. This meets the 2020 FreedomCAR target. The maximum steady state temperatures for 30 kW continuous loads were as follows.

- IGBT—164.5°C
- Diode—154.2°C
- Coolant fluid—127.8°C

Figure 5 shows the FEA results for the simulated octagonal module. Figure 6 is an exploded view showing all of the components specified for the Direct Water-Cooled Power Electronics Substrate Inverter Package.

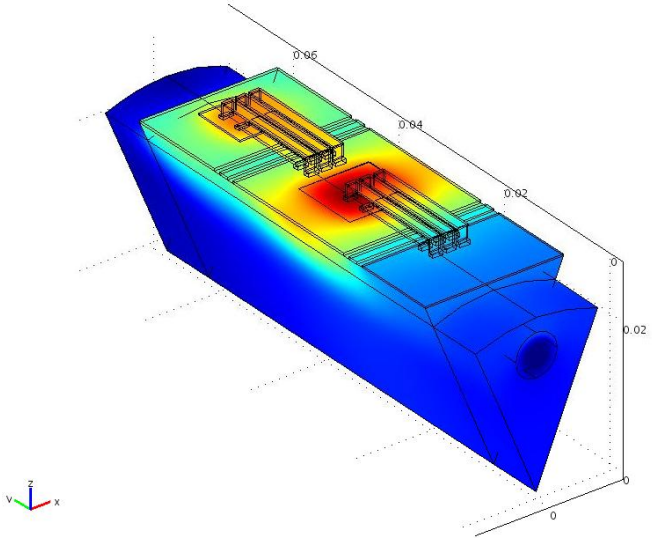


Fig. 5. FEA results of the simulated octagonal model.

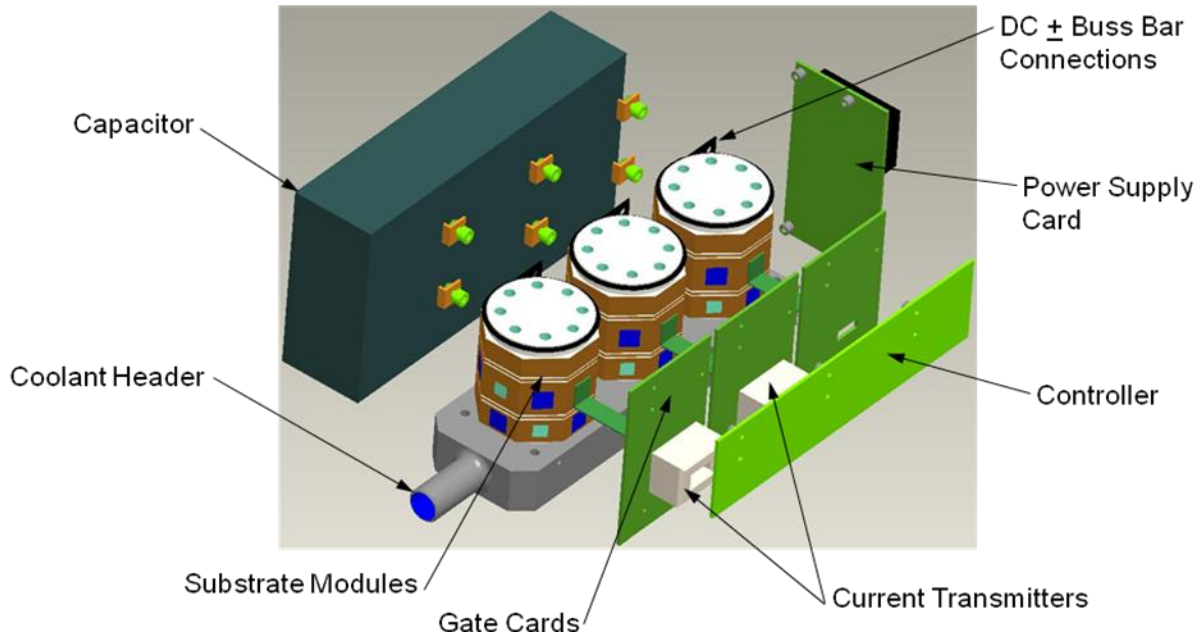


Fig. 6. Exploded view of complete Direct Water-Cooled Power Electronics Substrate Inverter Package (upper coolant header removed for clarity).

3. FABRICATION OF INVERTER COMPONENTS

To evaluate the copper to alumina substrate bond, one of the alumina four-hole substrates was sent to Stellar Industries, Inc., to be copper plated. This process involves plating the part with molybdenum/manganese and firing at a high temperature so the molybdenum/manganese bonds molecularly with the alumina. Then this surface can be plated with copper for an extremely intimate bond between the copper and the alumina substrate. Once a test piece was received from Stellar Industries, the substrate was sectioned and polished so the bond area between the copper and the alumina could be

evaluated under an electron microscope. Figure 7 shows the sectioned part, and Fig. 8 shows the bond area. The plating process used by Stellar Industries produces an excellent bond area, free of voids.

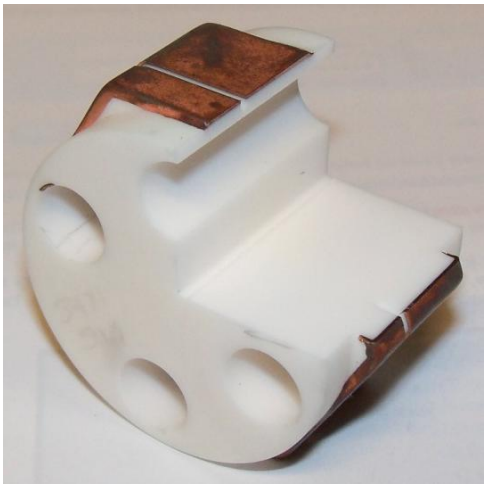


Fig. 7. Sectioned part used for copper bond evaluation.

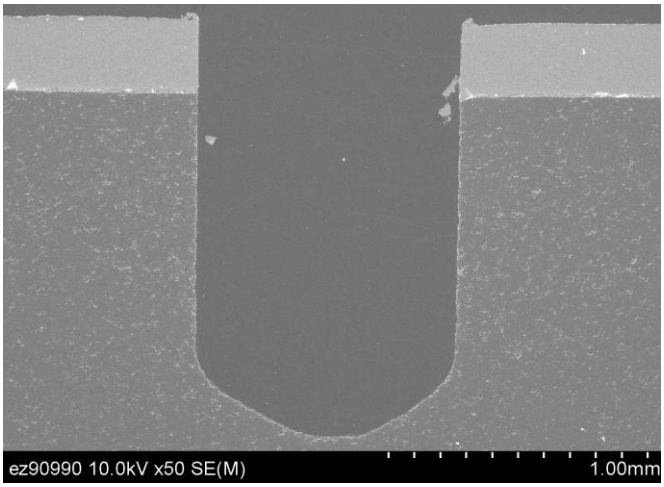


Fig. 8. Magnified bond area shows an excellent bond between the alumina and copper.

After the initial copper plating evaluation, fabrication of the octagonal alumina substrates was completed by CoorsTek, Inc. The parts were initially produced as green parts, rough machined to shape, and fired to their final densification. After firing, the parts were machined to their final dimensional shape. The octagonal flats were checked for flatness, and all parts met the required specification. Figure 9 shows the finished alumina octagonal substrate.

Fig. 9. Finished alumina octagonal substrate fabricated by CoorsTek.

The finished octagonal substrates were shipped to Stellar Industries to be copper plated. Figure 10 shows a final component bonded with copper.

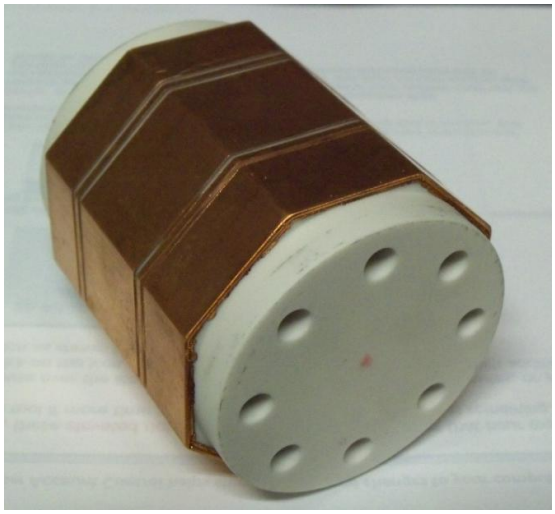


Fig. 10. Final component bonded with copper by Stellar Industries.

Before plating, Stellar Industries performed a dye penetrant test on the substrates to determine the integrity of the parts. This was done to ensure that the parts could withstand high temperature firing without failure. Some of the parts were determined to have fine stress cracks that could possibly affect them during the plating process. Figure 11 shows the cracks revealed by the dye penetrant test.

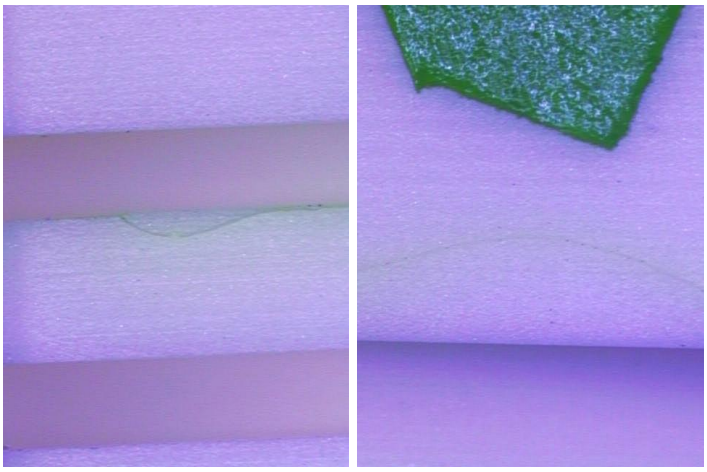


Fig. 11. Cracks revealed by dye penetrant testing.

CoorsTek was contacted concerning the nature of these stress cracks and indicated that the final firing process combined with the final machining process could have produced these fine stress cracks. The CoorsTek process of firing to a final densification of the octagonal substrate and final machining process can be modified to eliminate this problem.

However based on this experience, it was necessary to ensure that if some of the substrates developed fine stress cracks during high volume manufacturing, the plating process would not cause the cracks to propagate to the point of substrate failure. Therefore, the copper plating process was applied to one of the stress cracked parts to determine whether the crack in the substrate would be affected by the high temperature firings of the plating process. Upon completion of the plating process, it was determined that the high temperature firing process had no detrimental effect on the cracked component.

Fig. 12. Nickel-/silver-plated part with IGBTs and diodes sintered into position.

Once the copper plated octagonal structures were received from Stellar Industries, the modules were shipped to NBE Technologies, LLC, to be plated with nickel/silver and then have the IGBTs and diodes sintered into position. Figure 12 shows one of the completed modules. The IGBTs and diodes have been sintered into position and are ready for wire bonding. Also note that the dc connection tabs have been soldered into position.

Flow headers were designed to be multifunctional. The primary purpose of the headers was to be the transport medium for the WEG coolant. The headers also provide structural support for the inverter assembly, the gate cards, the control card, and the power supply card. An FEA analysis was performed on the flow header to ensure a balanced flow between the three supply areas for each of the three modules. Figure 13 shows the balanced FEA result.

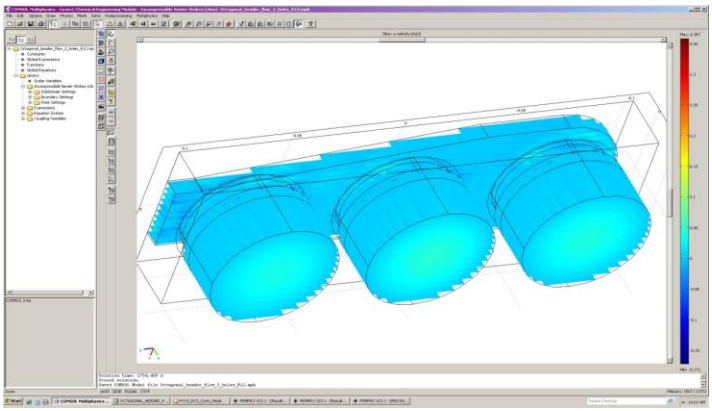


Fig. 13. FEA results of header flow analysis showing a balanced flow.

A flow test was completed and the flow measured between the three output areas to confirm that the flow was balanced. A slight modification was needed to the first flow output area to bring it into balance with the middle and last output area. Figure 14 shows the completed header assembly with the cover removed so the internal flow output areas can be seen. Figure 15 shows the assembly buildup as of September 24, 2010.

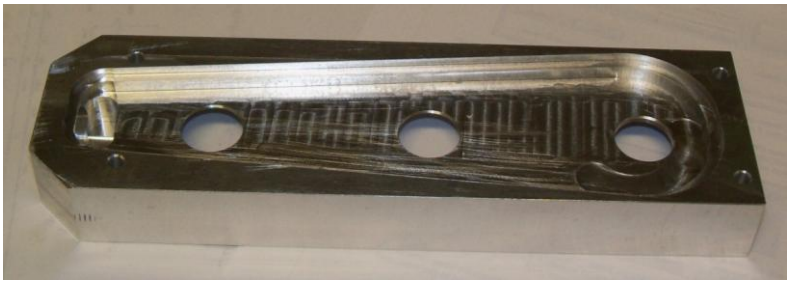


Fig. 14. Inverter flow header.

Fig. 15. Inverter assembly buildup as of September 24, 2010 (top flow header removed).

Gate cards were designed to fit within the dimensional specifications necessary to ensure a compact overall volume as well as the electrical requirements for use in high temperature environments. The gate drive board design is capable of driving three 200 A IGBT dies in parallel and plugs directly into the

digital signal processing controller. Figure 16 shows a completed gate drive board which has been populated with the necessary components for high temperature operation.

Fig. 16. Completed gate drive board.

Capacitors necessary to complete the inverter build were fabricated by Electronic Concepts, Inc., in Eatontown, New Jersey. The capacitors were built to a specification of 600 µF and 500 Vdc. The dc connection tabs were specifically placed so it would bolt directly to the tabs on the modules and still remain within the specified volume of the design. Figure 17 shows a completed capacitor.

Fig. 17. Completed capacitor from Electronic Concepts.

Conclusion

The Direct Water-Cooled Power Electronics Substrate Packaging concept developed at ORNL substantially improves upon the established packaging concepts used today through the following.

- Elimination of the auxiliary cooling loop, resulting in a system cost savings of $175.00.
- Removal of the baseplate and heat sink.
- Use of silicon switches with high temperature (105°C) coolant.
- Removal of the TIM or thermal grease, which vastly improves waste heat removal in the system.
- Elimination of the copper baseplate and the aluminum heat exchanger, which results in additional weight, volume, and cost savings.
- Flowing coolant directly through the ceramic substrate, which delivers cooling more directly to the semiconductor dies.

This innovative design and thermal stack reduction is expected to achieve higher inverter power densities and significantly reduce system costs. Results from this program indicate that a 175°C rated silicon IGBT

could work using 105°C WEG coolant. The current design also shows the potential to exceed the 2020 FreedomCAR target of 14.1 kW/kg with the use of 105°C coolant.

Patents

1. R. H. Wiles, et al., *Direct Cooled Power Electronics Substrate,* U.S. Patent 7796388, awarded on September 14, 2010.

2.3 High Temperature, High Voltage Fully Integrated Gate Driver Circuit

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Objectives

- Increase the current drive of the preceding high temperature gate driver circuit design.
- Improve the gate driver design to make it more robust against temperature variation.
- Enhance some gate driver circuitry to improve functionality [e.g., voltage regulator, undervoltage lockout (UVLO)].
- Incorporate additional protective features with the core gate driver circuit (e.g., desaturation detection and gate current monitoring circuitry).
- Integrate a charge pump with the core gate driver to enable a 100% high-side duty cycle.
- Include a low voltage differential signaling (LVDS) circuit.
- Design input-isolation test circuitry as a step toward an input-isolation solution.
- Move all capacitors necessary for full functionality on-chip.
- Rework gate driver layout to increase space use and reliability.

Approach

- Make as much use of the bipolar complementary metal-oxide semiconductor–double diffused metal-oxide semiconductor (DMOS) on silicon-on-insulator (SOI) process features to optimize the gate driver design for high ambient temperature operation.
- Test different types of wide bandgap semiconductor power switches with the driver circuit.

Major Accomplishments

- Designed and sent the fourth generation (Corinth) gate driver circuit for fabrication.
- Made refinements to the LM723 based voltage regulator.
- Integrated the charge pump with the core gate driver.
- Incorporated desaturation detection and gate current monitoring circuitry in the gate driver chip.
- Designed input-isolation test circuitry and placed on the chip.
- Integrated LVDS circuit with the gate driver.
- Integrated capacitors on-chip.
- Reworked gate driver layout.

Future Direction

- Use results from Corinth to improve the gate driver design, if necessary.
- Develop an input-isolation solution.

- Integrate the gate driver with WBG power switches in a smart power module.
- Work with industry to achieve product commercialization.

Technical Discussion

The goal of this project is to develop an SOI based high temperature, high voltage gate driver integrated circuit with high drive current capability for WBG power switches, such as silicon carbide (SiC) and gallium nitride (GaN). Power electronics in future electric vehicles (hybrid, plug-in hybrid, and full electric) are expected to use WBG based power devices which are capable of working at much higher ambient temperatures than the conventional silicon based power switches. Implementation of WBG based power modules in automotives will allow the use of air cooling for electronics under the hood. To obtain the full advantage of the high temperature capability of WBG devices, the associated control electronics (such as gate driver circuits) also need to operate at higher temperatures with minimal thermal management. By placing the gate driver circuit close to the power switches, system reliability as well as performance can be improved.

Third Generation Gate Driver Measurement Results

Figure 1 shows the test setup used for characterizing the prototype third generation (3G) gate driver chips. A polyimide test board with the gate driver chip was placed inside the environmental chamber. Chamber temperature was varied to test the gate driver circuit at different ambient temperatures. For both resistance-capacitance (R-C) load and SiC power switch tests, the actual load was kept outside the chamber. A 600 V, 16 A, direct current (dc) power supply unit was used for the SiC power switch tests.

Fig. 1. High temperature gate driver test setup.

The chip was first tested with the on-chip current limiting resistor R_G connected in series with an external 10 nF capacitive load at different ambient temperatures by placing the test board inside the temperature chamber. Figure 2 shows the 30 V peak-to-peak (–15 V to +15 V), 20 kHz, gate pulse signal generated by the chip at 200ºC ambient temperature with a nominal R_G value of 3.4 Ω. The drive current wave shape is presented in Figure 2. At 200°C, the peak sourcing and sinking currents were 2.5 A and 2.2 A, respectively.

Figure 3 presents the measured source and sink current peaks at different ambient temperatures for three different integrated circuits (ICs) with the same R-C load (R_G = 3.4 Ω and C =10 nF). Small chip-to-chip variations in drive current were observed.

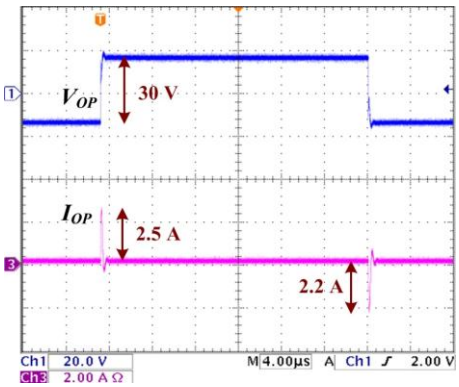

Fig. 2. R-C load test results at 200°C with R_G =3.4 Ω and C_{Load} = 10 nF.

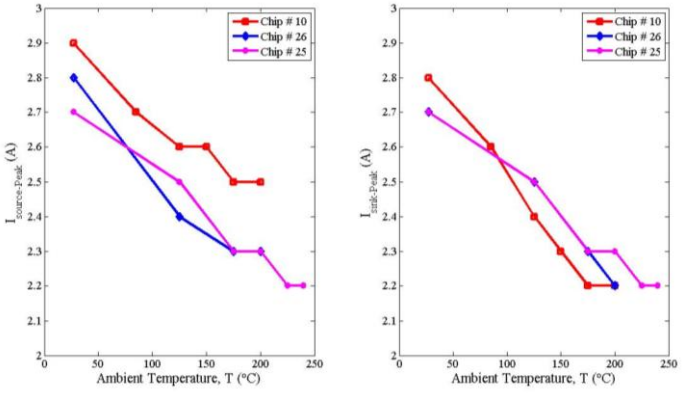

Fig. 3. Measured source and sink current peaks at different ambient temperatures for three different ICs with same R-C load (R_G= 3.4 Ω and C=10 nF).

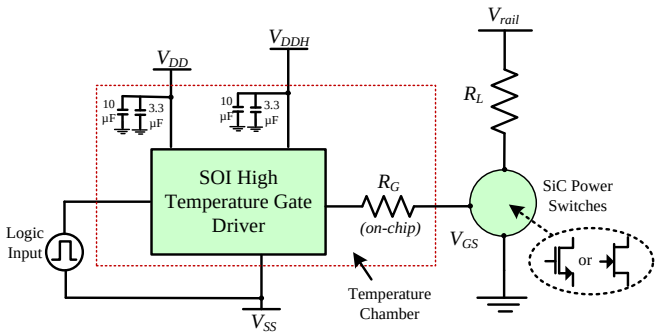

Fig. 4. Schematic of test setup for MOSFET (VDDH = 15 V, VSS = −5 V) and for normally ON JFET module (VDDH = 3 V, VSS = −5 V).

A SiC powered metal-oxide semiconductor field-effect transistor (MOSFET) (1,200 V, 10 A) prototype device developed by Cree was tested with this gate driver chip. An 80 Ω, 250 W load resistor (in series with the drain terminal) was used with the SiC MOSFET in a common-source configuration. Figure 4 shows the test connection for the SiC powered MOSFET test with the gate driver circuit.

Rail voltage was set at 560 V using a 600 V, 16 A, dc power supply. A 7 A peak load current was passed through the MOSFET when it was turned "ON" by the gate driver chip. A 20 V peak-to-peak (+15 V to −5 V) drive signal was applied to the gate terminal of the SiC MOSFET through the 3.4 Ω on-chip current limiting resistor (R_G). The test board was placed inside the temperature chamber, and the SiC MOSFET was kept outside the chamber as it was not packaged for high temperature applications. Starting from room temperature, the chip was tested up to 200ºC. Switching frequency was set at 20 kHz, and the duty cycle was 5%.

Figure 5 shows the gate voltage (pink), MOSFET drain terminal voltage (blue), and load current (cyan) waveforms at 200°C. The temperature of the chamber was raised from room temperature to 200°C in three steps (27°C, 125°C, and 200°C). The ringing effect observed in the wave shapes was due to the added parasitic inductances of the connection wires that ran from inside the temperature chamber to the outside load. A 10% to 90% rise time and a 90% to 10% fall time for both the gate drive voltage signals and the MOSFET drain voltage at each temperature level are recorded in Table 1. These readings show that this high temperature gate driver circuit maintains a fairly constant driving strength over the entire test temperature range.

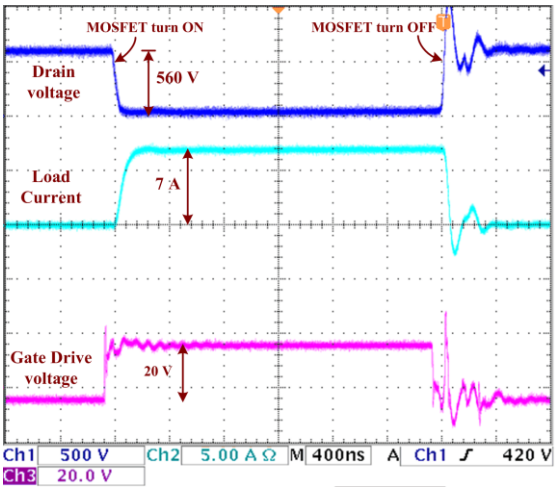

Fig. 5. Prototype circuit's test results at 200°C when driving a 1200 V, 10 A, SiC MOSFET.

Table 1. Rise Time and Fall Time at Different Ambient Temperatures

Ambient temperature (°C)	Drain voltage (V_{DS})		Gate voltage (V_{GS})	
	t_{rise} (ns)	t_{fall} (ns)	t_{rise} (ns)	t_{fall} (ns)
27	15.7	33.4	2.8	3.6
125	15.7	35.1	3.1	4.0
200	20.2	41.0	4.0	5.6

The prototype high temperature gate driver IC was also tested with an SiC normally "ON" junction field-effect transistor (JFET) (1,200 V, 50 A) power module developed by Microsemi using SemiSouth's normally "ON" SiC JFET. A gate driver circuit was biased to generate an 8 V peak-to-peak (−5 V to

+3 V) gate signal to control the JFET module which was connected to a 560 V rail voltage through an 80 Ω load resistor. Figure 6 shows the test result at 200°C ambient temperature with 1 kHz switching frequency.

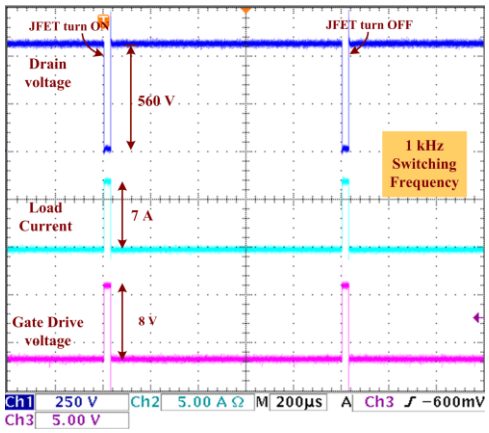

Fig. 6. SiC normally ON JFET module (1200 V, 50 A) test results.

The wide temperature on-chip voltage regulator exceeds the operating range and temperature stability performance of commercially available voltage regulators, including the LM723 Zener reference based voltage regulator design upon which it is based. The measured parabolic temperature curve of the new SOI voltage regulator indicates minimal output voltage variation over the entire temperature range thanks to the reference voltage temperature compensation scheme used in this design. The voltage regulator is capable of operating in environments up to 250°C. The regulated voltage over temperature is shown in Fig. 7.

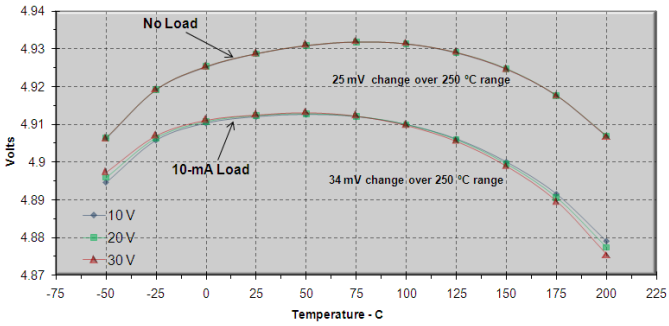

Fig. 7. Regulated voltage over temperature.

This 3G gate driver also contained several protection circuits that will send a fault signal to the gate driver logic if operational boundaries are exceeded. These circuits included a temperature sensor, UVLO circuit, and short circuit protection (SCP) circuit. The temperature sensor is designed to have nearly zero quiescent power loss until it approaches high temperature, unlike traditional sensors that have nearly constant power dissipation over temperature [1]. Several temperature cycles were carried out to measure the upper and lower triggering temperatures for this sensor circuit. Figure 8 shows the results of these temperature cycle tests for several chips.

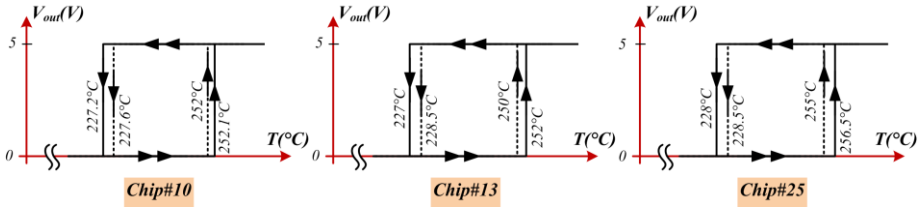

Fig. 8. Temperature sensor output in response to temperature cycling.

The SCP circuit measures the current through the power device driven by the gate driver and sends a fault if this value exceeds the limits set by the user. Figure 9 demonstrates the SCP circuit in action at 175°C detecting a high current event and sending a fault signal and recovery from the fault. After detecting a high current incident, the SCP shunts voltage from the gate of the power device to reduce the fault current before sending the fault signal that deactivates the gate driver.

(a) **(b)**

Fig. 9. SCP test results at 175°C of current fault: (a) fault "ON"; (b) fault "OFF."

The UVLO circuit monitors the supply (VDD and VDDH) power rails and sends a fault signal if they drop below 10% of their rated value. Figure 10 shows measurement results at 200°C for the 5 V power rail switching between undervoltage and nominal voltage conditions.

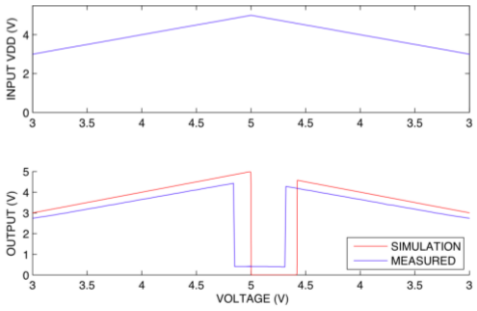

Fig. 10. UVLO detecting an undervoltage at 200°C on the 5 V rail.

Fourth Generation (Corinth) Gate Driver

Circuit design, simulation, layout, post-layout simulation, and submission for fabrication for the Corinth gate driver circuit have been completed. Figure 11 shows the block diagram schematic of the Corinth gate driver circuit. Compared to earlier prototypes, this version of the gate driver comprises several modifications and improvements in the core driver circuit.

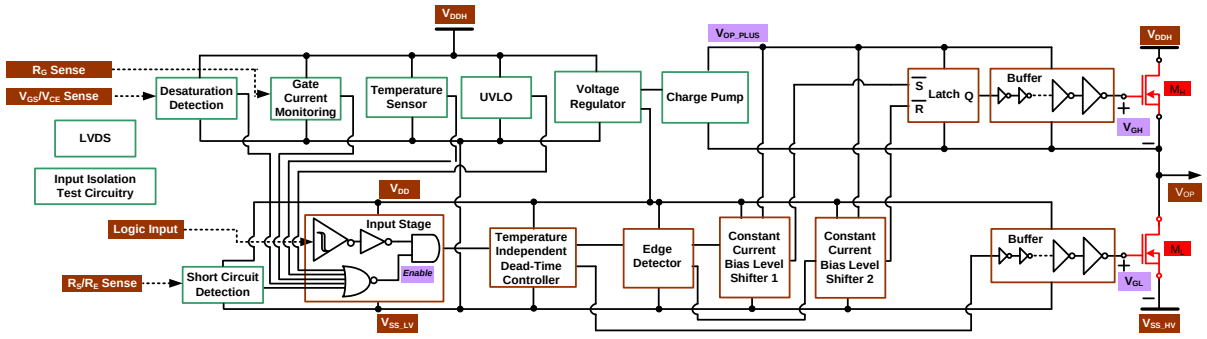

Fig. 11. Block diagram of Corinth.

Charge Pump

The charge pump was designed to replace the bootstrap capacitor and diode used in previous revisions of the gate driver. The bootstrap circuit was used to provide a 5 V floating supply rail to power the high-side circuitry that drives the current sourcing output transistor, M_H. It necessitated periodically turning the gate driver output "OFF" to allow the bootstrap capacitor to recharge. This effectively limited the lower frequency bound for the operation of the gate driver to no less than 1 kHz for reliable operation.

The charge pump in Fig. 12, based on [2], removes the recharge cycle limitation by providing charge independent of the gate driver's switching state. This is accomplished by continually refreshing the charge of capacitor C2. A logic signal, V_{SWITCH}, drives switches S1 and S2. When this signal is high, S1 is "ON," allowing current to flow through diode D1 and charging the boost capacitor C1. At the same time S2 is "ON," maintaining switch S3 in an "OFF" state. When switches S1 and S2 are turned "OFF," the charge on capacitor C1 begins to charge the gate of switch S3 through resistor R1, eventually activating switch S2. With switch S2 "ON," capacitor C1 is connected to C2, and charge is exchanged. When switches S1 and S2 are activated again, switch S3 is pulled low and deactivated, while capacitor C1 is again placed in charging mode. With continuous cycling, based on the logic control signal V_{SWITCH}, charge is maintained on capacitor C2, and power is constantly available to the high-side circuitry of the gate driver, allowing for 100% high-side duty cycle operation.

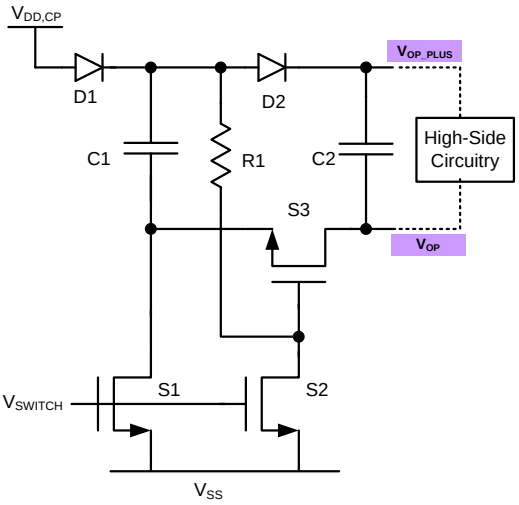

Fig. 12. Basic charge pump schematic.

$V_{DD,CP}$, the power supply used to charge capacitor C1, is supplied by a version of the voltage regulator modified to provide a particular voltage curve of 6.7 V to 6.2 V across 27°C to 200°C. This is done to offset the change in the diode's voltage drop for the same temperature range and allow for a supply voltage of about 5 V to be available to the high-side circuitry for the entire temperature range.

Output Drivers

As observed in Fig. 3, showing test results from the 3G gate driver, the maximum output current drive at 200°C was not as high as expected. While drive current is greater than 2.2 A at 200°C, maximum current was expected to be about 5 A. The source of the lower current drive is believed to be related to self-heating of the output drivers. The output driver arrays were made up of eight hundred 45 V lateral DMOS devices, each on the 3G design. These devices were placed at minimum spacing from each other, which would create the worst case self-heating effects. Several steps have been taken to alleviate this condition: the devices have been spaced further apart; heat pipes (metal traces tied to ground and pads) were added to help remove heat from the output driver area of the chip; and wider metal traces were used for all high current wires (and elsewhere where possible), as shown in Fig. 13.

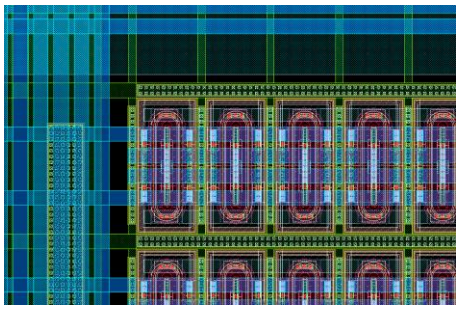

Fig. 13. Corner of output driver on Corinth.

Voltage Regulator

The Corinth voltage regulator design implements the same basic LM723 topology seen in the 3G voltage regulator [3]. The impressive temperature performance and supply rejection found in the 3G design is once again used while 3G test data allow for significant design improvements. The most significant improvements of the Corinth voltage regulator result from modifications to the operational amplifier output stage. As seen in Fig. 14, the output stage of the Corinth voltage regulator has been implemented as a class-AB source follower. The class-AB output stage significantly reduces the output impedance and allows for symmetrical sinking and sourcing of output current. An output capacitor is used to supply load

current during transient events, as these load transients greatly exceed the bandwidth of the op-amp (operational amplifier). To ensure the pole generated by the output capacitor occurs beyond the unity-gain frequency, the output stage requires a low output impedance and therefore a large quiescent current (about 2 mA). With this arrangement, the output capacitor of the voltage regulator is able to supply charge to the gate driver circuits during load current transients without inducing instability.

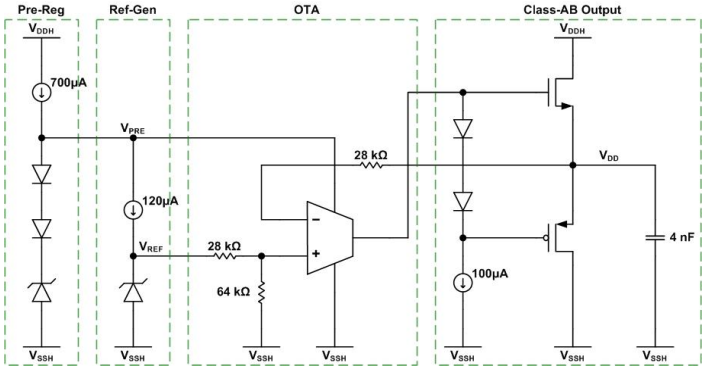

Fig. 14. Voltage regulator topology.

The preregulator and reference generator of the Corinth voltage regulator are relatively unchanged with only slight changes in biasing and temperature compensation schemes to accommodate the changes made in the op-amp design. The Corinth voltage regulator also improves on the offset voltage found in the 3G voltage regulator. Because device matching is impossible for laterally-diffused bipolar junction transistor (BJT) devices, the bias point of the differential input pair is set to minimize the effects of input bias current at the output. Figure 15 shows a simulation of the voltage regulator's output voltage for the fully integrated gate driver during a transient event, the switching of the gate driver output. The output of the voltage regulator is maintained within 125 mV of the nominal value during all transient events. This modest variation in output voltage is within the requirements of the gate driver circuits and allows for reliable operation without the requirement of an external capacitor.

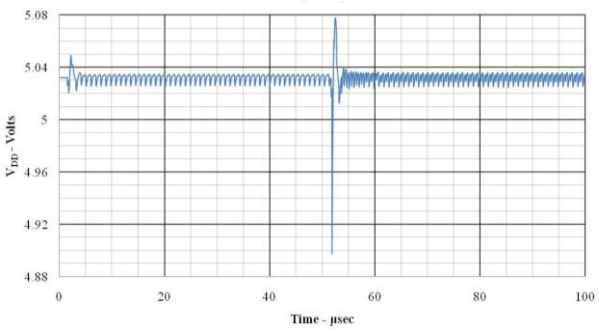

Fig. 15. Corinth voltage regulator transient event simulation.

Undervoltage Lockout

The integrated UVLO circuit used in the gate driver monitors V_{DDH}–V_{SSH} and provides an enable signal when usable supply voltages are available. The Corinth UVLO uses a current-sourced Zener diode to provide the reference voltage for the UVLO comparator, shown in Fig. 16. This reference voltage is compared to resistively-divided V_{DDH}–V_{SSH}, where the resistors R_1 and R_2 are set according to the value of V_{DDH}–V_{SSH} via external jumpers. The 3G UVLO used a resistively loaded Zener diode reference that failed due to large diode currents. In addition to providing a more robust architecture, the reference circuit used in the Corinth UVLO provides improved supply rejection for more accurate UVLO performance [4].

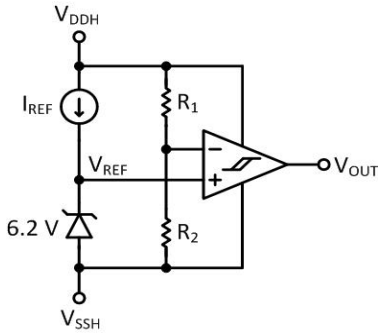

Fig. 16. UVLO topology.

Low Voltage Differential Signaling Receiver

The Corinth gate driver circuit is designed to allow the use of LVDS for input signal transmission. This signaling method provides low noise, high speed signaling capabilities to increase reliability of gate

driver operation. To properly use LVDS, the Corinth chip requires an on-chip LVDS receiver circuit (Fig. 17) to convert the LVDS signal into a usable single ended 5 V signal.

This circuit design consists of a positive feedback decision circuit (M5–M8), an output buffer (M9–M12), and two inverter stages (M13–M16). The decision circuit inherently incorporates hysteresis into the threshold characteristic of the LVDS receiver. This hysteresis aids in reducing the effects of differential and common-mode noise injected into the input signal. The LVDS input signal is a 350 mV_{p-p} square wave with a 1.25 V common-mode voltage. Figure 18 shows the LVDS receiver simulation performance for a 1 MHz input signal with a 10 pF load capacitance. Simulations over temperature reveal modest delay time changes that lie well within LVDS and Corinth requirements.

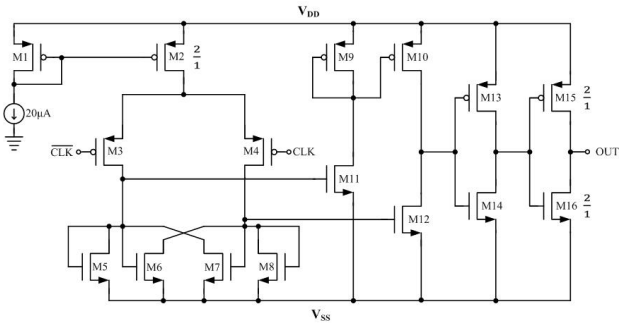

Fig. 17. Corinth LVDS receiver.

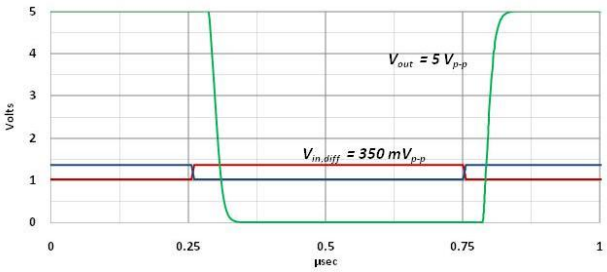

Fig. 18. Corinth LVDS receiver simulation at 200°C.

Photodetector

Among the input isolation test circuitry on Corinth is a photodetector for testing an in-package optical isolation approach using an on-chip photodetector and in-package light emitting diode (LED) to provide the electrical isolation required to operate the gate driver in bridge configurations (Fig. 19). To withstand the harsh temperature of the application environment an LED similar to a GaN LED will be used.

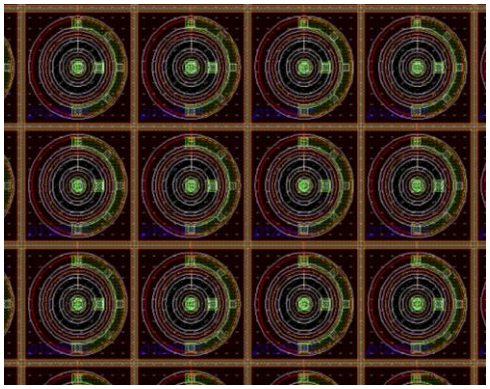

Fig. 19. Array of open-base NPN BJTs.

The photodetector is composed of an array of NPN BJTs in which the photosensitive base is left open and has no electrical connection. When a photon is incident on the base, electron hole pairs generated in the reverse biased base-collector junction are swept out of the space charge region giving rise to a photocurrent. This photocurrent is injected into the base, forward biasing the base-emitter junction. This leads to normal transistor action. The photocurrent in the base is multiplied by the transistor current gain β. To increase the current driving capacity, multiple phototransistors will be used in an array configuration. The depletion region of the collector has a high carrier generation efficiency, so a metal window will be placed across the collector junctions of the transistors. The transistors are biased to operate in the forward-active region, and a current mirror will duplicate the photodetector's current across a resistor to create a detectable voltage. This configuration is shown in Fig. 20.

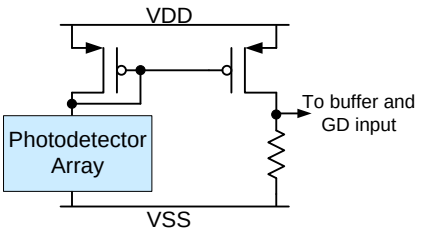

Fig. 20. Photodetector configuration.

Transformer Based Isolation Circuitry

The transformer based input isolation test circuitry is designed to give an impression of how an on-chip transformer based solution might perform. It uses an on-chip transformer to isolate the logic-level control signal from high voltage transient signals of the gate driver. Because the on-chip transformer is designed and optimized at a specific frequency, any noise at other frequencies will be decoupled from the gate driver side. Even for noise near the operating frequency of the transformer, the isolation will be significant such that the input control sections are isolated from the gate driver circuits.

The transformer based input isolation is shown in Fig. 21. It operates by modulating the input signal with the high frequency output from an oscillator. The modulated or chopped differential high frequency signal is then buffered to match the transformer's low input impedance. On the output of the transformer the signal is fed into a differential envelope detector composed of a full-wave rectifier and RC load, which is partially the parasitic impedance of the input gate of driver circuits.

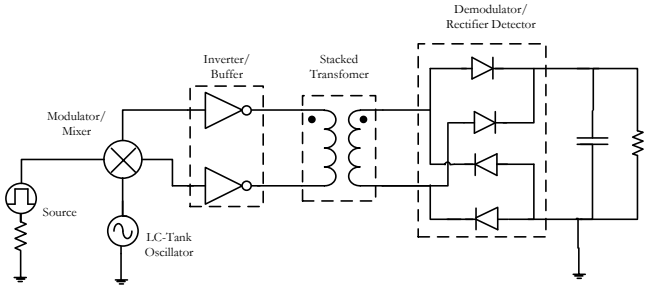

Fig. 21. Block diagram of transformer based input isolation.

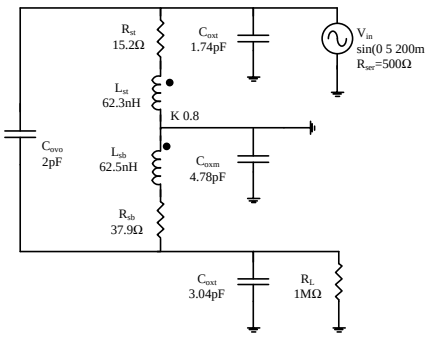

Fig. 22. Lumped analytical model for stacked transformer.

A stacked architecture was chosen for the on-chip transformer. Stacked transformers provide higher coupling efficiency but larger parasitic capacitance, which leads to a lower resonant frequency compared with planar types. However, for an operating frequency of 200 or 300 MHz, a stacked transformer with a resonant frequency of more than 1 GHz can be implemented without parasitics being a concern [5–7]. As no support for transformers is provided by the SOI process, the transformer design was accomplished by using a lumped transformer model. Based on process parameters, a stacked transformer with an outer diameter of 700 µm, 10 turns, a winding width of 20 µm, and a winding space of 2 µm was chosen. The lumped analytical model is shown in Fig. 22.

The oscillator used for generating the 200 MHz high frequency carrier signal is shown in Fig. 23. It is an LC-tank oscillator commonly used in RF circuits. One of the key components of an LC-tank oscillator is the parallel inductor and capacitor and their associated parasitic capacitance and resistance. Based on the inductors designed for the transformer, an inductor constructed for one side of the transformer with an inductance no less than 130 nH was designed. The associated series resistance, interwinding, and ground coupling capacitance are estimated following the methods used in the transformer design. The PMOS and NMOS transistors have large width-to-length ratios to facilitate the oscillation, providing strong positive feedback.

The simulation results for the complete system are shown in Fig. 24. The oscillator signal is the 200 MHz output of the LC tank. This signal is then modulated with the gate driver's input signal to produce a modulated input signal which is fed into the transformer through buffers. The output of the transformer is connected to the input of the rectifier. The rectifier's output is a close reproduction of the original input signal.

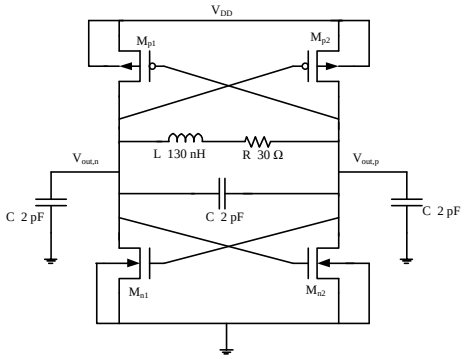

Fig. 23. LC-tank oscillator.

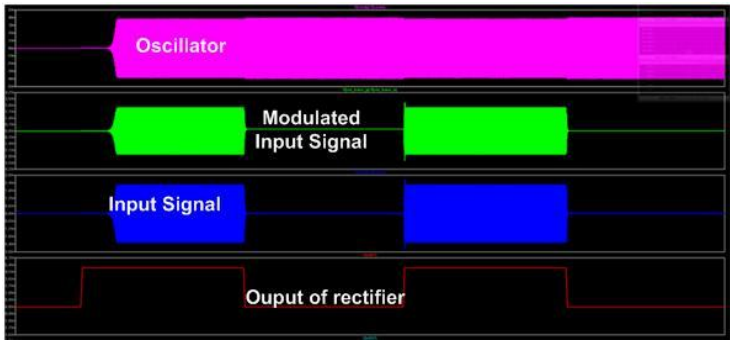

Fig. 24. Transformer based isolation simulation.

Short Circuit Protection

High temperature testing (up to 200°C) has been conducted on the 3G short circuit protection (SCP) circuit. The SCP circuit operates by monitoring the source current of the power device and sending a fault signal if the value moves beyond set parameters. The measurement results, Fig. 9, match well with simulations. In the measurements, V_{ref} is set to 400 mV, while V_{sense} is 1 Hz square wave from 0.3 V to 0.5 V. The gate driver input signal is set to 10 kHz square wave, with no load at the output.

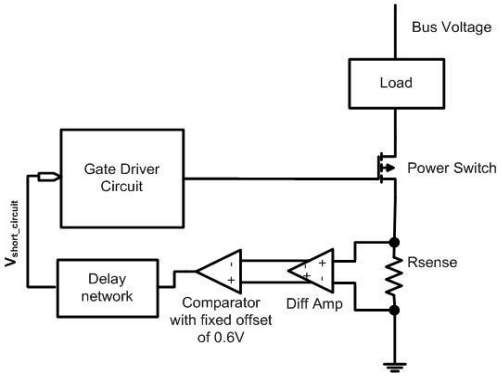

Fig. 25. Circuit diagram for SCP.

The improved Corinth version of the SCP has been altered to include a differential amplifier, Fig. 25, similar to the amplifier used in the new gate current monitoring circuitry. The amplifier helps to reduce noise from the sense resistor input signals by canceling out the common-mode noise present in the signals.

Desaturation Short Circuit Protection

Desaturation SCP is used to detect when a power switch is "ON" but is not operating within the saturation region, a high V_{CE} or V_{DS} event (a potential high or short circuit current condition). The schematic for the circuit is shown in Fig. 26. Under normal load the power switch is "ON." Diode D2 turns on with the power switch to provide Va = V_{CE} + V_{D2} and V_{C1} = [R2/(R2+R3)] × (Va − V_{D4}). Here, V_{D2} is the anode to cathode forward-bias voltage for diode D2, and V_{CE} is the voltage drop across the power switch (power switch load not shown). In this case, there is no fault signal. When a short circuit occurs, V_{CE} and Va increase due to the increase in current. As a result, C1 is charged to a higher voltage. When V_{C1} reaches V_{ref}, a fault signal is generated to shut "OFF" the power switch. The power switch will remain "OFF" until the SCP situation is removed externally.

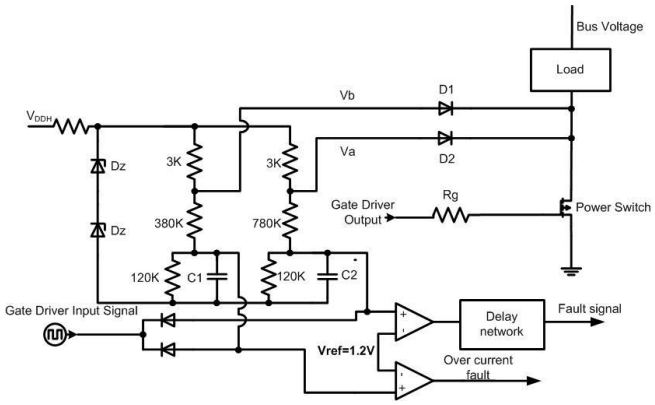

Fig. 26. Desaturation SCP.

Gate Current Monitoring

Gate current monitoring is necessary to protect the gates of the power switches. Transient gate current usually exists during the transient switching of the power devices as the gate drive quickly charges and discharges (less than 10 ns) the gate capacitance. However, under certain situations, such as a short circuit or excessive device wear, the gate current can become higher or last longer and become unsafe to the device or system. This can cause irreversible damage to the power device. Excess and continuous gate current is usually due to a short between the gate and the source while longer duration gate current is mainly due to the dielectric wear of the power device [8].

The gate current monitoring circuit, Fig. 27, uses a sense resistor placed in series with the gate resistor to detect the fault current. Any current outside of the expected range or lasting longer than expected will be detected as a fault by the circuit. It operates as follows.

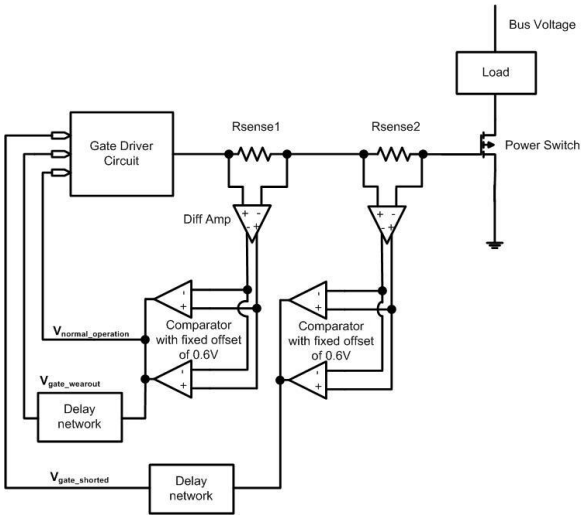

Fig. 27. Gate current monitoring.

- The gate current is converted to a voltage by the *Rsense* resistor.
- Normal switching current will be detected by reference *Vref2*; thus signal *Vnormal_operation* is sent to the gate driver core circuit.
- If the gate current lasts longer than expected, it will be detected by the delay network block and fault signal *Vgate_wearout* is sent to the gate driver circuit.
- Excess high and persistent gate current will be recognized by *Vref1* and trigger the *Vgate_shorted* signal.

Extensive simulations have been conducted across temperature as the gate driver output voltage can swing 30 V peak to peak within 10 ns. A brief look at simulation results is provided in Figs. 28 and 29, with a 30 V supply at room temperature. Figure 28 shows the normal operation of the gate driver chip as a pulse of *Vnormal_operation* is generated during each switching transient. Figure 29 illustrates both gate degradation and shorted situations where the signals *Vgate_wearout* and *Vgate_shorted*, respectively, will be triggered.

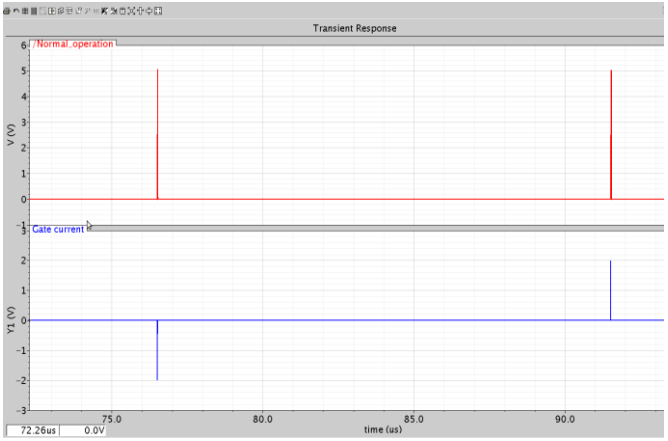

Fig. 28. Normal operation of gate driver.

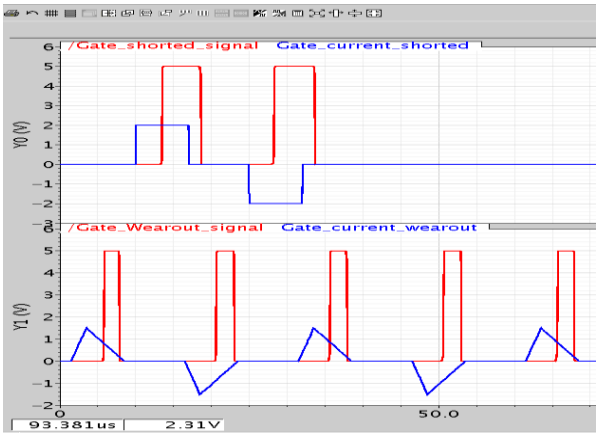

Fig. 29. Gate wear and gate shorted situation.

Conclusion

This challenging project involves the development and demonstration of a high temperature, high voltage gate driver circuit with large current sourcing/sinking capability to drive different types of WBG power switches. Successful integration of this gate driver circuit with WBG power switches will result in smart power converter modules with reduced volume and weight compared to the conventional all silicon based topologies. The 3G gate driver chip designed in 2009 has been shown to operate at 200°C with a current drive strength greater than 2.2 A at frequencies greater than 100 kHz with no active or passive cooling mechanism.

The improved version of the gate driver, Corinth, is currently being fabricated. Its enhancements include a higher output drive current, refined voltage regulator, charge pump for 100% high-side duty cycle, and LVDS circuit. The new protection features, gate current monitoring and desaturation SCP, augment the previously available on-chip circuits. Also, the input isolation test circuitry is a step toward an on-chip or in-package integrated approach to input isolation.

Publications

1. M. A. Huque, et al., "SOI-Based High-Voltage, High-Temperature Integrated Circuit Gate Driver for Sic-Based Power FETs," *IET Proceedings on Power Electronics*, Vol. 3, 2010 (in press).
2. Liang Zuo, et al., "A Universal BCD-on-SOI Based High Temperature Short Circuit Protection for SiC Power Switches," IMAPS International Conference on High Temperature Electronics (HiTEC 2010), May 11–13, 2010, Albuquerque, New Mexico.
3. Liang Zuo, et al., "A Universal SOI Based High Temperature High Voltage Gate Driver Integrated Circuit for SiC Power Switches with Short Circuit Protection," accepted for poster presentation at IEEE Lester Eastman Conference, August 3–5, 2010, Troy, New York.
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5. M. A. Huque, et al., "A High-Temperature, High-Voltage SOI Gate Driver IC with High Output Current and On-Chip Low-Power Temperature Sensor," 42nd International Symposium on Microelectronics (IMAPS 2009), November 1–5, 2009, San Jose, California.

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8. L. Chen, F.Z. Peng, and D. Cao, "A smart gate drive with self-diagnosis for power MOSFETs and IGBTs," *2008 IEEE Applied Power Electronics Conference and Exposition*, February 24–28, 2008, Austin, Texas, pp.1602–1607 (2008).

2.4 Inverter Using Current Source Topology

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Objectives

- Overall project objectives
  - Develop new Z-source current source inverter (ZCSI) topologies that combine the benefits of ORNL's current source inverter (CSI) efforts and Michigan State University's work on Z-source inverters (ZSIs) to significantly reduce cost and volume through the integration of voltage boost, inverter, regeneration (regen), and plug-in electric vehicle (PEV) charging functions.
- Objectives for FY 2010 effort
  - Perform a simulation study on selected ZCSI topologies.
  - Produce a design for a 55 kW ZCSI based on the selected topology.
  - Perform a feasibility assessment of using the ORNL voltage to current source (V-I) converter based CSI topology for hybrid electric vehicle (HEV) configurations with more than one motor.

Approach

- Use ORNL's CSI with a quasi-Z network (ZCSI) of passive components to enable
  - single stage voltage buck and boost power conversion,
  - battery charging, and
  - safe operation in open circuit events.
- Eliminate antiparallel diodes with reverse-blocking (RB) insulated gate bipolar transistors (IGBTs).
- Reduce total capacitance.
- Provide sinusoidal voltages and currents to the motor.
- Demonstrate tolerance of phase leg shoot-through conditions.
- Extend constant-power speed range without using a dc-dc boost converter.

Major Accomplishments

- Developed two new ZCSIs with a reduced component count: a current-fed trans-ZSI (CF-trans-ZSI) and a CF-trans-quasi-ZSI (CF-trans-qZSI). Simulation study indicates the new ZCSIs have a voltage boost ratio of 3 in contrast to 2 for the previous ZCSIs.
- Completed a design for a 55 kW ZCSI based on the CF-trans-qZSI using first generation RB-IGBT technology. The design yields a specific power of 4.89 kW/kg, a power density of 16.6 kW/L, and an efficiency of 93.8% in boost mode and 94% in buck mode. With next generation RB-IGBT technology, the efficiency numbers can be increased to 96% and 96.7%, respectively.
- Confirmed through simulation the feasibility of using the ORNL V-I converter based CSI topology in series and power-split series parallel HEV configurations. The CSI dual-motor-drive power

electronics (PE) using RB-IGBTs provides significant performance improvements over the 2007 Camry PE:
- — 49% increase of specific power (6.4 vs 4.3 kW/kg),
- — 60% increase of power density (9.9 vs 6.2 kW/kg), and
- — 34% reduction of cost ($15.4/kW vs $23.2/kW).

Future Direction

- Further improve the specific power and power density of the ZCSIs by reducing the size and weight of the passive components.
- Investigate by simulation and experiment performances of the two new ZCSIs for charging batteries in PEVs.
- Design, fabricate, and test a 55 kW ZCSI prototype.
- Design, build, and test a 55 kW V-I converter based CSI dual-motor-drive inverter prototype.

Technical Discussion

Background

Current electric vehicles (EVs) and HEVs use inverters that operate off a voltage source. They are called voltage source inverters or VSIs [Fig. 1(a)] because the most readily available and efficient energy storage devices, batteries, are inherently voltage sources. The VSI, however, possesses several drawbacks that make it difficult for it to meet the FreedomCAR goals for inverter volume, lifetime, and cost established by the U.S. Department of Energy and its industrial partners [1]. The VSI requires a very high performance direct current (dc) bus capacitor to maintain a near ideal voltage source and absorb the ripple current generated by the switching actions of the inverter. The root mean square (rms) value of the ripple current can reach 50% to about 80% of the motor current. Concerns about the reliability of electrolytic capacitors have forced HEV makers to use film capacitors, and currently available film capacitors that can meet the demanding requirements of this environment are costly and bulky, taking up one-third of the inverter volume and making up one-fifth of the cost. The reliability of the inverter is also limited by the capacitors and further hampered by the possible shoot-throughs of the phase legs making up a VSI [S_1–S_2, S_3–S_4, and S_5–S_6 in Fig. 1(a)]. Steep rising and falling edges of the pulse width modulated output voltage generate high *dv*/*dt* related electromagnetic-interference noises, cause motor insulation degradation due to the voltage surges resulting from these rapid voltage transitions, produce high frequency losses in the windings and cores of the motor, and generate bearing-leakage currents that erode the bearings over time. Furthermore, for the VSI to operate from a low voltage battery, a bidirectional boost converter is needed.

All these problems can be eliminated or significantly reduced by the use of another type of inverter, the CSI [Fig. 1(b)]. The CSI requires no dc bus capacitors and uses only three alternating current (ac) filter capacitors of a much smaller capacitance. The total capacitance of the ac filter capacitors is estimated to be about one-fifth that of the dc bus capacitors in the VSI. In addition, the CSI offers many other advantages important for EV/HEV applications: (1) it does not need antiparallel diodes in the switches, (2) it can tolerate phase leg shoot-throughs, (3) it provides sinusoid-shaped voltage output to the motor, and (4) it can boost the output voltage to a higher level than the source voltage to enable the motor to operate at higher speeds. These advantages could translate into a significant reduction in inverter cost and volume, increased reliability, a much higher constant-power speed range, and improved motor efficiency and lifetime. Furthermore, by significantly reducing the amount of capacitance required, the CSI based inverter with silicon IGBTs will be able to substantially decrease the requirements for cooling systems and, further, could enable air-cooled power inverters in the future when silicon carbide based switches become commercially viable.

Two factors, however, have so far prevented the application of CSIs in HEVs. The first is the difficulty of incorporating batteries into a CSI as energy storage devices and controlling the motor at low speeds; the

second is the limited availability of power switches that can block voltages in both forward and reverse directions. However, IGBTs with RB capability are being offered as engineering samples, and the technology is rapidly reaching the maturity needed for commercial production. This project aims to take advantage of the latest technologies to remove the remaining hurdles and bring the CSI to HEV applications by offering new inverter topologies based on the CSI but with novel schemes to incorporate energy storage devices. Two approaches are being examined: one uses a V-I converter and the other uses a passive Z-network of inductors, capacitors, and diodes. The former, although it requires switches, has the advantage of being able to be applied in multiple-motor traction drive systems.

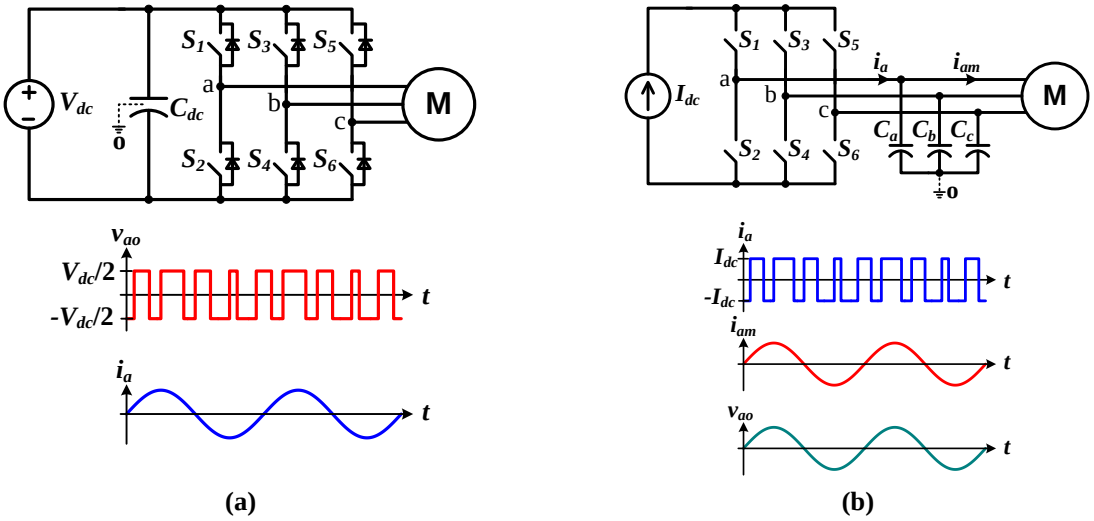

Fig. 1. Schematics of the two types of inverters and typical output voltage and current waveforms: (a) VSI; (b) CSI.

V-I Converter Based CSI

Figure 2 shows a schematic of a V-I converter based CSI for a dual-motor drive system for series or power-split series parallel HEV applications with two CSI bridges connected back-to-back through a V-I converter. The V-I converter includes two switches, S_a and S_b; two diodes, D_1 and D_2; and a dc choke, L_{dc}. The V-I converter transforms the voltage source of the battery into a current source for the inverters, CSIB1 and CSIB2, by providing the capability to control and maintain a constant dc bus current, I_{dc}. The V-I converter also enables the inverters to charge the battery during dynamic braking without the need for reversing the direction of the dc bus current.

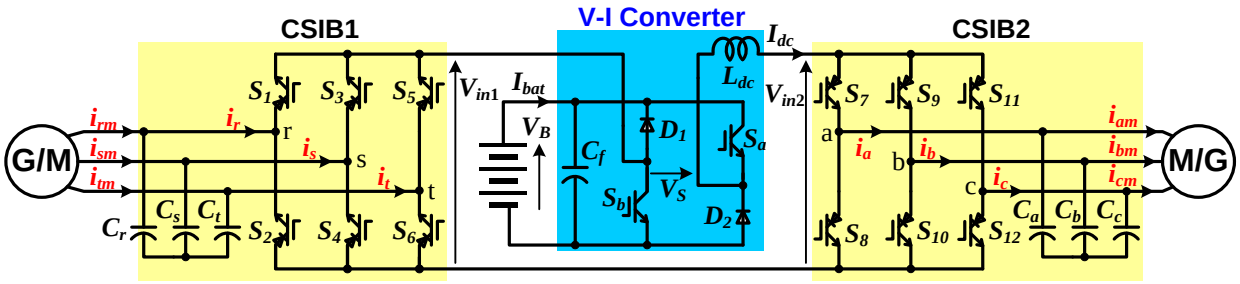

Fig. 2. V-I converter based CSI for a dual-motor drive system for series or power-split series parallel HEV applications.

The CSI based dual-motor drive system provides the following advantages: (1) sharing a single dc link inductor and battery interface circuit (V-I converter); (2) enabling three operation modes: (a) both motors/generators in motoring, (b) both in regen, and (c) one in motoring and one in regen; and (3) producing even higher output voltages for the motor compared to a single CSI drive, as shown in Fig. 3. Table 1 summarizes the performance improvements of the CSI dual-motor-drive PE over the Camry PE.

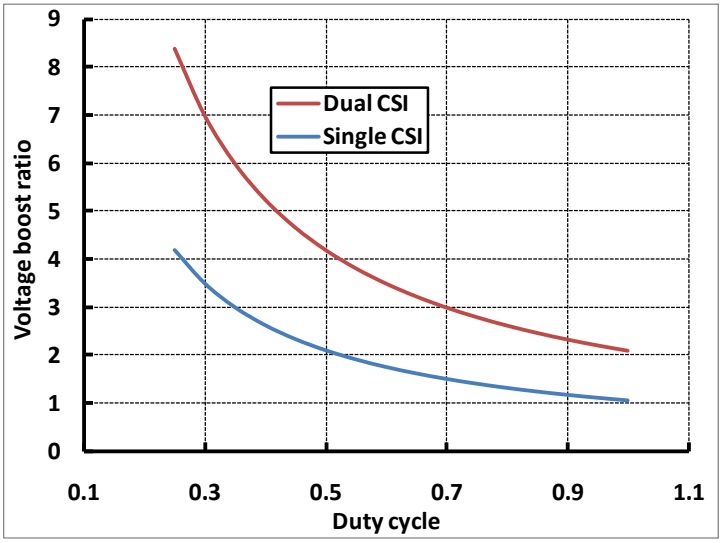

Fig. 3. Voltage boost ratio vs CSI duty cycle.

Table 1. Performance Improvements of the CSI Dual-Motor-Drive PE Over the Camry PE

	Camry PE			**CSI dual-motor-drive PE with regular IGBT[a]**			**CSI dual-motor-drive PE with RB-IGBT[b]**		
	Weight (kg)	Volume (L)	Cost ($)	Weight (kg)	Volume (L)	Cost ($)	Weight (kg)	Volume (L)	Cost ($)
Bus Cap	3.57	2.6	$260.00	0.36	0.26	$26.00	0.36	0.26	$26.00
Side housing	1.2	0.98	$1,040.00	1.20	0.98	$1,040.00	1.20	0.98	$728.00
Power module	5	4.3		5.00	4.30		2.75	2.37	
Boost/V-I converter	6.6	3.5	$325.00	6.60	3.50	$325.00	6.60	3.50	$325.00
Subtotal	16.37	11.38	$1,625.00	13.16	9.04	$1,391.00	10.91	7.11	$1,079.00
Reductions in weight, volume, and cost				**20%**	**21%**	**14%**	**33%**	**38%**	**34%**
Performance metrics	4.3 (kW/kg)	6.2 (kW/L)	23.2 ($/kW)	5.3 (kW/kg)	7.7 (kW/L)	19.9 ($/kW)	6.4 (kW/kg)	9.9 (kW/L)	15.4 ($/kW)
Performance improvement				**23%**	**24%**		**49%**	**60%**	
Reduction in cost/kW						**14%**			**34%**

[a]Assumptions: (1) 90% reduction of capacitance and (2) 20% of inverter cost from capacitor.

[b]Assumptions: (1) 90% reduction of capacitance, (2) 20% of inverter cost from capacitor, (3) 30% reduction in diode cost of the inverter switch module, (4) 45% reduction in diode volume and weight of the inverter switch module, and (5) no changes between the boost converter in the Camry PE and V-I converter in the CSI.

Z-Network Based Current Source Inverter

Two new Z-network based current source inverter (ZCSI) topologies have been developed. Figure 4 shows a schematic drawing of the CF-trans-qZSI, and Fig. 5 depicts the CF-trans-ZSI. Both topologies use a Z-network consisting of a diode, D_1; a capacitor, C_1; and a coupled inductor-transformer, L_1 and L_2. Compared to previous ZCSIs, the new topologies eliminate one capacitor and can extend the constant-power speed range by increasing the transformer turns ratio to provide a higher voltage boost ratio. Compared to the traditional CSI, the ZCSIs can buck and boost the output voltage in a single stage, charge the battery during regen operation, and tolerate open circuit conditions in the CSI bridge.

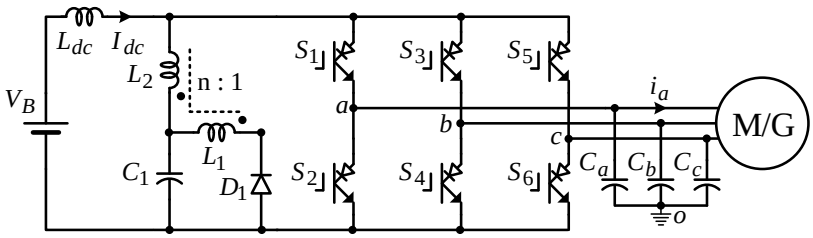

Fig. 4. CF-trans-qZSI.

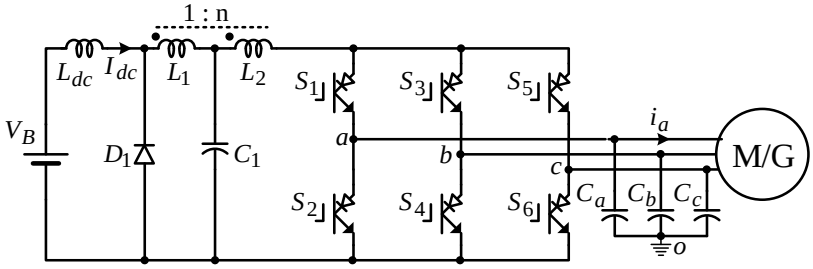

Fig. 5. CF-trans-ZSI.

In addition to the traditional CSI control method, two open circuit–zero state references are added to the current references, as shown by the shaded intervals in Fig. 6. During these intervals, the shoot-through zero states, in which both switches, S_1 and S_2, are conducting, are changed to open circuit zero state by turning off both switches.

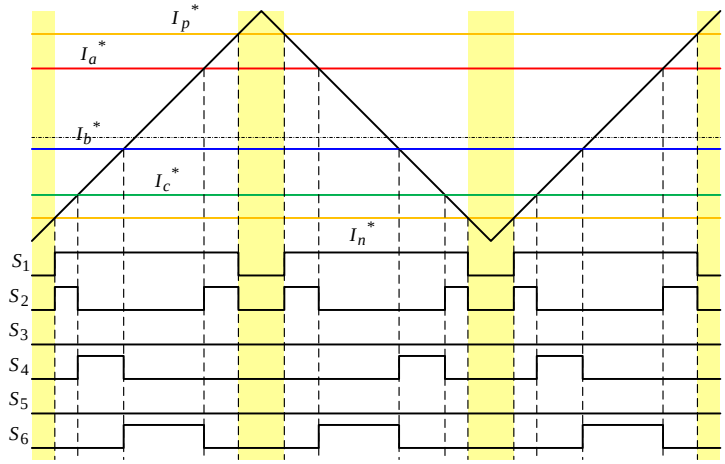

Fig. 6. Pulse width modulated control method with open circuit–zero state references inserted.

Depending on how the open circuit–zero state reference is generated, there are three ways to insert it: (1) simple boost control, in which two straight lines are added as the open circuit–zero state reference; (2) maximum boost control, which uses the envelop of the three-phase current references; and (3) constant boost control, in which the reference is produced by injecting a third harmonic into the current commands, as shown in Fig. 7. The maximum boost control transfers the entire shoot-through zero state interval to open circuit zero state, while the simple boost and constant boost control have the same open-state duty cycle over every switching cycle.

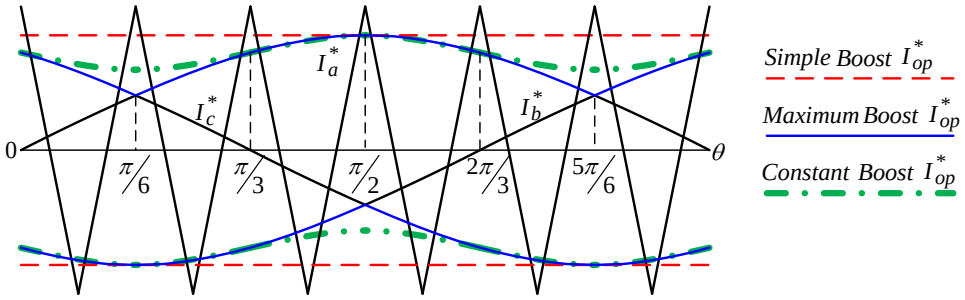

Fig. 7. Pulse width modulated control methods using three different open circuit–zero state references.

Figure 8 shows the equivalent circuits of the CF-trans-ZSI. There are three dc operation states: active, shoot-through zero state, and open circuit zero state. Figure 8(a) shows the active state, in which the inverter operates in one of the six active states and the diode, D_1, (ref Fig 5) is not conducting. Figure 8(b) shows the shoot-through zero state, in which one of the inverter legs is short-circuited and the diode, D_1, is not conducting. Figure8(c) shows the open circuit zero state, in which all the switches of the inverter are off and the motor is disconnected from the battery. The diode, D_1, is conducting during this state. Figure 9 shows the three similar dc equivalent circuits for the CF-trans-qZSI.

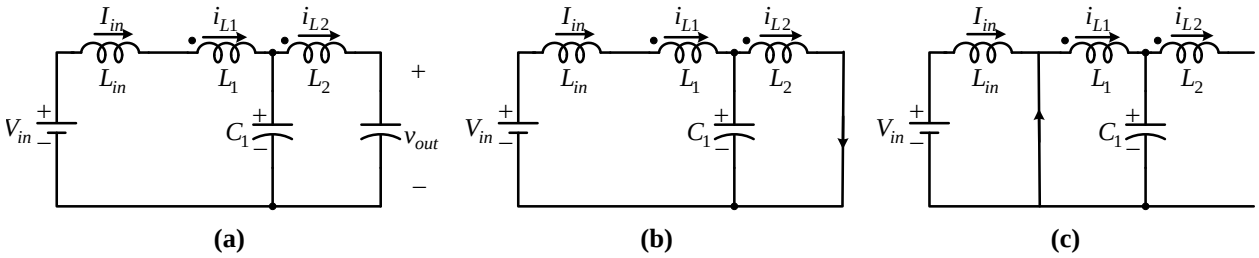

Fig. 8. CF-trans-ZSI equivalent circuit: (a) active state, (b) shoot-through zero state, and (c) open circuit zero state.

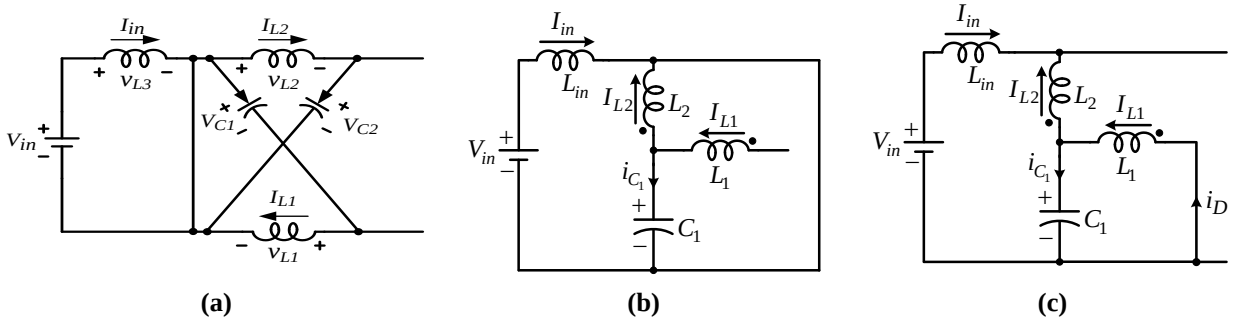

Fig. 9. CF-trans-qZSI equivalent circuit: (a) active state, (b) shoot-through zero state, and (c) open circuit zero state.

The dc voltage gain of the CF-trans-ZSI and CF-trans-qZSI can be derived from the equivalent circuits as

$$\frac{V_{out}}{V_{in}} = \frac{1 - D_{op}(1 + \frac{n_2}{n_1})}{D_A} .$$

For a turns ratio of 2 (i.e., $n_2/n_1 = 2$), the above equation becomes

$$\frac{V_{out}}{V_{in}} = \begin{cases} \frac{1}{D_A} & \text{if } D_{op} = 0 \\ \frac{3D_A - 2}{D_A} & \text{if } D_{sh} = 0 \end{cases} ,$$

where n_2/n_1 is the turns ratio of the coupled inductor and D_A, D_{op}, and D_{sh} represent the duty cycles for the active, open circuit, and short circuit zero states, respectively.

Figure 10 shows the dc output voltage gain of the CF-trans-ZSI and CF-trans qZSI. There are three operation regions, A, B, and C. In region B the inverter operates in the motoring mode and can produce an equivalent dc output voltage in the range of 0 to about 3 Vin. Region C is the regen region as indicated by the negative output voltage gain. In this region, the inverter can operate as a pulse width modulated rectifier to charge the battery. Region A is a prohibited region because the diode of the Z-network will conduct automatically, interrupting the proper operation of the inverter. The output voltage will get distorted due to the unwanted conduction of the diode. If it is desired to extend the motoring operation region, the diode will have to be replaced with an RB switch. Alternatively, increasing the transformer turns ratio can also extend the motoring operation region. In addition, the line marked "Mode 1" represents the motoring operation region boundary on which no open circuit zero states are introduced and the highest voltage gain is achieved. The line marked "Mode 2" is the regen region boundary line where all the shoot through zero states are replaced by open circuit zero states. During this mode, the inverter produces the lowest possible voltage.

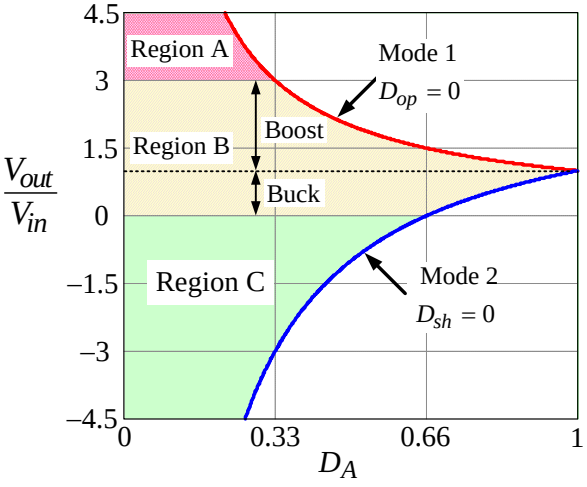

Fig. 10. CF-trans-ZSI and CF-trans-qZSI dc output voltage gain.

Table 2 summarizes the open circuit duty cycle, D_{op}, voltage and current gains corresponding to the modulation index, M, for the three control strategies. In the table, n is the turns ratio of the coupled inductor and cosδ is the power factor (PF) of the motor.

Table 2. Comparison of the Three Different Control Strategies

Control method	D_{op}	Voltage gain	Current gain
Simple boost	$1-M$	$\frac{4}{3M\cos\delta}\left(M(1+n)-n\right)$	$\frac{M}{M(1+n)-n}$
Maximum boost	$1-\frac{3\sqrt{3}M}{2\pi}$	$\frac{4}{3M\cos\delta}\left(\frac{3\sqrt{3}M}{2\pi}(1+n)-n\right)$	$\frac{2\pi M}{3\sqrt{3}M(n+1)-2\pi n}$
Constant boost	$1-\frac{\sqrt{3}M}{2}$	$\frac{4}{3M\cos\delta}\left(\frac{\sqrt{3}M}{2}(1+n)-n\right)$	$\frac{2M}{\sqrt{3}M(n+1)-2n}$

Figure 11 plots the output line-to-line peak voltage gain of the CF-trans-ZSI and CF-trans-qZSI versus the modulation index at n = 2 and PF = 1 for the three control methods. The simple boost method produces the narrowest operation area while the maximum boost method leads to a slightly wider regen area than that of the constant boost scheme.

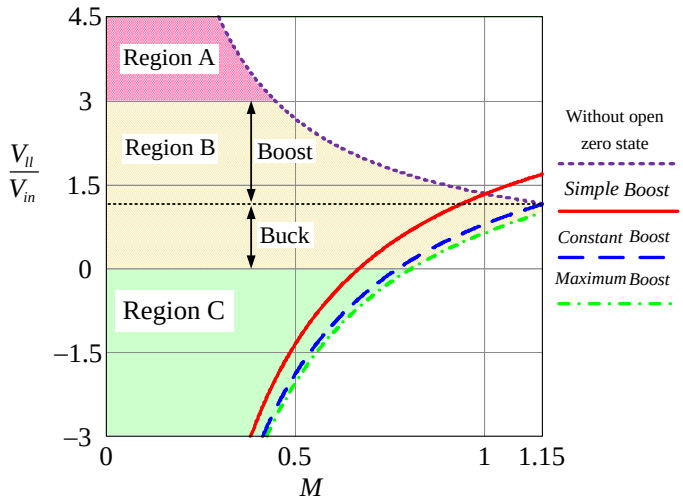

Fig. 11. Output voltage gain at *n* = 2 vs modulation index for the three control methods.

55 kW CF-trans-qZSI Design

A design for a 55 kW CF-trans-qZSI (Fig. 4) was produced for the following conditions.

- Peak power rating: 55 kW
- Battery voltage, V_{in}: 260 V
- Output line-to-line voltage: 0~500 V
- Switching frequency: 10 kHz
- Coupled inductor turns ratio: 2

Based on the calculated voltage stress of 780 V and current stresses of 243 A peak and 70 A average for the switches, an RB-IGBT rated at 1,200 V and 200 A should be chosen. However, because RB-IGBTs with those ratings are not available at the present, the conduction and switching loss data of the 1,200 V–100 A RB-IGBT from Fuji will be used to estimate the losses and efficiency of the inverter design. At $V_{ce(sat)}$ = 2.8 V and an average switch current of 70 A, conduction losses of the six switches are estimated to be 1,176 W (6 × 2.8 × 70). Assuming the RB-IGBT switching loss of 200 A would be twice that of the 100 A devices, the total switching loss of the six devices under 10 kHz switching would be 1,800 W (6 × 30 mJ × 10 kHz). The estimated volume and weight of the RB-IGBT module are 0.308 L and 0.85 kg, respectively, based on the current 100 A RB-IGBT modules.

Based on the calculated diode voltage stress of 390 V and current stresses of 626 A peak and 211 A average, a diode rated at 600 V and 600 A could be sufficient for the design. The readily available diode from Powerex (QRS0680T30, rated at 600 V and 800 A) was, however, chosen for the design. The weight and volume of the diode are 0.22 kg and 95.88 mL, respectively. The diode conduction and reverse recovery losses are estimated at 358.7 W and 13.0 W, respectively.

Requirements for the Z-network capacitor are 300 V, 450 Arms, and 300 µF. To meet the ripple current requirement, four Electronic Concepts film capacitors, UL34Q157K, in parallel were chosen for the design, resulting in a total capacitance of 600 µF, a total volume of 0.87 L, and a total weight of 1.2 kg. The loss due to the electric series resistance is 24.3 W.

Requirements for the Z-network inductors, L_1 and L_2, are 15 µH/367 Arms and 60 µH/300 Arms, respectively. With the selected amorphous core, AMCC500, and 6 turns for L_1 and 12 turns for L_2, the resulting coupled inductor has L_1 = 12.6 µH, L_2 = 50.4 µH, core weight of 2.89 kg, core loss of 393 W, copper loss of 202 W, copper weight of 1.9 kg, and a total inductor volume of 0.75 L.

Requirements for the input inductor, L_{dc}, are 212 A and 69 µH. With the selected amorphous core, AMCC320, and 11 turns, the resulting inductor has L_{dc} = 60.5 µH, core weight of 2.17 kg, core loss of 295 W, copper loss of 70 W, copper weight of 0.649 kg, and a total inductor volume of 0.72 L.

The voltage stress of the output ac filter capacitors is around 500 Vrms, and the required capacitance is 30 µF per phase. By connecting the output capacitors in delta, the required per-phase capacitance value will be reduced to one-third (i.e., 10 µF). The Electronic Concepts film capacitor, 5MPA2106J, rated at 530 VAC and 10 µF, was selected, resulting in a total volume of 0.265 L and weight of 0.408 kg.

A water-cooled heat sink about twice the size of the switch module was chosen for the design. The volume and weight of the heat sink are 0.308 L and 0.974 kg, respectively.

Table 3 provides a summary of component volumes and weights and the resulting power density. Figure 12 shows inverter volume breakdown by component; the Z-network capacitor and inductors are the major volume-contributing parts, constituting 71% of the total inverter volume. Figure 13 illustrates weight breakdown by component; the Z-network inductor contributes the most to the inverter weight (42%). Figures 14 and 15 show loss breakdown in boost mode and buck mode. The estimated efficiency is 93.8% in boost mode and 94% in buck mode.

Table 3. Summary of Component Volume, Weight, and Power Density for the 55 kW Inverter Design

	Switches	**Diode**	**Z-network capacitor**	**Z-network inductor**	**Input inductor**	**Output capacitor**	**Heat sink**	**Total**	**Power density**
Weight (kg)	0.85	0.22	1.2	4.79	2.816	0.408	0.9735	**11.2575**	**4.89 kW/kg**
Volume (L)	0.308	0.09588	0.87	0.75	0.72	0.265	0.308	**3.317**	**16.6 kW/L**

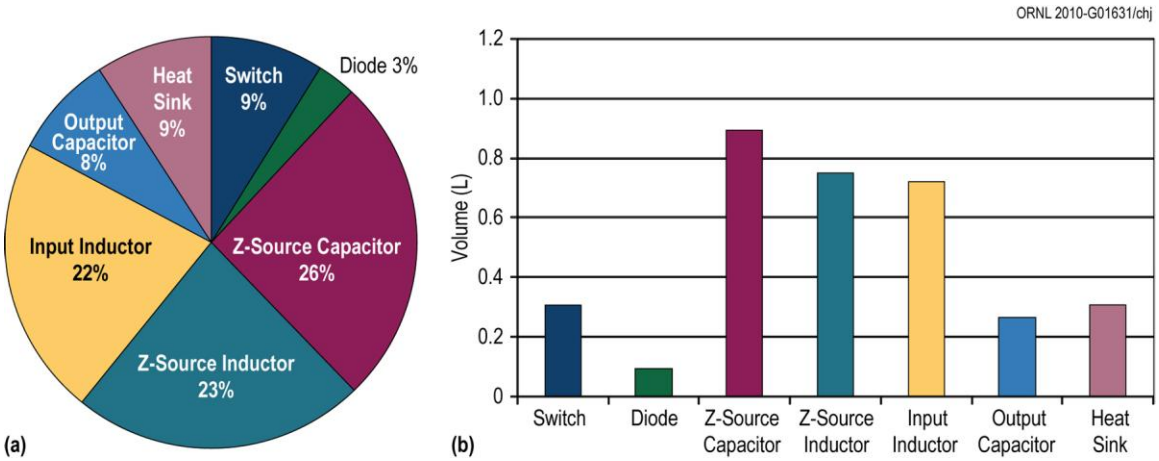

Fig. 12. Volume breakdown by component for the 55 kW CF-trans-qZSI design: (a) component percentage of total; (b) component volume in liters.

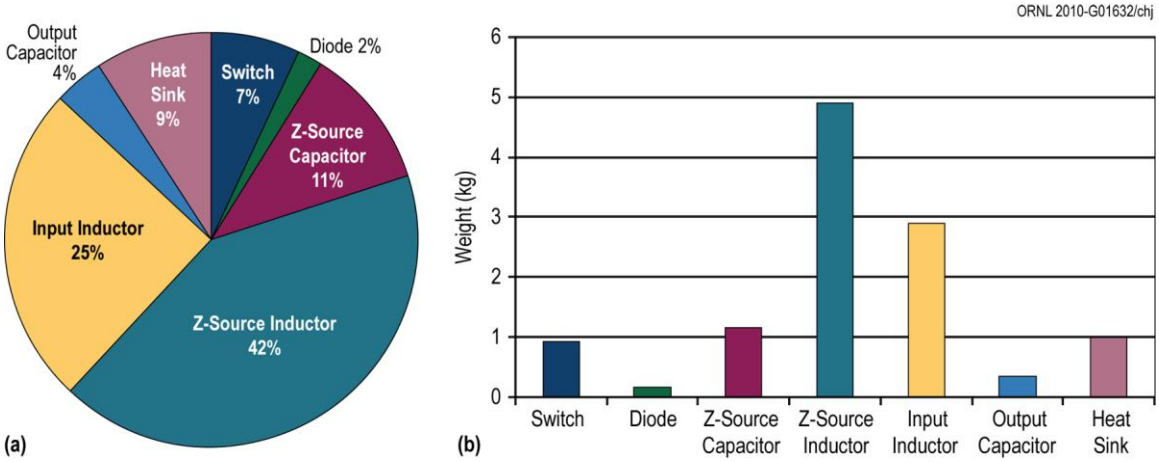

Fig. 13. Weight breakdown by component for the 55 kW CF-trans-qZSI design: (a) component percentage of total; (b) component weight in kilograms.

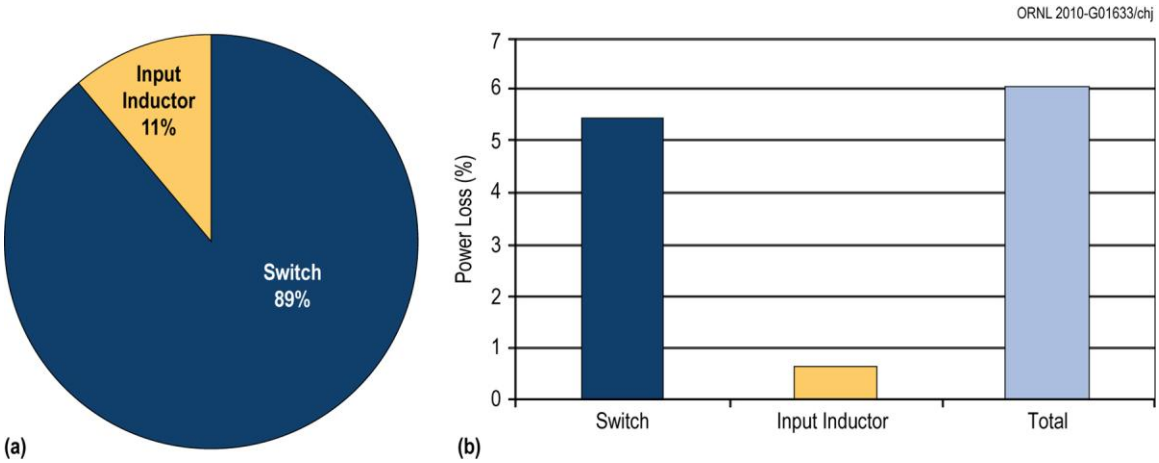

Fig. 14. Boost mode loss breakdown by component for the 55 kW CF-trans-qZSI design: (a) component loss as a percent of the whole; (b) individual component power loss.

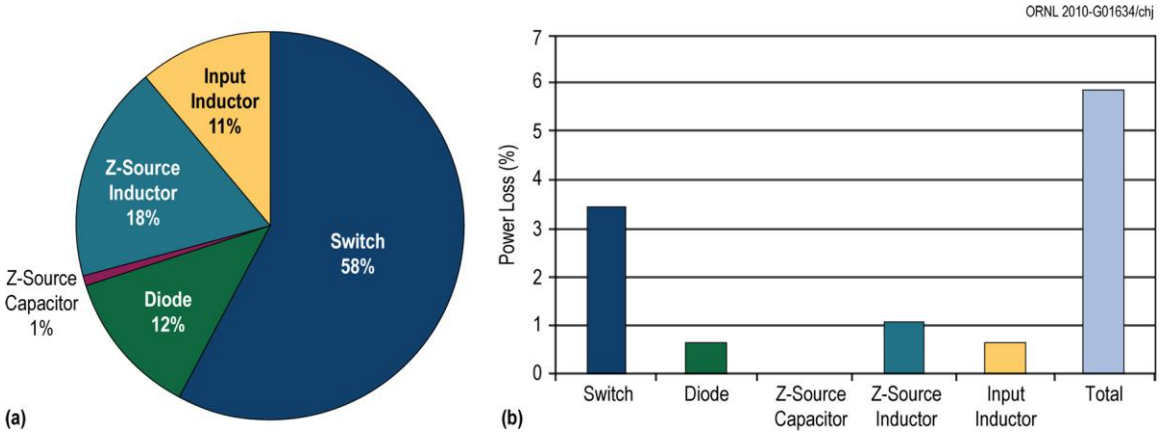

Fig. 15. Buck mode loss breakdown by component for the 55 kW CF-trans-qZSI design: (a) component loss as a percent of the whole; (b) individual component power loss.

The switching device loss is the major contributor to the total loss. To achieve higher power density and reduce the size of the inductor, the switching frequency should be increased. But the device switching loss will also increase, negatively impacting the converter efficiency. Currently available first generation RB-IGBT technology was used in this design. With anticipated 100% reductions in switching and conduction losses with next generation RB-IGBTs, the boost mode and buck mode efficiency numbers can be increased to 96% and 96.7%, respectively, as shown in Fig. 16. Further, future wide bandgap based devices, which can switch at high frequencies while still maintaining low switching losses, can be used to shrink the size of the inductors and improve the power density and efficiency.

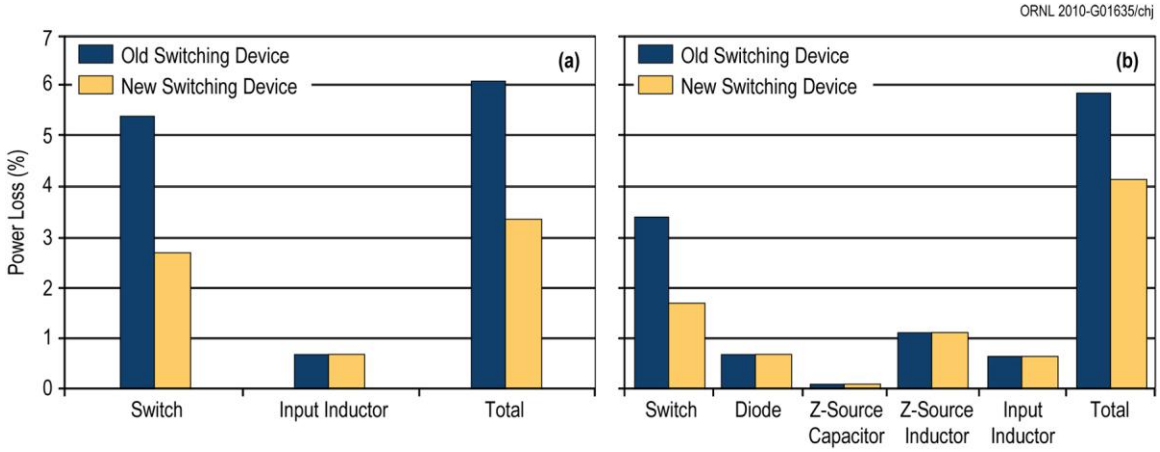

Fig. 16. Power loss comparisons showing anticipated loss reductions with next generation RB-IGBTs for (a) boost mode and (b) buck mode.

Figures 17–19 show simulated waveforms of three-phase motor voltages, Vab, Vbc, and Vca; motor currents, ia, ib, and ic; battery current, Iin; and battery voltage, Vin, for the 55 kW ZCSI design operating in boost, buck, and regen modes.

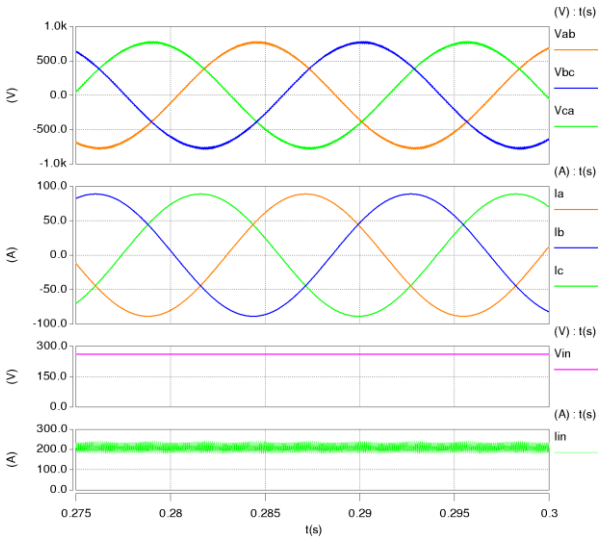

Fig. 17. Simulated waveforms in boost mode.

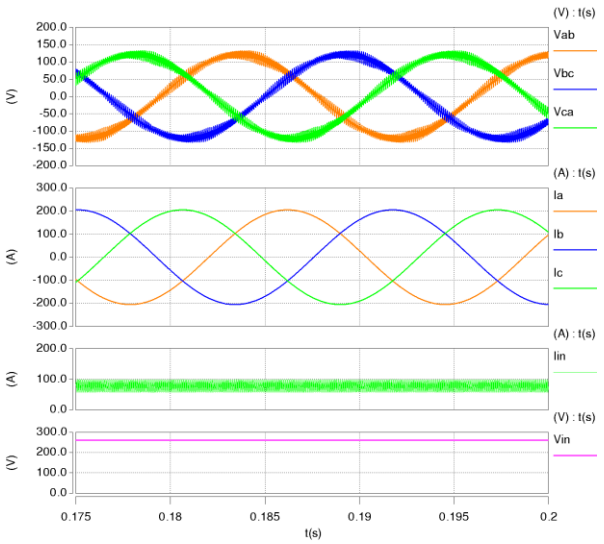

Fig. 18. Simulated waveforms in buck mode.

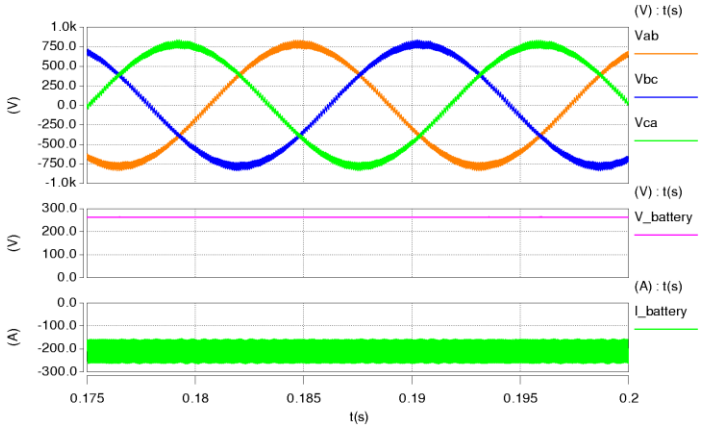

Fig. 19. Simulated waveforms in regen mode.

Conclusion

Two new ZCSIs with a reduced component count, CF-trans-ZSI and CF-trans-qZSI, were developed. Simulation study indicates the new ZCSIs have a voltage boost ratio of 3 in contrast to 2 for the previous ZCSIs.

A design for a 55 kW ZCSI based on the CF-trans-qZSI was completed using first generation RB-IGBT technology. The design yields a specific power of 4.89 kW/kg, a power density of 16.6 kW/L, and efficiency of 93.8% in boost mode and 94% in buck mode. With next generation RB-IGBT technology, it is estimated the efficiency numbers can be increased to 96% and 96.7%, respectively.

Simulation results confirmed the feasibility of using the ORNL V-I converter based CSI topology in series and power-split series parallel HEV configurations. The CSI dual-motor-drive PE using RB-IGBTs provides significant performance improvements over the Camry PE: 49% increase in specific power (6.4 vs 4.3 kW/kg), 60% increase in power density (9.9 vs 6.2 kW/kg), and 34% reduction in cost ($15.4/kW vs $23.2/kW).

Publications

1. L. Tang and G. J. Su, "Boost Mode Test of a Current-Source-Inverter-Fed Permanent Magnet Synchronous Motor Drive for Automotive Applications," in Proceedings of *the 12th IEEE Workshop on Control and Modeling for Power Electronics* (COMPEL 2010), June 28–30, 2010, Boulder, Colorado.
2. G. J. Su, L. Tang, and Z. Wu, "Extended Constant-Torque and Constant-Power Speed Range Control of Permanent Magnet Machine Using a Current Source Inverter," in *Proceedings of the 5th IEEE Vehicle Power and Propulsion Conference* (VPPC '09), pp. 109–115, Sept. 7–11, 2009, Dearborn, Michigan.
3. Z. Wu and G. J. Su, "High-Performance Permanent Magnet Machine Drive for Electric Vehicle Applications Using a Current Source Inverter," in *Proceedings of the 34th Annual Conference of the IEEE Industrial Electronics Society* (IECON '08), pp. 2812–2817, November 10–13, 2008, Orlando, Florida.

References

1. M. Takei, Y. Harada, and K. Ueno, "600V-IGBT with reverse blocking capability," pp.413–416 in *Proceedings of IEEE ISPSD '2001*, 2001.
2. E. R. Motto, et al., "Application Characteristics of an Experimental RB-IGBT (reverse blocking IGBT) Module," in *Proceedings of IEEE IAS 2004 Annual Meeting*, pp. 1504–1544 (2004).

Patents

1. Gui-Jia Su, "Power Conversion Apparatus and Method," application US12/399,486, March 6, 2009, patent pending.

2.5 A Segmented Drive Inverter Topology with a Small dc Bus Capacitor

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Objectives

- Overall project objectives
  - — Significantly reduce the amount of inverter direct current (dc) bus capacitance through reducing the ripple current by 60%.
- Objectives for FY 2010 effort
  - — Demonstrate a 55 kW segmented inverter prototype that is capable of operating with an amount of bus capacitance reduced by 60% compared to a standard voltage source inverter (VSI).

Approach

- Use a segmented drive system topology that does not need additional switches or passive components but can significantly reduce the dc link ripple current and the capacitance.
- Perform simulation study of various pulse width modulation (PWM) schemes using PSIM circuit simulation software to assess their impact on the capacitor ripple current.
- Design, build, and test a 55 kW inverter prototype to experimentally validate the simulation study.

Major Accomplishments

- Demonstrated a 55 kW segmented inverter prototype with a 60% reduction of dc bus capacitance compared to a standard VSI.
  - — Prototype test results show
    (a) a significant reduction of 55% to about 75% in capacitor ripple current and
    (b) a significant reduction of 70% to about 90% in battery ripple current.
  - — Estimated performance improvements when the technology is applied to the Toyota Camry motor inverter include
    (a) 40% increase in specific power to 12.9 kW/kg,
    (b) 35% increase in power density to 15.9 kW/L,
    (c) 11% decrease in $/kW to $11.6/kW, and
    (d) exceeding the DOE 2015 target for specific power and the 2020 target for power density.

Future Direction

- Design, build, test, and characterize a 55 kW prototype of an integrated segmented inverter-motor drive to reduce drive system cost.

Technical Discussion

Background

The dc bus capacitor is an essential component for maintaining a stable dc bus voltage for the VSI based traction drive systems in electric vehicles, hybrid electric vehicles (HEVs), and plug-in HEVs. Figure 1 is a schematic of the standard VSI based drive system. The VSI, mainly comprising six power semiconductor switches—typically insulated gate bipolar transistors (IGBTs)—and a dc bus filter capacitor, switches the battery voltage according to a chosen PWM scheme to control the motor torque and speed through regulating the motor current and voltage. In doing the switching operations, it generates large ripple currents in the dc link, necessitating the use of the dc bus filter capacitor to absorb the ripple currents and suppress voltage transients, which occur on the dc bus at every instant of inverter switching and are detrimental to the battery life and reliability of the semiconductor switches in the inverter.

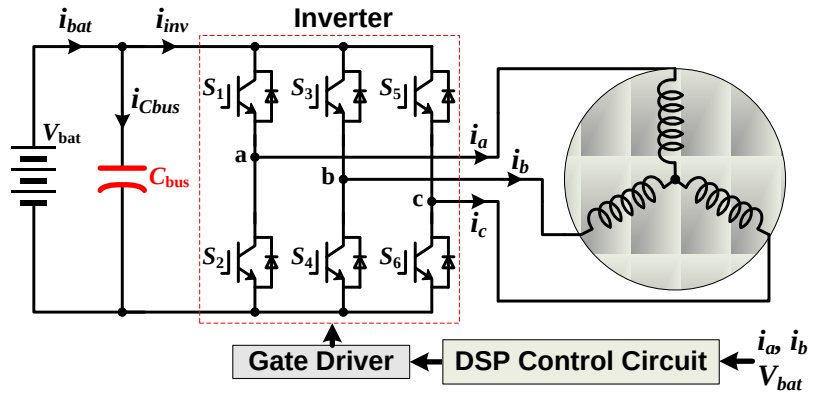


Fig. 1. Standard VSI based drive system in HEVs.

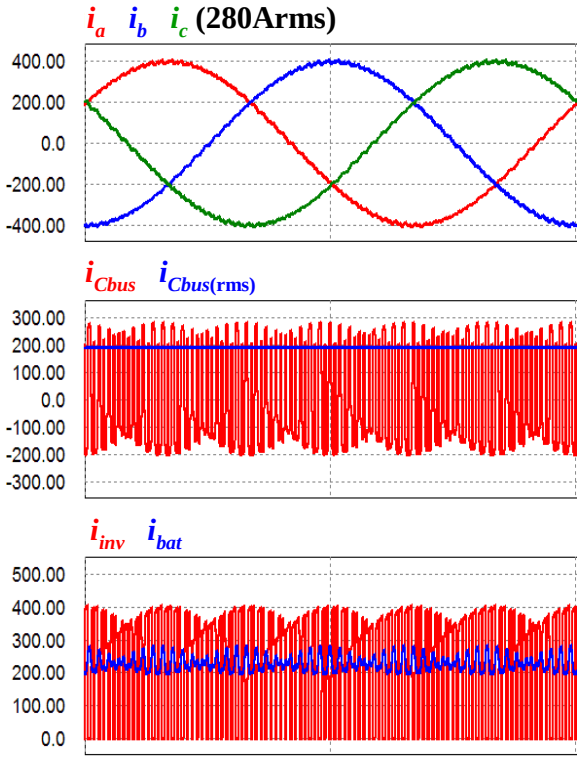


Figure 2. Simulated waveforms in the standard VSI based drive system.

Figure 2 shows simulated motor currents, i_a, i_b, and i_c; capacitor ripple current, i_{Cbus} and $i_{Cbus(rms)}$; inverter dc link current, i_{inv}; and battery current, i_{bat}, in a typical 55 kW HEV inverter. The capacitor ripple current reaches as large as 200 Arms, and thus, a bulky and costly dc bus capacitor of about 1,000 µF is required to prevent this large ripple current from flowing into the battery.

Concerns about the reliability of electrolytic capacitors have forced HEV makers to use film capacitors, and currently available film capacitors that can meet the demanding requirements are costly and bulky, taking up one-third of the inverter volume and making up one-fifth of the cost. The dc bus capacitor, therefore, presents significant barriers to meeting the requirements of the FreedomCAR goals for inverter volume, lifetime, and cost established by DOE and its industrial partners [1].

The large ripple currents become even more problematic for the film capacitors in high temperature environments because their ripple current handling capability decreases rapidly with rising temperatures, as indicated in Fig. 3, which maps this capability for a typical film capacitor. For example, as the ambient temperature rises from 85 to

105°C, the weight, volume, and cost of capacitors could increase by a factor of 5 due to the decrease of their ripple current capability from 50 to 11 A.

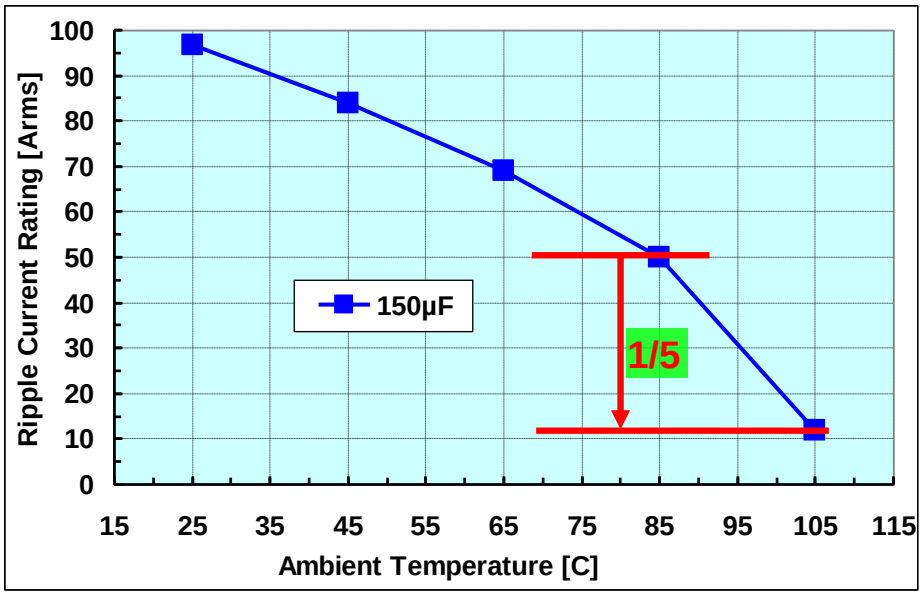


Fig. 3. Film capacitor ripple current capability vs ambient temperature (Electronic Concepts UL31 Series) [2].

To help achieve the FreedomCAR targets, there is thus an urgent need to minimize this bulky component by significantly reducing the ripple current. A much smaller dc bus capacitor would also enable inverters to operate at higher temperatures. The following factors, however, make this a difficult task:
(1) increasing the switching frequency, which is one of the anticipated benefits with future wide bandgap based switches, has little impact on the bus capacitor ripple currents because the capacitor ripple currents depend on the motor peak current and (2) the major components of the capacitor ripple currents have frequencies of multiples of the switching frequency (nf_{sw}) or their side bands ($nf_{sw} \pm f_m$, $nf_{sw} \pm 2f_m$, …), as given by the equation below and illustrated in Fig. 4. The high frequency nature makes it impractical to actively filter out the ripple components because doing so requires the use of very high switching frequencies in the active filter.

$$i_{inv} = I_{dc} + \sum_{k=0}^{\infty}\sum_{n=1}^{\infty} I_{n,k} \sin[2\pi(nf_{sw} \pm kf_m)t + \alpha_{n,k}] \quad ,$$

where

f_{sw} = switching frequency
f_m = motor fundamental frequency.

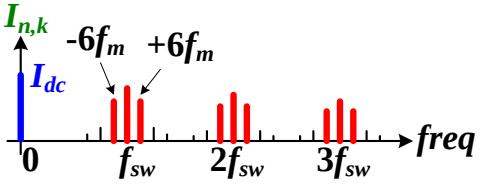


Fig. 4. Ripple components in the dc link current in the standard VSI based drive system.

Features of the Proposed Segmented Drive

A segmented drive system topology is being examined in this project to reduce the dc bus capacitor ripple current. Because the technology is under patent review, details of the topology will not be shown in this report. However, the segmented topology does not need additional switches or passive components but enables the use of optimized PWM schemes to significantly reduce the dc link ripple current generated by switching the inverter output currents.

The uniqueness of this technology is that, while being able to significantly reduce the capacitor ripple current, it *does not*

- need additional silicon or passive (L or C) components,
- need additional sensors, or
- add control complexity.

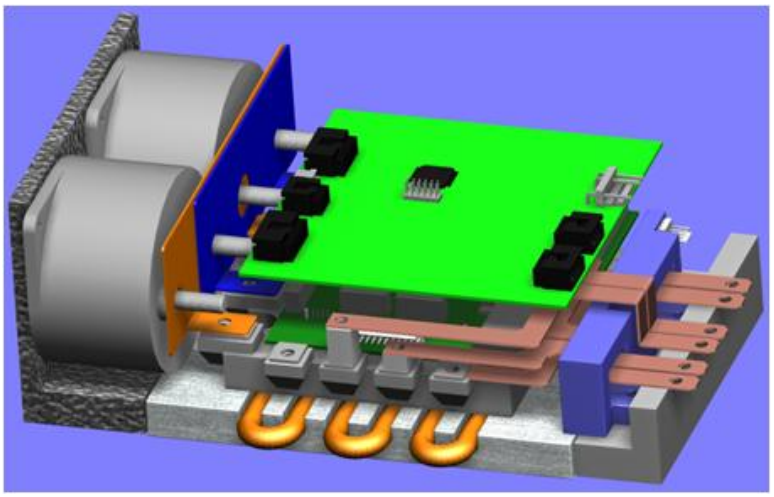
The following positive impacts are expected:

- substantially reduced bus capacitance (at least 60%) and thus reduced inverter volume and cost,
- reduced battery losses and improved battery operating conditions through elimination of battery ripple current, and
- significantly reduced motor torque ripples (up to 50%) or reduced switching losses (by 50%).

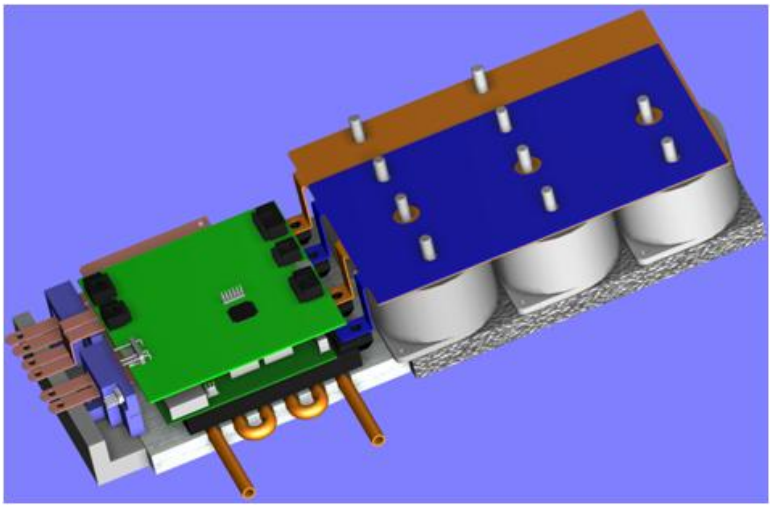
A simulation study using PSIM carried out in FY 2009 has validated the segmented drive concept and indicated that the bus capacitance can be reduced by 60% from that needed for a standard VSI. The simulation results also show that, compared to the standard inverter configuration, the segmented drive inverter can achieve (1) more than 65% reduction in capacitor ripple current, (2) 80% reduction in battery ripple current, (3) 70% reduction in dc bus ripple voltage, and (4) 50% reduction in motor ripple current.

Prototype Design and Test Results

Incorporating the simulation study, a 55 kW prototype was designed, built, and tested during FY 2010. Figure 5(a) is a three-dimensional drawing of the hardware design for the 55 kW prototype. A design for a 55 kW baseline standard VSI is also shown for comparison [Fig. 5(b)]. Both designs use the same IGBT modules, purchased from Powerex, and the same water-cooled cold plate, measuring 6 in. by 7 in., for cooling the IGBT modules. Capacitor requirements for the segmented inverter are 400 µF and are fulfilled with two film capacitors, each rated at 500 V/200 µF. In comparison, a total of 1,000 µF capacitance is needed for the baseline VSI design and is furnished by five film capacitors, each rated at 500 V/200 µF. The capacitors are mounted on an aluminum heat sink attached to the cold plate. Because of the capacitance requirement (more than twice that of the segmented inverter), the baseline design requires a significantly larger heat sink for mounting the capacitors. Table 1 gives a comparison of heat sink size and capacitor volume for the two designs. Figure 6 is a photo of the assembled 55 kW segmented inverter prototype. A Texas Instruments 32 bit fixed-point digital signal processor chip, TMS320F2812, is used to implement the motor control and PWM switching schemes.



(a)



(b)

Figure 5. Hardware designs for 55 kW prototypes: (a) segmented inverter and (b) baseline standard VSI.

Table 1. Comparison of Heat Sink Size and Capacitor Volume

	Baseline	Segmented
Heat sink footprint	**6" × 7"+ 6.6" × 9.6"**	**6" × 7"+ 6.6" × 2.2"**
Cap. volume	**1.39 L**	**0.56 L** → **a 60% reduction**

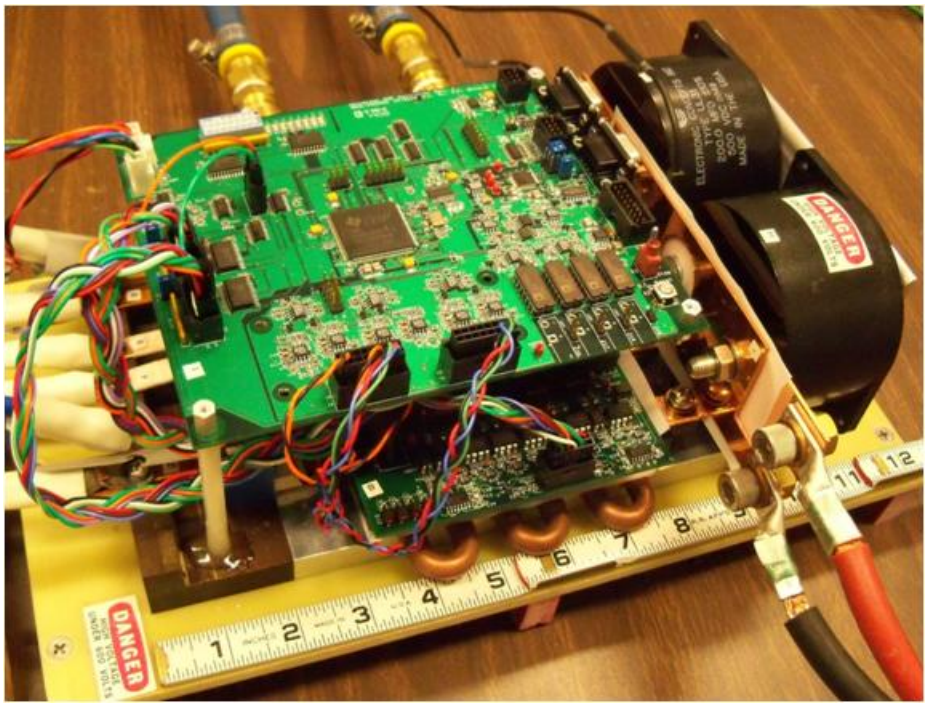
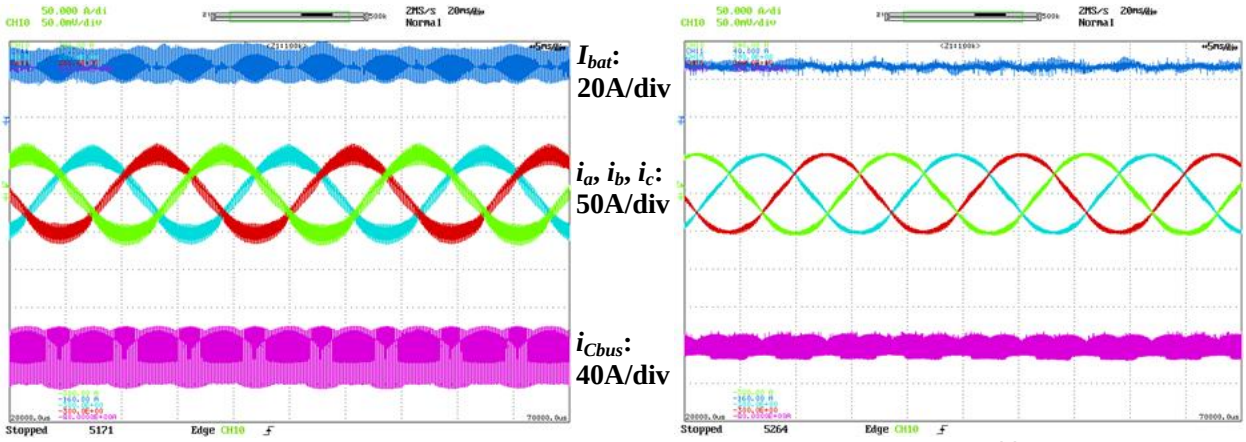


Fig. 6. A 55 kW segmented inverter prototype.

The prototype was tested first with an inductor-resistor (R-L) load bank with nominal circuit parameters of 0.45 mH and 1.6 Ω. A dc power supply was used to simulate a 300 V battery. For comparison, the prototype was reconfigured as the baseline VSI, but without the added capacitors, and tested at the same load conditions. Figure 7 shows battery current, I_{bat}; load currents, i_a, i_b, and i_c; and capacitor ripple current, i_{Cbus}, for a dc input power of 7 kW where (a) is for the baseline inverter and (b) for the segmented inverter. The measured capacitor ripple currents are 33.6 Arms for the baseline inverter and 9.2 Arms for the segmented inverter, and the measured peak-to-peak battery ripple currents are, respectively, 24 A and 8 A. These measurements give a reduction of 73% for capacitor ripple current and 67% for battery ripple current with the segmented inverter. Figures 8 and 9 show waveforms for the same currents at dc input power of 10.5 kW and 19 kW. Comparing the measured results reveals that the segmented inverter provides a reduction of 75% in capacitor ripple current and 73% in battery ripple current at the dc power of 10.5 kW. The reduction ratios are 62% and 78% for the case with dc input power of 19 kW. Moreover, while the three-phase load current waveforms in the baseline inverter have substantial harmonic components due to the relatively low load inductance, these harmonic components disappeared almost entirely from the current waveforms in the segmented inverter. This is another benefit with the segmented inverter and is important to permanent magnet (PM) motors, which have low inductance. It means a lower switching frequency can be used to increase the inverter efficiency.

Figure 10 plots the capacitor ripple currents at various levels of input dc power for both the baseline and segmented inverters. The segmented inverter offers a significant reduction of capacitor ripple current (in the range of 55%~75%).

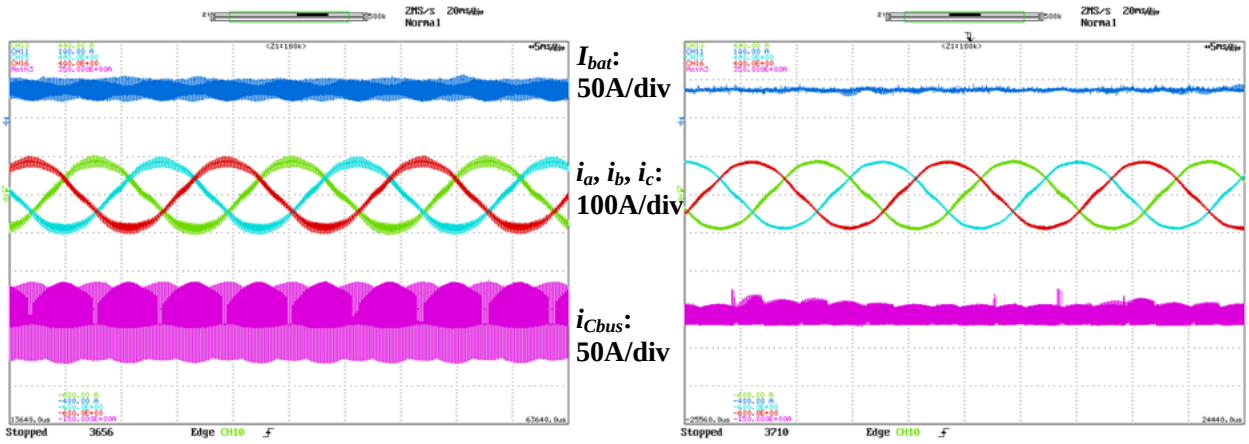
Figure 11 plots the battery ripple currents at various levels of input dc power for both the baseline and segmented inverters. Again, the segmented inverter offers a significant reduction of battery ripple current (in the range of 70%~80%).



Baseline inverter
$i_{Cbus(rms)}$: 33.6 Arms, $I_{bat,\ p\text{-}p\ ripple}$: 24 A

Segmented inverter
$i_{Cbus(rms)}$: 9.2 Arms, $I_{bat,\ p\text{-}p\ ripple}$: 8A

Fig. 7. Waveforms with an R-L load at dc input power of 7 kW, showing a reduction of 73% for capacitor ripple current and 67% for battery ripple current with the segmented inverter.



Baseline inverter
$i_{Cbus(rms)}$: 54.6 Arms, $I_{bat,\ p\text{-}p\ ripple}$: 37 A

Segmented inverter
$i_{Cbus(rms)}$: 13.4 Arms, $I_{bat,\ p\text{-}p\ ripple}$: 10A

Fig. 8. Waveforms with an R-L load at dc input power of 10.5 kW, showing a reduction of 75% for capacitor ripple current, 73% for battery ripple current with the segmented inverter.

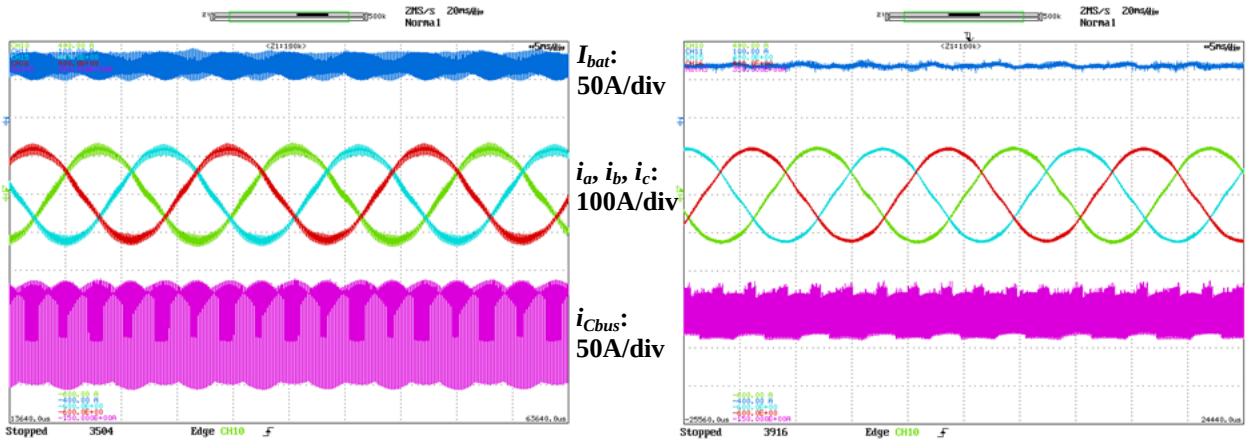


Fig. 9. Waveforms with an R-L load at dc input power of 19 kW, showing a reduction of 62% for capacitor ripple current, 78% for battery ripple current with the segmented inverter.

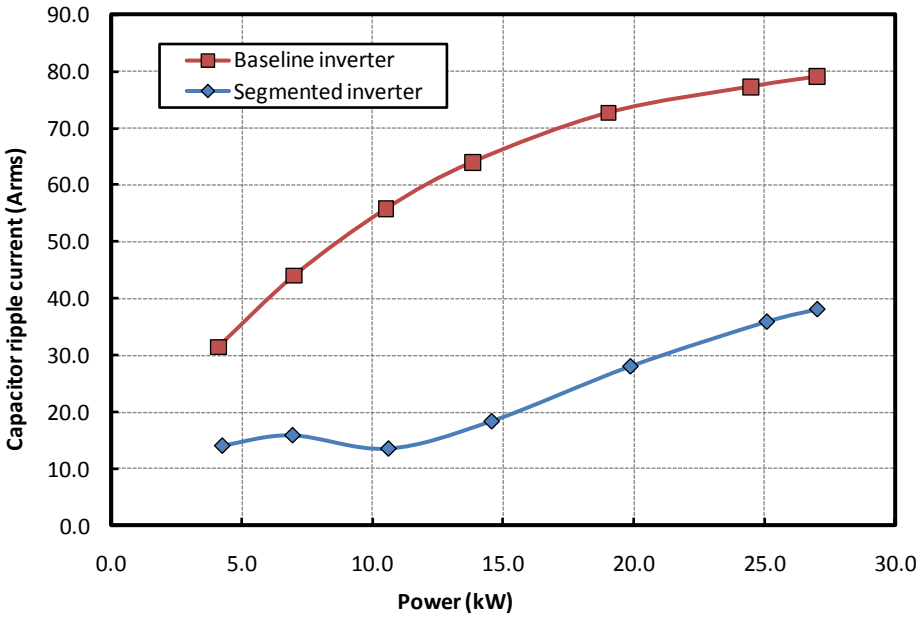


Fig. 10. Comparison of capacitor ripple current vs dc input power for an R-L load.

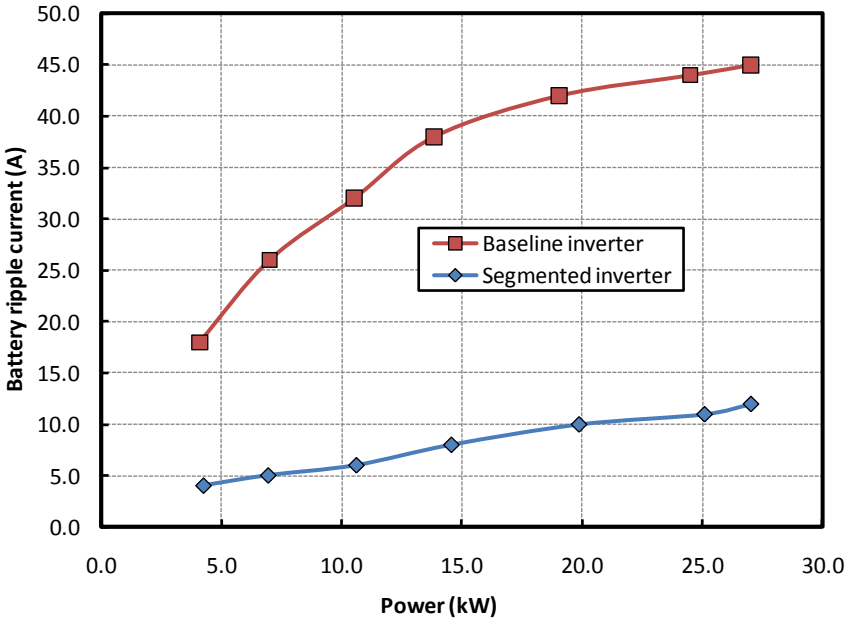


Fig. 11. Comparison of battery ripple current vs dc input power for an R-L load.

The prototype was then tested with a commercial, off-the-shelf, induction motor rated at 15 HP, 230 Vrms, 37.5 Arms, and 1,175 rpm. The motor is in delta connection and has six pole pairs. Tests were conducted at speed and load torque levels of 100%, 75%, and 50% of the rated value of 91 Nm. Due to the limitation of the maximum dc power supply voltage of 300 V, tests could not be done at the rated speed region. Figure 12 shows battery current, I_{bat}; motor currents, i_a, i_b, and i_c; capacitor ripple current, i_{Cbus}, at 565 rpm; and rated torque of 91 Nm where (a) is for the baseline inverter and (b) for the segmented inverter. The measured capacitor ripple currents are 37.1 Arms for the baseline inverter and 10.0 Arms for the segmented inverter, and the measured peak-to-peak battery ripple currents are 45 A and 5 A, respectively. These measurements show a reduction of 73% for capacitor ripple current and 89% for battery ripple current with the segmented inverter.

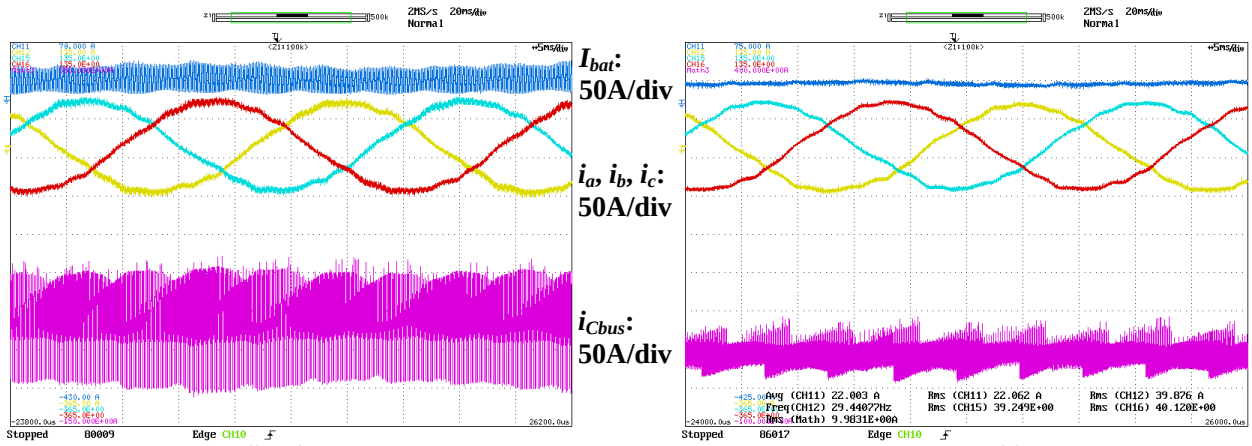


Fig. 12. Waveforms with an induction motor at 565 rpm and rated torque of 91 Nm, showing a reduction of 73% for capacitor ripple current and 89% for battery ripple current with the segmented inverter.

Figure 13 plots the capacitor ripple currents at various levels of load torque vs motor speed for both the baseline and segmented inverters. The segmented inverter offers a significant reduction of capacitor ripple current, in the range of 55%~75%, at the rated torque; 50%~70% at 75 % of rated torque; and 50%~60% at 50% of rated torque. It is also worth noting that the maximum ripple current with the baseline VSI approaches the rated motor current of 37.5 Arms.

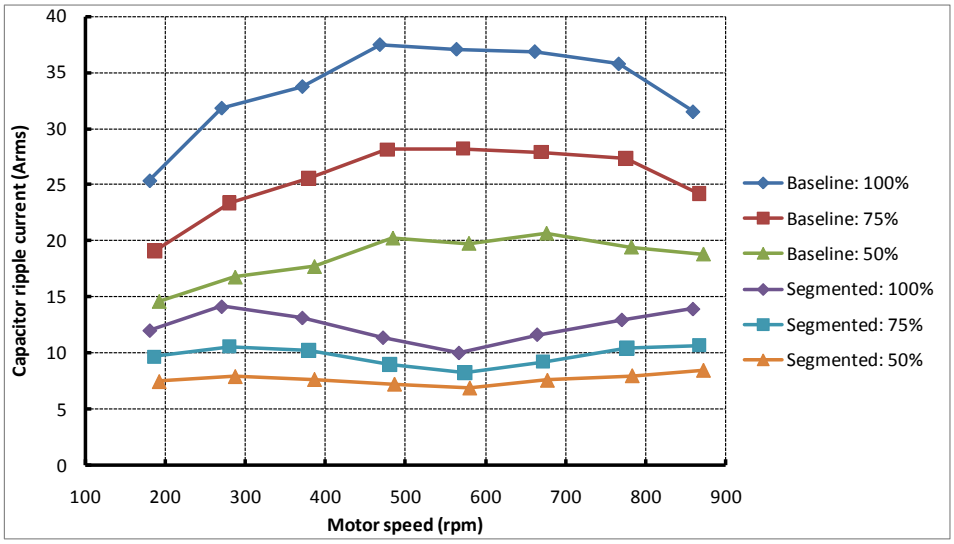


Fig. 13. Comparison of capacitor ripple current vs motor speed at load torque of 100%, 75%, and 50% of rated torque of 91 Nm.

Conclusion

A 55 kW segmented inverter prototype with a 60% reduction of dc bus capacitor was designed, built, and successfully tested with both R-L load and an induction motor. Test results show a significant reduction of 55%~75% in capacitor ripple current and 70%~90% in battery ripple current. Moreover, a lower switching frequency can be used with the segmented inverter to increase the inverter efficiency while still maintaining a low level of harmonic components in motor currents even for low inductance motors such as PM motors.

Table 2 shows estimated performance improvements when the technology is applied to the Toyota Camry motor inverter: 40% and 35% increases in specific power and power density, respectively, and 11% decrease in cost per kilowatt. It also indicates that the segmented inverter would exceed the DOE 2015 target for specific power and the 2020 target for power density.

Table 2. Estimated Performance Improvements

	Camry inverter[a]			**Segmented inverter[b]**		
	Weight (kg)	Volume (L)	Cost ($)	Weight (kg)	Volume (L)	Cost ($)
Bus Capacitor	3.57	2.6	182	1.43	1.04	73
Others	3.99	3.36	728	3.99	3.36	737
Subtotal	7.56	5.96	910	5.42	4.4	810
Metrics	**kW/kg**	**kW/L**	**$/kW**	**kW/kg**	**kW/L**	**$/kW**
	9.3	11.7	13	**12.9**	**15.9**	**11.6**
DOE targets	12	12	5	14.1	13.4	3.3
		2015			2020	

[a] Assumptions: Capacitor costs 20%.
[b] Assumptions: A reduction of 60% in bus capacitor requirement.

References

1. U.S. Department of Energy, "FreedomCAR and Fuel Technical Partnership Technical Goals," http://www1.eere.energy.gov/vehiclesandfuels/about/partnerships/freedomcar/fc_goals.html.
2. Electronic Concepts Datasheet, http://www.eci-capacitors.com/product_details.asp?productid=29.

Patents

1. Gui-Jia Su, "Electrical Motor/Generator Drive Apparatus and Method," U.S. Patent App. 12/887,110, filed September 25, 2009.

2.6 Novel Packaging to Reduce Stray Inductance in Power Electronics

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Objectives

- Package devices in large power modules such that stray inductance is reduced.
- Reduce the stress on the insulated gate bipolar transistors (IGBTs) in hybrid electric vehicle (HEV) traction drives and dc-dc converters. Therefore, the IGBT can work at higher power rating and/or have better reliability and longer lifetime.
- Less distortion in output voltage and more reliable converter operation.

Approach

- Layout design of phase leg module using P-cell and N-cell technique, which is the series connection of IGBT and diode, instead of antiparallel connection of IGBT and diode.
- Perform electromagnetic-field simulation of the package to extract the parasitics using Ansoft Q3D Extractor.
- Perform circuit simulations for obtaining switching characterization with package parasitics.
- Use impedance analyzer to measure the parasitics in a prototype phase leg module.
- Use double pulse test (DPT) to experimentally test the switching behavior of the phase leg module.

Major Accomplishments

- Modeled package for phase leg module using Ansoft Q3D Extractor and obtained the parasitics in the module.
- Conducted double pulse testing using Saber simulator.
- Observed "turn-on" and "turn-off" switching behavior and analyzed the effect of the parasitics during switching.
- Fabricated the prototype of the power modules, obtained the steady state characteristics, and measured the parasitics (stray inductance and resistance).

Future Direction

- Build a DPT circuit to test and compare the conventional and proposed modules in terms of switching behavior, voltage (or current) stress, and ringing.
- Design single phase leg module with paralleling devices by using novel switching cell and conventional cells.
    - First, devices with positive coefficient will be selected.
    - Second, layout design and parasitics extraction will be performed using Q3D.

  - — Third, electrical behavior will be investigated by Saber simulation.
  - — Finally, two power modules with paralleling devices (one with conventional approach and one with new proposed approach) will be fabricated and experimentally compared.
- Extend the packaging design approach to three phase power module.
- Summarize and generalize the packaging design approach for P-cell and N-cell based power module.

Technical Discussion

Parasitics are a major concern in design and layout of IGBT packages and power stages with both high switching speed and high power handling requirements. In HEVs, this problem is especially important because of the high power rating and harsh working environment. The goal of this project is to reduce the stray inductance in a power module, improve the switching behavior of the power module, and improve the reliability and performance of the converter. To address the goal, we use the concept of the basic switching cells to package a phase leg module instead of the conventional antiparallel cell. The rearrangement of the layout of the phase leg module reduces the physical distance of a commutation loop so that the stray inductance is reduced.

Packaging Electrical Layout Considerations

Power electronics packaging technology has been developed for several generations, involving material upgrading, structure improvement, and inter-connection technique innovation. Several packaging technologies exist, and each has its own merits. However, currently, wire bonding technology is still the dominant method for commercial power modules, because of its maturity and reliability.

Figure 1 is a diagram showing the layers in an IGBT power module. The base layer, called the baseplate, is a thick layer of metal used for mechanical fixation. Direct bonded copper (DBC) is soldered to it. Power semiconductor dice and terminals are then soldered on top of the DBC. Aluminum wires are used for interconnection of dice and terminals. The module is then put in a plastic case. The case is infused with silicone gel for protection and insulation.

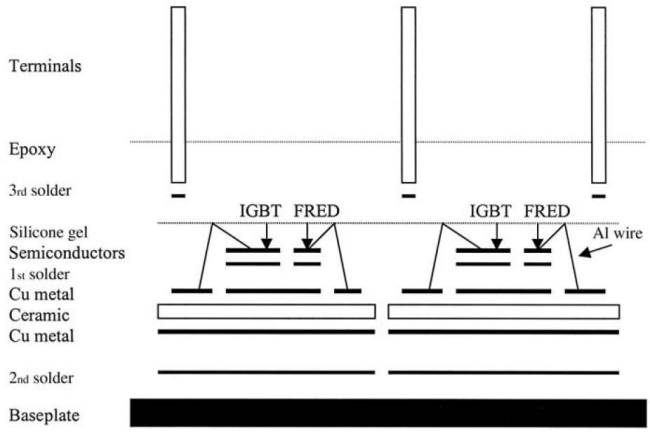


Fig. 1. Structure of an IGBT module. {*Source:* [1].}

In a wire bonding power module, terminal leads, bonding wires and DBC substrate all introduce stray inductance. For example, in a 300 A, 1,200 V, commercial power module, the terminal leads have inductance at the level of 30–40 nH, bonding wires have 10–15 nH, and substrate traces have 4–7 nH [2]. The parasitic inductance stores energy whenever the current flows through the interconnections inside the module when the IGBT is on. When it is turned off, the energy is released directly as a voltage spike and oscillation.

A scenario that is commonly used to explain the IGBT failure during thermal cycling is the coefficient of thermal expansion mismatch between the semiconductor dice and the DBC substrate. Actually, failures can be caused by the parasitic effects, and the performance of the device is limited by the parasitics. One of the examples is the IGBT or diode turn-off *dv/dt* spike, which is a function of total dc loop inductance. It can be controlled by the gate resistance of the IGBT, but slowing down the switching causes high turn-

on loss. After the IGBT fails, it is commonly found that one or two bonding wires were opened or the chip surface at the bonding joints is cracked.

High reliability and long term stability are essential in high power applications; therefore, reducing package stray inductance is an important issue. Several considerations and improvements in the structure of the package can reduce the parasitics of the module. They are discussed in the following paragraphs.

1. Terminal arrangement
As discussed above, in a power module the dominant stray inductance is the terminal. A laminated structure has smaller self-inductance, and also, when paralleling the positive and negative terminals, it enables the coupling of the two inductors to the greatest extent. The equivalent loop inductance equals the two self-inductances minus the mutual inductance. A larger mutual inductance will give smaller total equivalent loop inductance. When designing the terminals, the best way is put two parallel laminated bus bars as close as possible.

2. Bond wires consideration
The interconnection bond wires should be as short as possible. The direction of substrate current, which flows under the emitter bonding wires, is designed to be opposite to the direction of current flow in bonding wires. This wiring construction on the substrate is also achievable by using multilayered DBC technology. Consequently, the effect of the bonding wires on the module internal inductance can become practically negligible.

3. Use the substrate area
Although the substrate has the smallest inductance, a large substrate area can make the inductance considerably larger. This is especially true for high power modules because the paralleling of the power devices enlarges the substrate area. To accommodate the bonding wire connection, the substrate area has to be larger than the footprint of the semiconductor dice. When designing the substrate layout, maximum use should be made of the full substrate area.

4. The "U-package" technology [3]
In 1996 Mitsubishi made a major improvement on the bus bar structure that reduced stray inductance. The bus bars are molded into the sides of the case, aluminum wires are used to connect the substrate or die to the terminal. This relieves "S" bends that were needed in the electrodes of conventional modules. Elimination of these "S" bends helped to further reduce the electrode inductance. Overall, as a result of these inductance reducing features, the new package has about one third the inductance of conventional modules.

People are making every effort to reduce the stray inductance inside IGBT modules; however, one important issue has been neglected: the effective stray inductance while the module is operating. Stray inductance is everywhere in a module; the focus should be on stray inductance in the conduction path during switching on and switching off. The following sections introduce concepts of two basic switching cells in power converters, reveal the mechanism of how the switching cell works as a functional unit, and show how it can affect power module packaging. The concept and analysis have been verified by simulation.

Concept of Basic Switching Cells

As the basic circuit elements, switching devices [mainly metal-oxide semiconductor field-effect transistor (MOSFET) and IGBT], diodes, and inductors and capacitors are used in power electronic circuits to perform ac-dc, dc-dc, dc-ac, and ac-ac power conversion. On examining the basic building blocks of these power electronics converters, two basic switching cells were proposed in [4,5], as shown in Fig. 2. Each cell consists of one switching device (a MOSFET or IGBT) and one diode connected to three terminals:

(+), (–), and (→) or (←). Each cell has a common terminal which has a current direction shown as (→) or (←) on the schematic. For the P-cell, this common terminal is connected to the positive terminal of a current source or an inductor. For an N-cell, this common terminal is connected to the negative of a current-source or an inductor. The active switching device in a P-cell is connected between the (+) and common terminal, whereas in an N-cell, the switching device is connected between the (–) terminal and the common terminal. Although the switching cells have only two components, they can be connected in different combinations to construct various power electronic circuits.

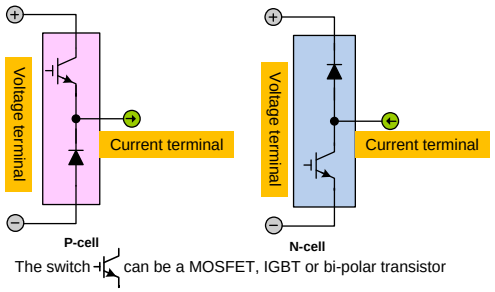


Fig. 2. Two basic switching cells: P-cell and N-cell.

Existing dc-dc converters can easily be represented and configured from the basic switching cells. Also, some new conversion circuits can be derived based on the mirror structure of the two switching cells. Figure 3 summarizes the four classical converters and their cell structures. The leftmost column [Fig. 3(a)] shows the four major classical converters. All of the conventional converters (except the boost converter) have an inherent P-cell structure where the active switching element is connected to the positive power supply terminal [Fig. 3(b)]. The conventional boost converter is inherently an N-cell boost converter.

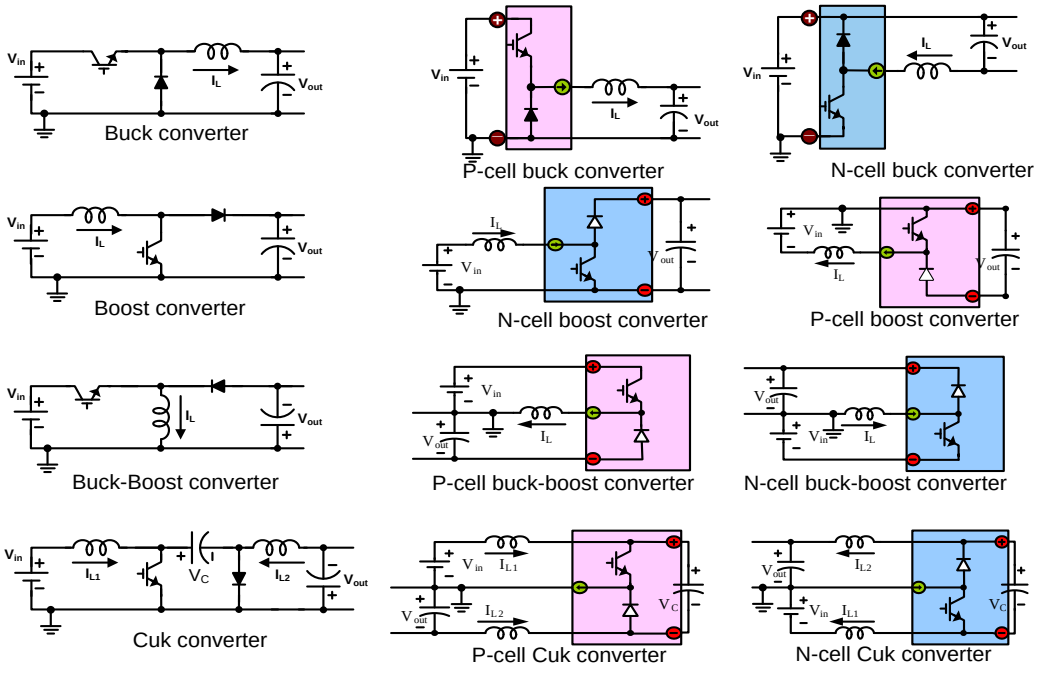
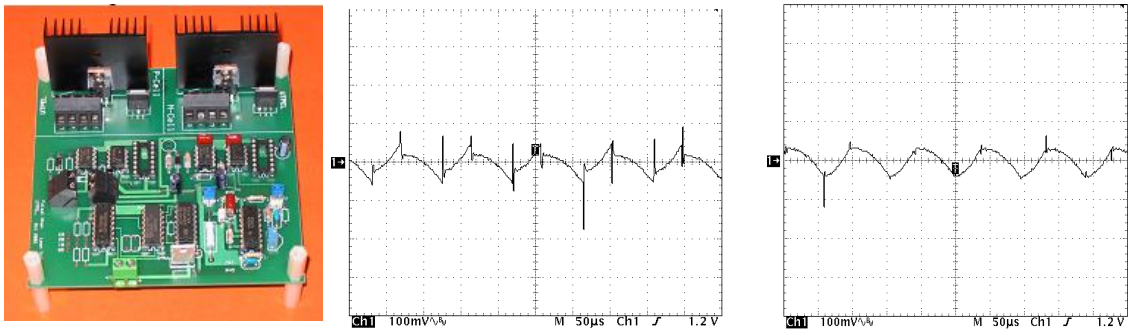


Fig. 3. The four classical converters and their cell structures: (a) classical dc-dc converters, (b) structure of the basic cells, and (c) basic cell mirror circuits.

All of these classical converters also have a mirror circuit representation [Fig. 3(c)]. When the P-cell in a buck converter is replaced with an N-cell, the circuit takes a different configuration. In the same way, the

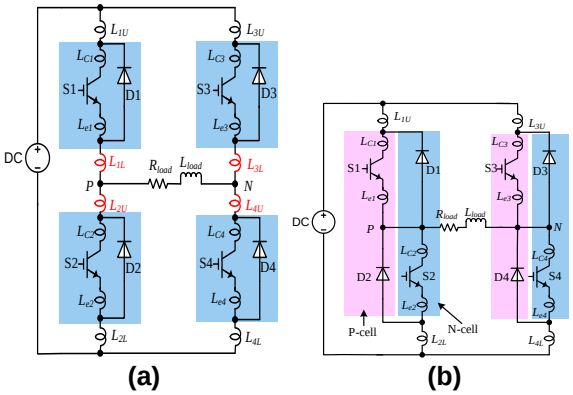
classical boost, buck-boost, and Ćuk converters can be reconstructed using their corresponding mirror cells. The reconstruction of the dc-dc converters using the mirror circuit can introduce advantages in gate drives. For example, in an N-cell buck converter, the gate drive signal is ground referenced so that the converter circuit is more tolerant to supply noise and ripple voltage. The experimental setup for P-cell and N-cell buck converters is shown in Fig. 4(a). As shown in Figs. 4(b) and 4(c), the output voltage is smoother in an N-cell buck than that in a P-cell buck because of the simplification of the gate drive circuit.



(a) **(b)** **(c)**

Fig. 4. Experimental setup for P-cell and N-cell buck converters: (a) experimental prototype of the P-cell and N-cell, (b) output voltage ripple (100 mV/div) of P-cell buck converter, and (c) output voltage ripple (100 mV/div) of N-cell buck converter.

In a traditional phase leg, the basic unit is the antiparalleled switch and diode as shown in Fig. 5(a). However, under induction load condition, current commutation is between S1 and D2 when current direction is from load terminal P to N or between S2 and D1 when current is from N to P. Therefore, in terms of natural current commutation pass, it is more reasonable to construct a phase leg by P-cell and N-cell, as shown in Fig. 5(b). Load current flows into the phase leg through an N-cell and goes out of the phase leg through a P-cell. Figure 5(a) also shows the stray inductance within each phase leg module. This stray inductance model is referred from [6]. L_{1U} and L_{2L} are introduced by terminal leads; L_{1L} and L_{2U} are the stray inductance of the internal bus connecting the upper and lower unit; and the values of these four inductors are relatively large. L_{C1}, L_{e1}, L_{C2}, and L_{e2} are associated with the die and wire bond, which are relatively small.



(a) **(b)**

Fig. 5. (a) Conventional full bridge inverter; (b) phase leg constructed by P-cell and N-cell.

Reorganization of the phase leg can reduce the stray inductance between the two commutation devices. Comparing Figs. 5(a) and 5(b) for the left phase leg, inductances L_{1L} and L_{2U}, introduced by the internal bus, are reduced in the cell structure.

These basic switching cells function as the basic building blocks in power electronic circuits, which cannot be further broken down or apart. They can be used as the basis for manufacturing/layout of single, dual, and six-pack modules that semiconductor manufacturers produce and should be integrated and manufactured as a module, which will have promising application in dc-dc converters and inverters. They not only bring convenience to building dc-dc converters but also reduce the stray inductance between the two devices. Separately packaged devices have stray inductance in both ends due to the package lead, wire bond connection, and external soldering. During current commutation from active switch to diode,

these inductances will cause voltage spikes and oscillations, which are the sources of electromagnetic interference and may even cause damage to the devices under high *di*/*dt* condition. Modularization of P-cells and N-cells can to a large extent reduce stray inductance.

IGBT Module Package Modeling and Parasitics Extraction

To build power modules and verify the concept proposed in the last section is expensive and time consuming. However, this process can be simplified by the aid of the software tool Ansoft Q3D Extractor. The software uses method of moments (integral equations) and finite element methods to compute capacitive, conductance, inductance, and resistance matrices. Providing the correct dimensions, material properties (resistivity of conductors and permittivity of insulators), and boundary conditions (the conductors and current paths), the software can extract the structural impedances of any arbitrary geometry. Thus, the module parasitics can be understood thoroughly before it is manufactured.

The conceptual phase leg modules (Fig. 6) are built using Ansoft Q3D Extractor. For comparison purposes, the two modules are similar in terms of substrate size and lead frame position. (Physical size characteristics are given in Table 1.)

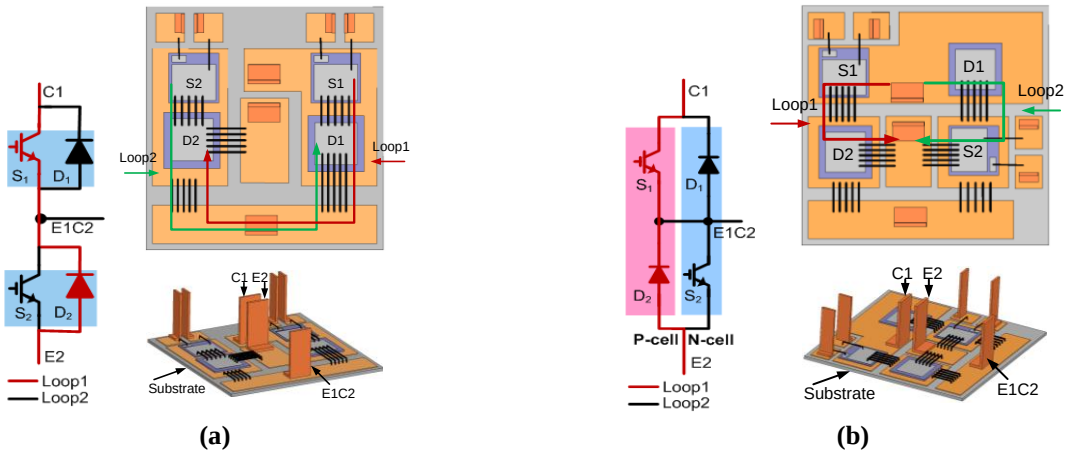


Fig. 6. Phase leg module layout: (a) conventional module layout; (b) proposed module layout.

Table 1. Physical Size of the Two Modules Shown in Figure 6

Component	Conventional module	Proposed module
DBC size (mm)	37.0 × 38.0	37.5 × 38.5
DBC thickness (mil)	8(Cu), 25(alumina)	8(Cu), 25(alumina)
IGBT (mm)	5 × 5	5 × 5
Diode (mm)	5.85 × 5.85	5.85 × 5.85
Bond wires	8 mil × 5	8 mil × 5

Figure 6(a) shows the connection and physical layout of a conventional module, while Fig. 6(b) shows the proposed P-cell and N-cell structure module. The marked Loop1 and Loop2 are two current commutation loops in a phase leg, specifically, from upper IGBT to lower diode and from lower IGBT to upper diode. In a conventional module, the upper leg devices S_1 and D_1 are seated at one side, while the lower leg, S_2 and D_2, are seated at the other side. The physical distance for Loop1 is shown as the red trace. It starts from lead C1, passes through S_1 and two groups of bond wires and output bus E1C2 and then another group of wires to D_2. The length for Loop2 is similar to Loop1. In the proposed P-cell and N-cell modules, the two devices in the commutation loop are seated at the same side; thus, the physical length of the commutation loop is reduced. For example, Loop1 (shown as the red trace) also starts from C1, goes

through only one group of wires, then reaches D_2. This is much shorter than the same loop in a conventional module.

After the geometries of the modules are built in Q3D Extractor, electromagnetic simulation is conducted. A dc excitation source is used in simulation; therefore, skin effect is neglected and the modeled parasitic resistance is smaller than the true value. The simulation results are shown in Table 2. It can be seen that Loop1 and Loop2 inductance are both more than 50 nH in the conventional module, while in the proposed module, the loop inductances are 39.91 nH and 35.18 nH, respectively. As expected, the main reduction is from S_1 emitter to D_2 cathode in Loop1 and from S_2 collector to D_1 anode in Loop2.

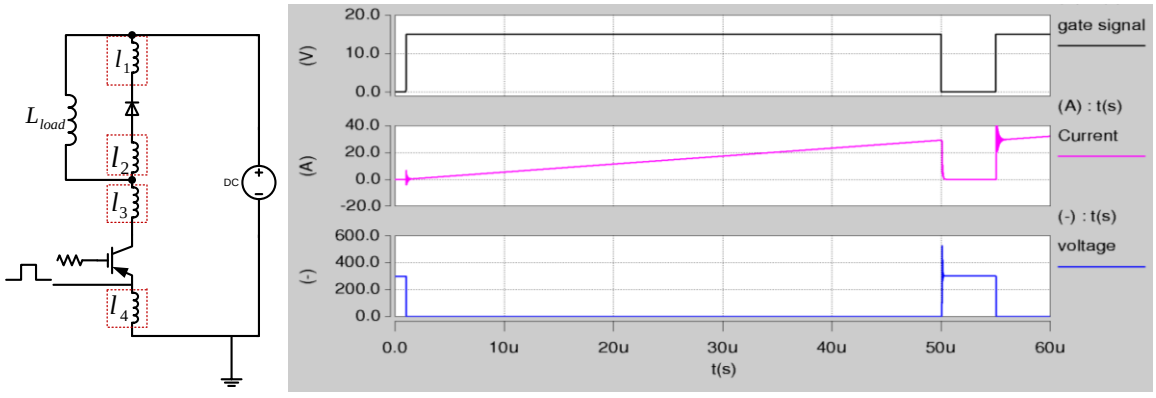
Table 2. Parasitic Resistance and Inductance Extracted from the Power Modules

Circuit	Conventional module	Proposed module
Loop1	8.36 mΩ, 53.06 nH	6.44 mΩ, 39.91 nH
Loop2	7.81 mΩ, 50.67 nH	5.62 mΩ, 35.18 nH
S_1 emitter to D_2 cathode	3.18 mΩ, 20.19 nH	1.26 mΩ, 4.23 nH
S_2 collector to D_1 anode	3.24 mΩ, 20.36 nH	4.04 mΩ, 5.14 nH

Simulation of Switching Characteristics Under Circuit Parasitics

The parasitics in a power electronics module affect the turn-on and turn-off transients and not the steady state performance. After extraction of the module parasitics, mainly the stray inductance, a study was performed to characterize the switching behavior for the two different power module layout cases.

A double pulse tester, shown in Fig. 7(a), was used to obtain the switching behavior under the influence of the module parasitics. It is essentially a step-down converter. The major components include one IGBT and one diode inside the module, an inductive load, L_{load}, the stray inductances extracted earlier (l_1, l_2, l_3, and l_4), and a dc voltage source. Only two pulses are applied to each IGBT; the first pulse is used to obtain the desired current. The switch turns off at the desired current, current commutates to the diode, and turn-off behavior can be observed accordingly. After a short while, the switch is turned on at the second pulse. Because of the large inductive load, the current does not change much, and turn-on behavior under the desired current can be observed. Some typical waveforms are shown in Fig. 7(b) for a DPT implemented in Synopsys Saber.



(a) **(b)**

Fig. 7. Double pulse tester: (a) circuit and (b) typical waveforms.

Table 3. Stray Inductance Used in Double Pulse Tester

	Conventional module	Proposed module
l_{p1}	15.3 nH	15 nH
l_{p2}	10.4 nH	2.07 nH
l_{p3}	10.4 nH	2.07 nH
l_{p4}	20.3 nH	20 nH

The parameters used in the double pulse tester are shown in Table 4. The point-to-point inductances are l_1, l_2, l_3, and l_4 (the loop inductance in Table 2 is the sum of these four inductances). The IGBT and diode are practical models from the Saber library: a Fairchild IGBT rated at 600 V, 40 A, and an IR diode rated at 600 V, 45 A. The simulation is conducted under 300 V, 30 A.

Table 4. Parameters Used in Double Pulse Tester

Parameters	Values
L_{load}	500 μH
IGBT	HGTG40N60B3
Diode	HFA45HC60C
dc source voltage	300 V
l_1, l_2, l_3, l_4 in proposed module	15.0 nH, 2.7 nH, 2.7 nH, 15.0 nH
l_1, l_2, l_3, l_4 in conventional module	15.3 nH, 10.4 nH, 10.4 nH, 15.3nH

Simulation results from the double pulse tester show the advantages of the proposed module compared with the conventional one. The voltage across the IGBT during turn off is shown in Fig. 8. After the voltage rises to the dc link voltage, there is an abrupt drop of the IGBT current and high *di*/*dt* causes a voltage drop across the stray inductance, which causes the voltage overshoot and oscillation as shown in Fig. 8. In the conventional module, the voltage overshoot is 246 V, while the overshoot voltage is 200 V in the proposed module. The overshoot is smaller in the proposed module because the stray inductance is smaller.

During turn on, after the IGBT current reaches the load current, the diode reverse recovery begins, and the IGBT turn-on current has an overshoot. After that, this current rings between the parasitic inductance and the diode parasitic capacitance. This phenomenon is shown in Fig. 9. The overshoot amplitude of the two cases is similar; however, the ringing damps faster in the proposed module as a result of the reduced inductance.

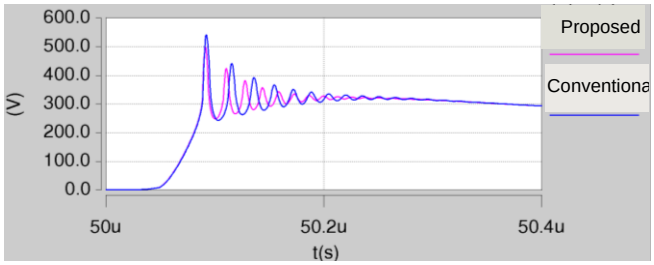


Fig. 8. Voltage waveform across IGBT at turn off.

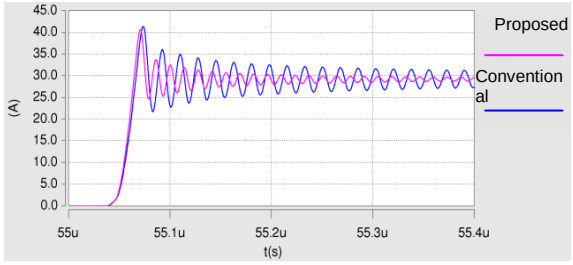


Fig. 9. IGBT current waveform at turn on.

Analysis of Resonance Caused by Parasitics

Oscillation during the turn-on and turn-off processes is triggered by not only the stray inductance but also the device capacitance in the IGBT and diode. The stray inductance introduced by the package and the capacitance of the device compose a resonant circuit that causes the voltage and current oscillation at switching. This section looks into the different current paths during turn on and turn off.

1. Identification of turn-off resonance circuit

The turn-off resonance sets up after the IGBT voltage reaches the dc source voltage; at this time the diode conducts current. The diode body capacitor C_J is bypassed. Resonance occurs between stray inductances, l_{diode} and l_{IGBT}, and the IGBT output capacitor, C_{OES}, as shown in Fig. 10(a). Stray inductance l_{diode} is the sum of the stray inductance connected to the cathode and anode of the diode, and l_{IGBT} is the sum of stray inductance connected to the collector and emitter of the IGBT.

2. Identification of turn-on resonance circuit

The turn-on oscillation occurs after the IGBT current reaches the load current. The voltage across the IGBT starts to drop, while the diode voltage increases. There is discharge current from capacitor C_{OES}; however, because the IGBT is already turned on, this current goes through the IGBT and does not resonate with the stray inductance. The diode capacitor C_J is also discharged; therefore, the resonance is between the stray inductance and C_J, as shown in Fig. 10(b).

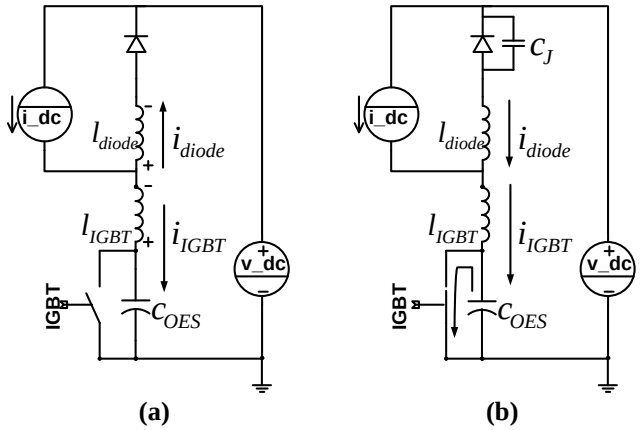


Fig. 10. Turn-off (a) and turn-on (b) equivalent resonant circuits.

Conclusion

As a result of investigating power electronics converters in terms of their topological characteristics and basic building blocks, a new packaging method based on the P-cell and N-cell has been proposed. The modularization of a single P-cell or N-cell increases the convenience of building dc-dc and dc-ac converters. More importantly, the proposed package reduces the parasitic inductance in the commutation loop and suppresses the LCR resonance, consisting of the parasitic inductance in the module and the capacitance in the power devices, during switch turn on and turn off.

Publications

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2.7 Air-Cooled Traction Drive Inverter

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Objectives

- Enable cooling the power electronics with air thereby eliminating the existing liquid-cooled thermal management system.
- Demonstrate the feasibility of air cooling for power electronics through studying component boundary conditions while achieving DOE Vehicle Technologies Program (VTP) 2020 inverter targets for a 55 kW peak/30 kw continuous power rated inverter.
- Reduce the cost for cooling power electronics by eliminating the liquid cooling system.

Approach

- Refine the air-cooled inverter models developed in FY 2009.
  - Perform thermal and fluid simulations on selected inverter architectures to predict the performance of the heat removal system.
  - Improve the geometric and airflow configuration developed during FY 2009 under the Wide Bandgap (WBG) project to improve the performance of the air-cooled inverter.
- Develop knowledge base to define requirements of the components in the inverter to meet VTP 2020 inverter targets (volume, weight, cost) using a baseline inverter design. The project will focus on studying the boundary conditions (such as ambient and inlet air temperatures, air flow rate, etc.) required for a 55 kW peak/30 kW continuous power rated inverter with air cooling.
- Prepare a summary report: A summary of feasibility study results of the air-cooled inverter will be incorporated into the VTP annual report.

Major Accomplishments

- Completed the parametric study of the air-cooled traction drive inverter with two different designs.
- Studied the parameters of the inverter designs for steady state conditions and drive cycle conditions to show the difference in the parameters affecting the air-cooled inverter design.
- Completed the study to determine the feasibility and boundary conditions required for a 55 kW peak/30 kW continuous power rated inverter with air cooling.

Future Direction

- ORNL will wait for the results of balance of plant thermal modeling from the National Renewable Energy Laboratory to determine whether this project should be continued in the future.

Technical Discussion

Parametric studies of two 55 kW peak/30 kW continuous power rated air-cooled inverter designs were conducted to determine their thermal performance and the boundary conditions of the components. The inverters were simulated over a range of parameters such as ambient conditions, inverter voltage, switching frequencies, etc. The two inverter designs are very different in configuration, and the designs will be referred to as design A and design B.

For evaluating their relative performance, both designs use the same number of identical devices, the same power generations curves, and the same materials and material properties. The parameters of the inverter designs were studied for steady state conditions and drive cycle conditions to show the difference in the parameters affecting the air-cooled inverter design. A total of 8 cases of steady state for design A and 24 cases for design B were computed.

A total of 16 combinations of transient performance results were computed using the US06 Supplemental Federal Test Procedure (hereafter US06 drive cycle) current distribution. The details of the technical approach to the design and the results of the simulations are presented below, starting with an overview of the design methodology followed by discussions of design A and design B.

1. Overview of the Design Methodology

The thermal performance of an inverter is based on the heat generated by the losses in devices. The loss models that are used in the inverter design are very critical and significantly impact the design process. In FY 2009, the inverter models used steady power dissipation in the power electronic devices based on the highest estimated losses of a 55 kW inverter obtained from test data. In FY 2010, device power loss equations which are dependent on voltage, current, switching frequency (f_{sw}), and temperature were used in the thermal-fluid simulations of the FY 2010 inverter geometries. These equations were generated from data taken at NTRC from testing the 1,200 V, 100 A, silicon carbide (SiC) metal-oxide semiconductor field-effect transistors and diodes performed under the WBG project. The data can be found in Sect. 4.1 of the annual report. These equations were used in an iterative process, with the junction temperature as the iterated quantity, to determine the steady state temperatures of both inverter geometries. The design methodology of this process is shown as a flowchart in Fig. 1.

Using the power dissipation equations of the SiC devices, the power loss values were significantly higher than FY 2009 models for constant current and voltage under steady state conditions. Having made the models more realistic with junction-temperature-based power losses, a parametric study of differing global inlet temperatures and flow rates was performed to obtain the thermal performance information of a single power module of the inverter. The parametric study was carried out on single power module and not the entire inverter. All the devices in the power module were modeled with their own power dissipation equations and feedback temperature loops to simulate the differing junction temperatures based on device position in the flow field and positioning relative to other thermal generating devices. This type of simulation provided useful information regarding gate driver connection temperatures, capacitor temperature, and phase connection temperatures.

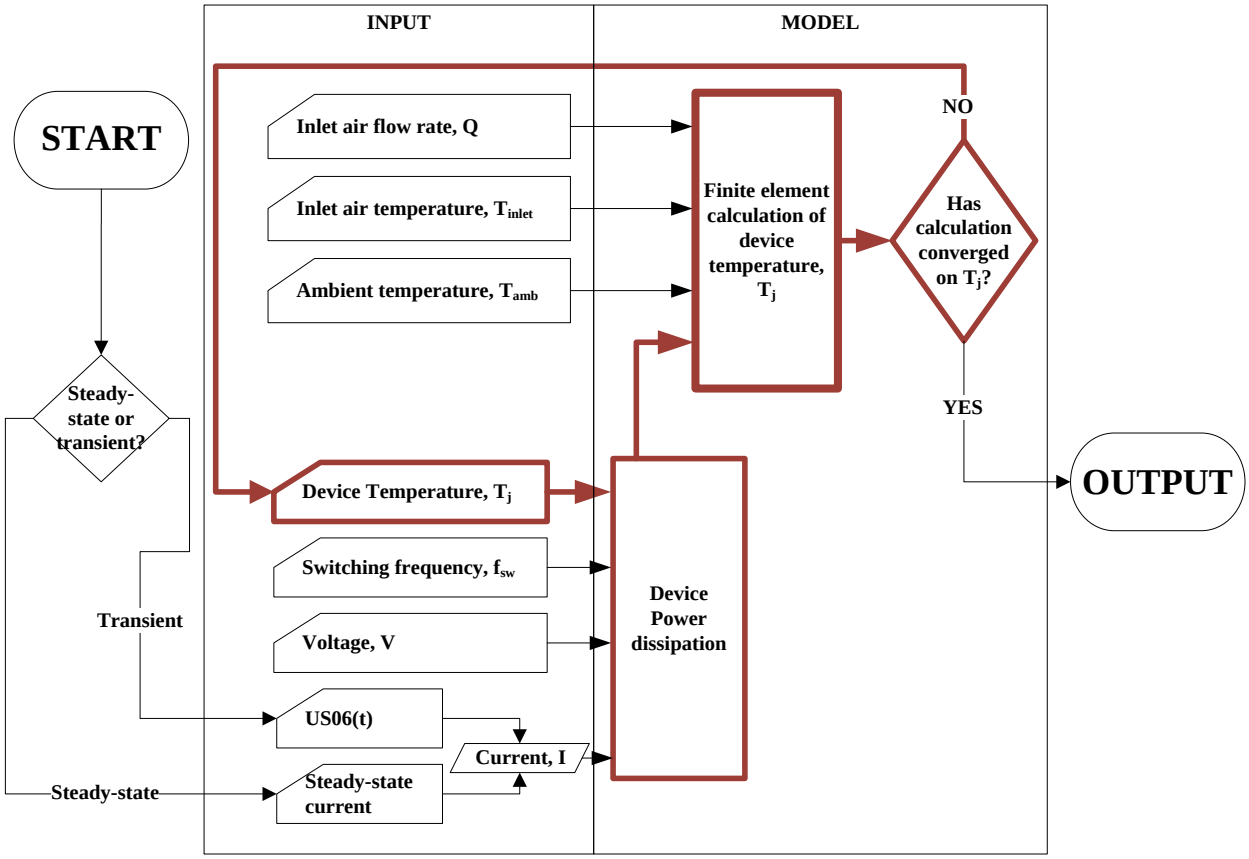

Fig. 1. Flowchart outlining junction temperature iterative procedure.

2. Design and Performance Evaluation: Design A

The overall air-cooled inverter concept was first evaluated in a feasibility study (FY 2009) of a radial-inflow inverter design concept from which the axial inflow inverter design process started. The first objective was to quantify this difference directly. Pressure drop was reduced 13% by simply changing the inlet air flow configuration from radial inflow to a more desirable and natural axial inflow. The design process underwent a series of revisions which were largely governed by the steady state temperature solutions.

2.1 Achieving Low Blower Power Requirements

Because the FY 2009 design had unacceptably high pressure drop and blower power requirements, the present study was focused on reducing them. The main reason for the high pressure drop in the radial inflow configuration is the unusually large area reduction of 90% (i.e., A_{out}/A_{in} = 10%).

Simply changing the inlet air flow orientation from radial in to axial, without reducing the area, and eliminating one turn of the flow reduced pressure drop (ΔP) across the device to 11.8 in. H_2O, which is an improvement of 11%. The results for the final configuration used in FY 2010 are shown in Fig. 2.

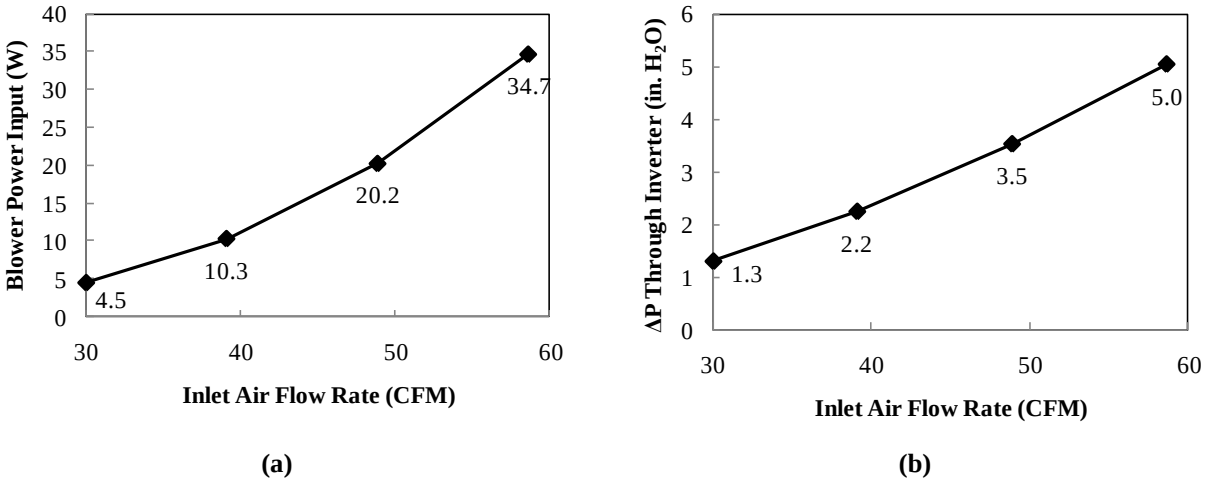

Fig. 2. Ideal blower power input (a) and ΔP across the inverter as a function of inlet air flow rate (b).

2.2 Steady State Thermal Modeling Results

For the results presented, power dissipated (E_{gen}) from the SiC power switches and SiC diodes is evaluated within the model as a function of current, voltage, f_{sw}, and device temperature. Steady state results for the final configuration are shown in Table 1.

Table 1. Steady State Temperature Results for Design A for Q = 50 and 60 CFM; V = 650V, I = 240 A, and T_{in} = 50–80°C

Q = 50 CFM				
Inlet temperature (°C)	50	60	70	80
Junction temperature (°C)	274	304	340	387
E_{gen}*(W)*	719	778	852	956
Q = 60 CFM				
Inlet temperature (°C)	50	60	70	80
Junction temperature (°C)	226	248	271	296
E_{gen}*(W)*	635	671	713	761

2.3 Transient Results of Finite Element Method Simulations of the Final Design Module

The transient response of the system is modeled with current as a function of time as provided by the US06 drive cycle. The transient response to the US06 drive cycle was obtained for two air flow rates of 30 and 60 cubic feet per minute (CFM), where 30 CFM represents the lowest cooling capability and 60 CFM the highest cooling of all the flow rates considered.

The parametric results are presented in Figs. 3 and 4. The junction temperature results for the transient models are tabulated in Table 2 for the 16 combinations of input frequency, voltage, ambient temperature (T_{amb}), and air flow rate. For all cases with inlet temperature (T_{inlet}) =50°C and T_{amb} = 120°C, the junction temperature (Tj) at the end of the cycle is always lower than that at the beginning, which is important when considering how the system would respond to multiple cycles. Essentially, the maximum temperature at the end of a cycle will not exceed 164°C for any number of cycles. For the input parameters described, the power density is calculated to be 12.4 kW/L (excluding the capacitor volume) based on 650 V bus voltage and 240 Arms output current.

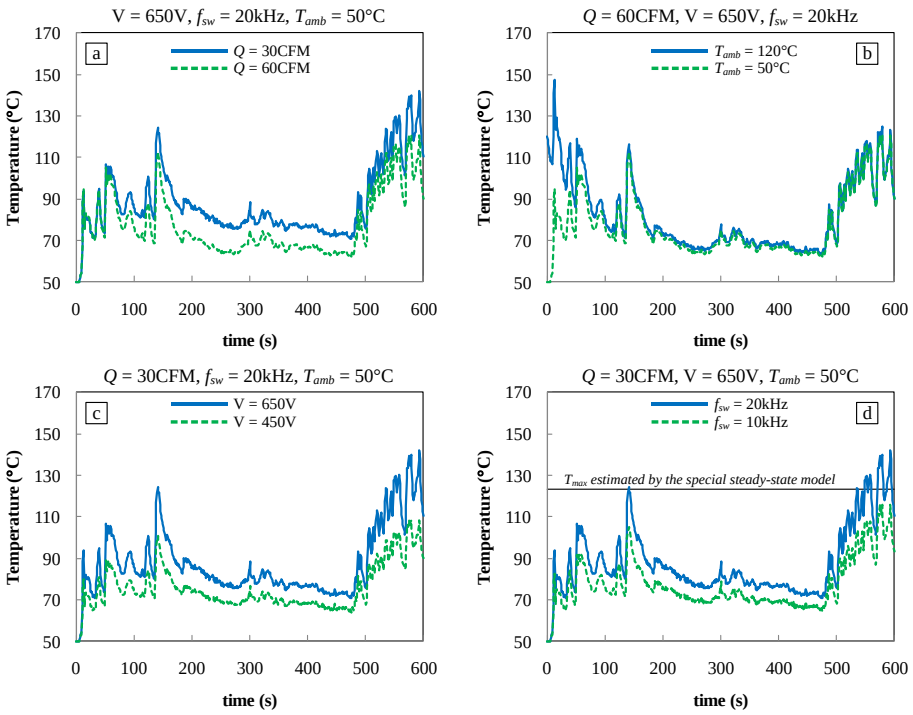

Fig. 3. Transient results for design A showing the effect of changing *Q*, T_{amb}, V, and f_{sw}.

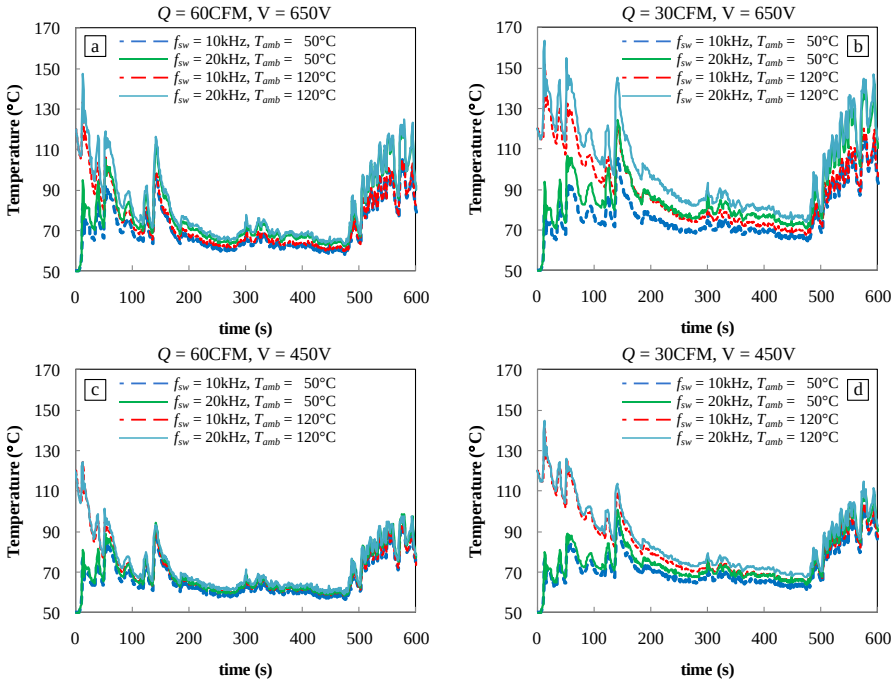

Fig. 4. Results of all 16 transient simulations of the US06 drive cycles for design A.

Table 2. Tabulated Results for all 16 Transient Cases of Design A

	Input parameters				Results
Case number	***Q*** **CFM**	T_{amb} **°C**	**V** **V**	***f*** **kHz**	***Max*** T_j **°C**
1	30	50	450	10	103
2				20	108
3			650	10	116
4				20	142
5		120	450	10	142
6				20	145
7			650	10	152
8				20	164
9	60	50	450	10	92
10				20	99
11			650	10	105
12				20	121
13		120	450	10	124
14				20	125
15			650	10	133
16				20	147

3. Design and Performance Evaluation of the Inverter: Design B

Design B is a new inverter design with a geometry that is different from design A. It was developed as an alternate solution to lower the blower power requirements below that of design A. However, for evaluating the relative performance of both designs, the same number of identical devices, power generations curves, materials and material properties are used in both designs.

3.1. Steady State Results of the Finite Element Simulations of the Final Module Design

The results for the finite element simulations of the three-dimensional (3-D) fully turbulent flow domain through the module are presented in Table 3. From Bernoulli's equation, we know that $\Delta P \sim \Delta Q^2$. The results from the simulations are consistent with this theory. A curve fit of the data with a quadratic polynomial yielded a coefficient of determination of 0.9991. The temperature results of the parametric study are presented in Table 4.

Table 3. Results for the Ideal Blower Power Requirements to Drive the Flow Field

Q per Module (CFM)	30	40	50	60	70	80
Q for Entire Inverter (CFM)	270	360	450	540	630	720
Inlet Velocity (m/s)	3.38	4.51	5.63	6.76	7.89	9.02
ΔP Across the Entire Inverter (Pa)	109	187	292	411	550	708
Ideal Blower Power for the Entire Inverter (W)	13.9	31.8	62	104.7	163.5	240.6

Table 4. Steady State Temperature Results for V = 650 V, I = 240 A, and T_{inlet} = 50 to 85°C

Q = 40 (CFM)								
T_{inlet} (°C)	50	55	60	65	70	75	80	85
Tj (°C)	252	264	276	288	302	315	330	346
$\dot{E}_{gen}$ (W)	730	753	777	804	831	862	892	932
Phase connection (°C)	159	168	177	185	195	204	214	225
Gate connection (°C)	165	173	183	191	201	211	221	232
dc connection (°C)	131	138	145	153	161	169	177	187
Capacitor (°C)	127	134	142	149	157	165	173	182
Q = 50 (CFM)								
T_{inlet} (°C)	50	55	60	65	70	75	80	85
Tj (°C)	206	215	224	234	243	253	263	274
$\dot{E}_{gen}$ (W)	646	662	679	696	713	732	752	773
Phase connection (°C)	126	133	140	147	154	161	169	176
Gate connection (°C)	134	141	148	155	162	170	178	185
dc connection (°C)	105	111	118	123	129	136	143	149
Capacitor (°C)	102	108	115	120	126	133	140	146
Q = 60 (CFM)								
T_{inlet} (°C)	50	55	60	65	70	75	80	85
Tj (°C)	184	193	201	209	218	227	235	244
$\dot{E}_{gen}$ (W)	610	624	638	652	667	683	699	716
Phase connection (°C)	111	117	124	130	137	143	150	157
Gate connection (°C)	119	126	133	139	146	153	160	167
dc connection (°C)	93	99	105	110	116	122	129	135
Capacitor (°C)	91	96	102	108	114	120	126	132

3.2. Transient Results of Finite Element Method Simulations of Final Module

A total of 16 different transient cases were simulated, comprising all possible combinations from two selected values for each of four parameters of interest. They are the volumetric flow rates of air at 30 and 60 CFM, voltages of 450 and 650 V, f_{sw}s of 10 and 20 kHz, and T_{amb}s of 50°C and 120°C. In all cases studied, the maximum Tjs reported in Table 5 are for the single device temperature, which was the maximum. The results of these simulations can also be seen in Figs. 5 and 6. All of these results are for T_{inlet} = 50 °C.

Note that the effect of changing T_{amb} has no significant effect on Tj at the end of the cycle, as can be seen in Fig. 5(b). This is a very significant result. Furthermore, the maximum temperature for all cases with $T_{amb} = T_{initial}$ = 120 °C occurs near the beginning of the cycle, as it was thermally soaked at this temperature. However, because T_{inlet} = 50°C (122°F) is lower than $T_{initial}$, the air flow cools the system and temperatures decrease beyond the initial peak values while the current levels are decreasing. Toward the end of the cycle when the current increases, the temperature begins to increase again. However, Tj at the end of the cycle is far below the peak value at the beginning of the cycle. The end-of-cycle Tj values are much closer to end-of-cycle Tj values for the $T_{amb} = T_{initial}$ = 50°C cases. In contrast, for the $T_{amb} = T_{initial}$ =

50°C cases, the maximum temperatures occur toward the end of the cycle in response to the increasing current.

Table 5. Transient Simulation Results of Design B for Operation Under US06 Drive Cycle

Case Number	Q (CFM)	Voltage (V)	Tamb (°C)	f_{sw} (kHz)	Tj (°C)
1	30	650	50	10	94
2				20	111
3			120	10	136
4				20	146
5		450	50	10	86
6				20	91
7			120	10	130
8				20	132
9	60	650	50	10	89
10				20	98
11			120	10	128
12				20	138
13		450	50	10	80
14				20	83
15			120	10	122
16				20	125

The maximum temperatures reported in Table 5 are valid for the simulations of the US06 drive cycle, but only for the first cycle. If these simulations are repeated sequentially, for more than one cycle, the maximum temperature results of all successive cycles after the first cycle (a) would be independent of T_{amb}, (b) would occur at the end of the cycle as in the T_{amb} = 50°C case, and (c) would be nearly equal to the value of the T_{amb} = 50°C case.

Increasing the voltage or f_{sw} increases the device temperatures as shown in Figs. 5(c) and 5(d). The shapes of the profiles are nearly identical. Figure 6 shows the results for all 16 transient simulations of the US06 drive cycle. The maximum temperature in these simulations was found to be 146°C.

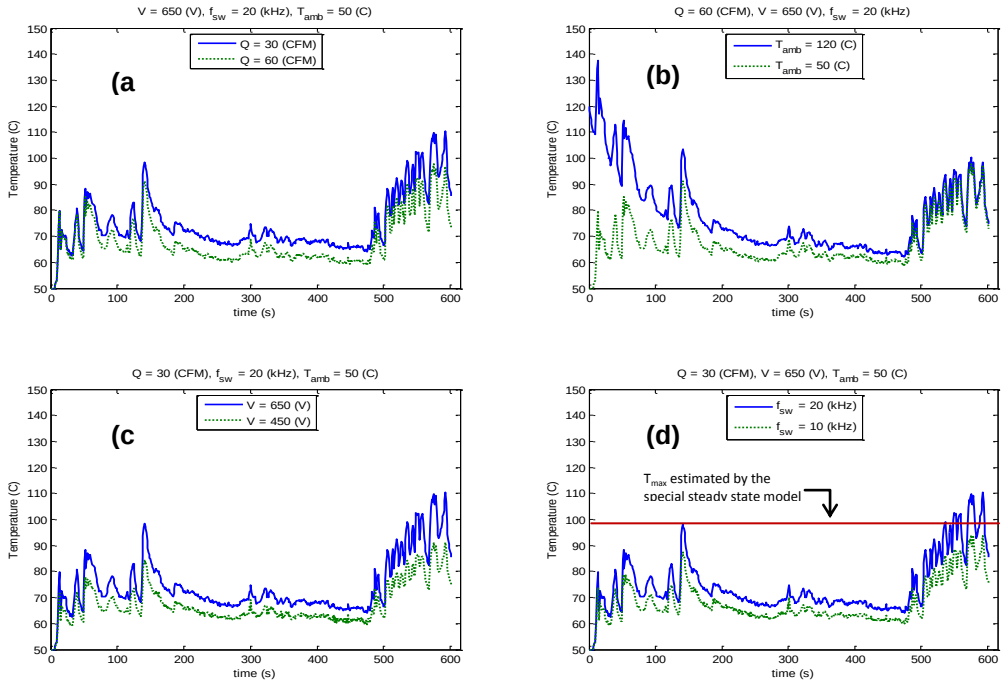

Fig. 5. Transient results showing the effect of changing Q, T_{amb}, V, and f_{sw}.

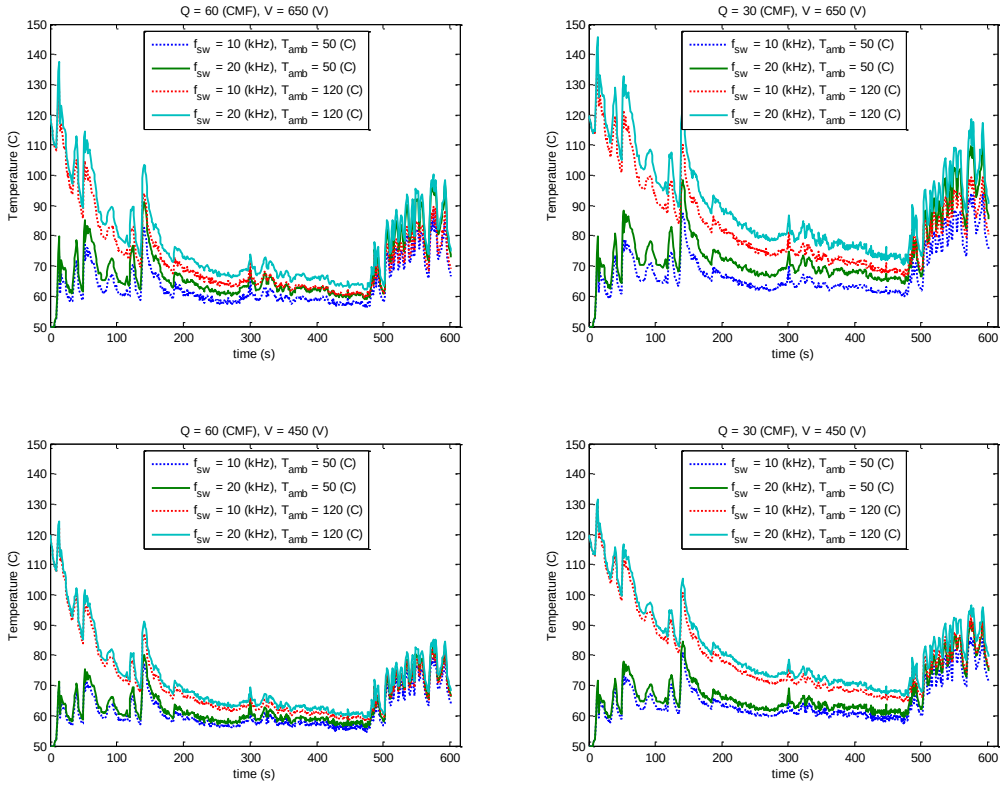

Fig. 6. Plot of all 16 transient simulations of the US06 drive cycle for design B.

From Table 6, which compares the performance of the two inverter designs, we note that (1) the power density ratios for these air-cooled inverters are comparable to those of liquid-cooled systems, (2) both the

pressure drop and the blower power requirements are lower for the lower flow rate and they increase as the square of the flow rate, and (3) the pressure drop and blower power values for design A are about 3 times those for design B.

Table 6. Comparison of the Performance of the Two Inverter Design Packages

Characteristic	Design A	Design B
Power density (kW/L)	12.4	12.01
Pressure drop (in. H_2O) at 30 CFM	1.3	0.436
Pressure drop (in. H_2O) at 60 CFM	5.0	1.64
Ideal blower power (W) at 30 CFM	40.3	13.9
Ideal blower power (W) at 60 CFM	312	104.5

4. Special Steady State Model to Verify Transient Results

Because the overall energy balances for the transient simulations could not be directly evaluated, a check case for the transient simulation results was conceived and implemented. The check case is a special steady state simulation for estimating Tj of all the devices. For this model, the current distribution of the US06 drive cycle, shown in Fig. 7, may be taken to have three distinct patterns: (1) a relatively higher level of current in the beginning up to about 192 s, (2) a lower level of current from 192 s up to a time of 482 s, and, finally, (3) a third higher level of current. An integrated average value of current is computed for the three time intervals, and the results are shown in Table 7 and by the red lines in Fig. 7. The highest of the three currents, 82.45 A, is used in the special steady state model under the most severe of the operational parameters, keeping Tinlet = Tamb = 50°C. The resulting junction temperatures are determined for both designs and compared to those resulting from the full cycle transient simulation (Table 8). As indicated in Table 8, the total power dissipated in this special model is higher than that dissipated over the entire US06 drive cycle.

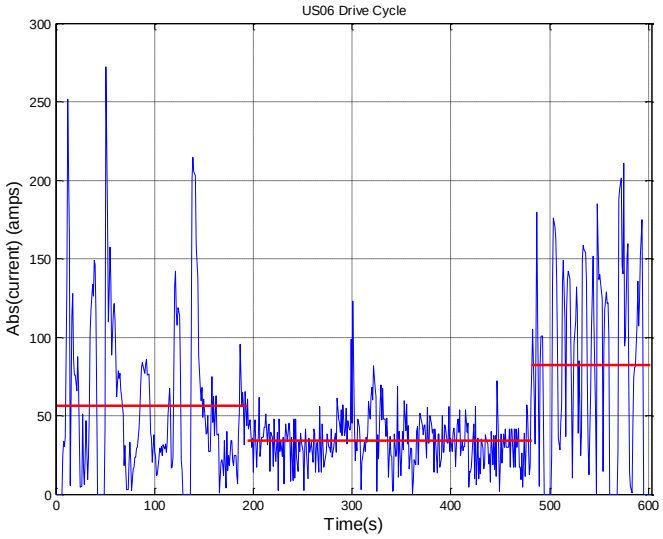

Fig. 7. Current distribution from the US06 drive cycle.

Each of the red lines (Fig. 7) represents the integrated average value over the time interval as shown. Each red level represents the effective steady state current that matches the power dissipation of the time dependent current in the particular time interval.

Table 7. Time-Averaged Values of Current for the Three Time Intervals of the US06 Drive Cycle

	Time Interval in the US06 Drive Cycle		
	1–194 s	194–482 s	482–602 s
Integrated average current (A) through inverter	56.31	34.19	82.45

Table 8. Comparison of Junction Temperature for Three Models[a]

Inverter	Ambient Temperature (°C)	Steady state		US06 drive cycle simple steady state model		Full transient US06 drive cycle
		Current (A)	Tj (°C)	Current (A)	Tj (°C)	Tj (°C)
Design A	50	240	> 274[b]	82.45	123.5	142
Design B	50	240	> 252[c]	82.45	97.8	111

[a]The three models compared in this table are (1) steady state simulation; (2) special steady state simulation; and (3) full transient simulation of the two inverter designs for the most demanding of the parametric cases with V = 650 V, f_{sw} = 20 kHz, Q = 30 CFM, and T_{inlet} = 50°C.

[b]The value for Q = 50 CFM. At Q = 30 CFM, expect Tj > 274°C.

[c]The value for Q = 40 CFM. At Q = 30 CFM, expect Tj > 252°C.

With a current of 240 A, the steady state simulations result in very high Tjs for all cases considered in this study (Tables 1 and 4). However, those temperatures are useful in establishing the upper limit on Tj that the device can reach. In reality, however, the current level will not be constant at 240 A but will be a time dependent function like the US06 drive cycle shown in Fig. 7. For this case the results are compared in Figs. 3(d) and 5(d) for both the inverter designs, design A and design B respectively. The Tj values from the transient simulations are lower than that predicted by the special steady state simulation for the first 550 s of cycle and exceed the predicted value during the final 50 s of the cycle, so the transient results can be considered to be realistic.

Conclusion

In this study two different inverter thermal packages, incorporating new concepts of thermal packaging, were designed, and their thermal performance was evaluated. Full 3-D turbulent-thermal-fluid models were developed. Further, device power dissipation at the individual chip level as a function of Tj, voltage, and current and f_{sw} is included in the models. These effects are included for both the steady state and transient models of the final designs. From the results presented and discussed, the following conclusions may be drawn.

1. For the steady state models with a current of 240 A, Tjs are very high.

2. For the transient models with US06 drive cycle,
   a. Tjs, compared to corresponding steady state models, are lower by about 100°C,
   b. for T_{amb} = 50°C, the highest Tjs occur toward the end of the cycle, and
   c. for T_{amb} = 120°C and T_{inlet} = 50°C, the highest Tjs occur early in the cycle and decrease significantly with decreasing current as a function of time. In the final 50 s of the cycle, Tjs increase to a level below the highest values. The end-of-cycle values of Tj are comparable to those of the case in 2b (above).
3. A special steady state model was developed to validate and provide a means to estimate the expected Tjs from the transient simulations. The results of this simplified model confirmed that the transient model predictions of Tjs are reasonable. As transient simulations require significantly higher computational resources and computational time, this simplified model may be used to estimate Tjs for other drive cycles.

2.8. Power Device Packaging

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Objectives

- Identify the limitations and shortcomings with existing device packaging approaches.
- Develop new packaging concepts to overcome the issues for improved power density, thermal management, cost, and reliability.
- Complement other packaging and thermal management research efforts within the Vehicle Technologies Program (VTP).

Approach

1. Benchmark through analysis and simulation selected state-of-the-art (SOA) commercial device packages. This involves
    1. selecting the SOA commercial packages, such as Toyota's and Semikron's, and
    2. analyzing the selected packages, including module packaging and cooling.
2. Identify underpinning issues with existing packaging.
3. Based on the results of benchmarking, determine why the available technologies are not sufficient to achieve the desired target. (This task focuses on key contributor identification.)
4. Develop and benchmark promising new packaging concepts and technologies through survey, analysis, and simulation.
5. Select and develop candidate technologies.
6. Prepare a summary report that includes evaluation results (incorporate into the annual VTP report).

Major Accomplishments

- Analyzed and summarized the advantages and disadvantages of SOA automotive power modules.
- Benchmarked existing packages by sectioning and constituent characterization of automotive inverter insulated gate bipolar transistor (IGBT) modules.
- Developed a new package concept and performed electrical properties and thermal performance simulations.
- Performed evaluation and down selection of packaging technologies (materials and processes), including die attach, substrate, insulation, and mechanical support.
- Extended the critical in-house packaging capability through integration of on-site packaging facilities.

Future Direction

Develop advanced power module packaging technologies aiming at the following.

- improved electrical performance;
- reliable high temperature operation;
- efficient thermal management (and cooling capability); and
- economic manufacturability;

by

— packaging structure optimization,
— material exploration, and
— processing techniques innovation.

Technical Discussion

1. Introduction

Power semiconductor devices, IGBTs, metal-oxide semiconductor field-effect transistors, and diodes fulfill the role of switching electric power through their fast turn-on and turn-off in tens of kilohertzes in power electronic conversion systems such as motor drives. The core element of these power switches is a small semiconductor die with a dimension of, for example, 10 mm × 10 mm × 0.3mm with rated current/voltage at hundreds of amperes (A) and hundreds of volts (V) for silicon (Si) IGBTs. To facilitate high power conversion configurations such as half or full bridge, three phase, matrix, etc., power modules are constructed by electrically interconnecting multiple dies and then encapsulating to form the building blocks for power conversion systems (converters and inverters). The process from multiple bare semiconductor dies to a module has been called power device/module packaging, as illustrated in Fig. 1(a).

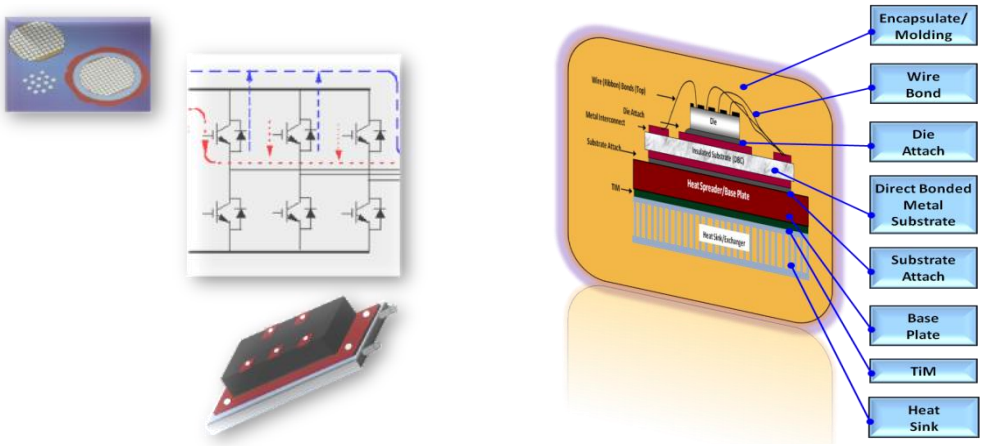


Fig. 1. Power module packaging: (a) from multiple semiconductor chips (dies) to a power electronics building block (not in scale); (b) typical power module packaging structure (inside).

During operation, the dies generate relatively large amounts of heat (on the order of hundreds of watts per die), leading to temperature increases. Semiconductor devices and the associated packaging materials ultimately dictate the inherent temperature limitations. For example, the maximum operation temperature of Si devices is 150°C to 200°C [1], depending on the voltage rating. So refined cooling measures must be taken to control the die's temperature, which leads to strict requirements for a module's thermal performance. In addition, another main function of the module structure is to supply mechanical support for operation under heavy vibration conditions and in harsh environments.

The characterization of power modules' packaging includes specific parameters; for example, thermal resistance, electrically parasitic inductance/resistance, power density, and thermal/power cycling number to failure. All these performance parameters are related mainly to the physical structure and material properties of the power module assembly. These factors, plus associated packaging process technologies, determine the overall cost of the power modules and systems.

To meet these requirements, hybrid packaging technology has been used with diverse materials and process techniques. Figure 1(b) illustrates a conventional wire-bond packaging structure. The bonding wire and solder are used to connect the electrodes on the top and bottom of the die onto the etched circuit of the direct bonded copper (DBC) substrate, which comprises of copper (Cu) bonded with an electrically insulative ceramic plate sandwiched between double side Cu layers. The power and signal input/output are accomplished through soldered Cu terminals on the DBC substrate. This assembly is then soldered onto a flat Cu baseplate and encapsulated in a plastic housing with an electrically insulative polymer (silicone gel) to provide mechanical support, electrical isolation, and protection. This module will then be bolted onto a heat sink or cooler with thermal paste (thermal interface material or TIM) in between to reduce the contact thermal resistance. The module may also be bolted onto a bus bar for a higher level electrical connection.

2. Benchmarking Automotive Power Modules

Advances in power module packaging have been a direct result of modifications to this basic structure. Table 1 gives a few examples of SOA automotive power modules with the results of our analyses. It can be seen that many concepts have been pursued in the quest for improvements in packaging structure, materials, and techniques.

The module in the Toyota LS 600 [2] consists of many packaged switch units based on paralleled IGBT and diode die. These dies are interconnected by direct soldering onto planar electrodes. The dies have solderable front surface metallization (FSM) supplied by Fuji Semiconductor [3]. These switch units are sandwiched between minicoolers with bare silicon nitride, electrically insulative ceramic slices between cooler and electrodes to exploit the thermal advantages of double sided-cooling. However, the double sided thermal grease layers with each ceramic insulator add thermal resistance to each thermal path, negating the positive effects of double sided cooling. In addition, a pressure mechanism must be continually applied to ensure the press contact of all package units and minicoolers. A complicated bus bar is needed for electrical connection of these units. This complex assembly is costly.

In the Prius III (2010), Toyota uses an integrated cooler structure [4] in which the DBA (direct bonded aluminum) substrates are directly bonded (by brazing) onto a specially fabricated cold plate. Compared to the standard module structure, it eliminates the need for a baseplate and TIM layer. It is estimated this construction achieves a 30% improvement in thermal performance. However, to release the stresses between the cooler and DBA due to the coefficient of thermal expansion (CTE) mismatch, a buffer plate with punched holes was inserted. This addition results in processing complexity and worsens the thermal conduction.

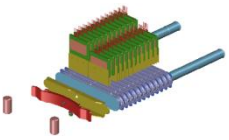
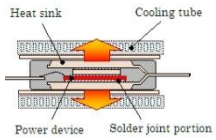
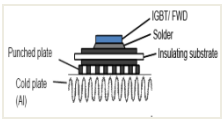
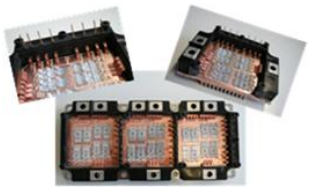
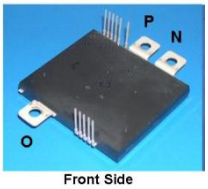
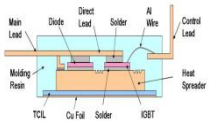
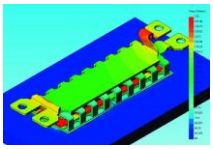
Infineon, a leading power semiconductor manufacturer, has developed power modules for automotive applications [5]. Their Hybidpack2 features a direct-cooled Cu baseplate with pin fins, eliminating the TIM layer and reducing the thermal resistance. In this structure the Cu pin fins baseplate is difficult to manufacture. The O-ring sealing between baseplate and coolant channel is an issue.

Mitsubishi, another major power semiconductor manufacturer, supplied a TPM (transfer-molded power module) [6] for the Honda Insight and other hybrid vehicles. It is a phase leg package and needs further assembly to form inverter modules. It eliminates the DBC substrate and instead uses a thermal conductive

insulation layer (TCIL) sandwiched in between two Cu plates as an insulator and bonder. Double sided planar interconnection has been used by soldering Cu leads on the IGBT/diode dies. Again the dies have solderable FSM. It reduces parasitic electrical resistance (compared to wire bond top interconnection). The disadvantage of this packaging includes poor thermal conductivity of the TCIL layer, and assembly from phase leg package to module requires double layers of TIM. This will worsen the thermal performance.

Semikron, a power module packaging developer, produced their SKiM modules [7], in which the baseplates are eliminated. Press contacts provide both the terminal electrical connection to pads on the DBC and the DBC to heat sink. More remarkably, sintered silver (Ag) has been used for the die attach bonding material, replacing widely used solders. This significantly increases the reliability of the power module thermal cycling; however, the mechanical integrity of the assembly and TIM layer uniformity remain concerns.

Table 1. Features of State-of-the-Art Automotive Power Modules

	Toyota LS600 [2]	Toyota Prius III [4]	Infineon Hybridpack2 [5]	Mitsubishi TPM [6]	Semikron SKiM [7]
Module	 	 	 	 Front Side 	 
Advantage	• Double sided planar interconnection; • No baseplate; • Double sided cooling	• Direct bond cooler • No baseplate • No TIM layer • Al Ribbon bond	• Direct cooled baseplate • No TIM layer • Integrated cooler	• No DBC substrate • Phase leg unit • Direct planar lead bond	• No baseplate • Press contact • Ag sintered die attach
Disadvantage	• Complex inverter (electrical and thermal) assembly • Ceramic slice insulation and double TIM layers	• Stress relax buffer layer worsens thermal conductivity • Large electrical parasitic parameters	• Difficulty in pin fin manufacture • Large electrical parasitic parameters • Difficult integration of cooler	• Double TIM layers • Poor thermal of TCIL • Module level assembly needed	• Mechanical integrity concern • Large electrical parasitic parameters • Poor TIM layer uniformity

To further understand the details of these modules, advanced microstructure chemical analyses (energy dispersive spectroscopy, elemental mapping, etc.) and scanning electron microscopy technologies have been used. Figures 2–5 present some examples of the microstructural and chemical analysis results. Figure 2(a) shows the package in the Toyota LS 600 module, and Fig. 2(b) is a cross-sectional view of a double sided planar interconnection and paralleled IGBT and diode die. Figure 2(c) shows the die attach structure at a high magnification, where a Cu shim and dimples (for stress release) can be seen. Figure 3 shows the Toyota Prius III module's microstructure. The cross section is shown in Fig. 3(a). It is a

complete integrated stack from semiconductor die to cooler configuration. Figure 3(b) presents the chemical constituents of the die attach solder layer, which is clearly lead free. Figure 3(c) features a highly magnified portion of the multilayer aluminum (Al) construction, including the directly bonded interface between the DBA and laminated cooler. Al-2 is a machined Al slice with punched holes, as shown in Fig. 3(d), which is designed to promote passive stress relaxation within the structure. Figure 3(e) shows the chemical composition of finishing metallization on the DBA substrate, which must be metallurgically compatible to solder. Figure 4 shows the Mitsubishi TPM module's microstructure. The IGBT and diode dies are directly attached onto a thick (3 mm) Cu plate with multiple dimples for stress release, as shown in Fig. 4(a). Figure 4(b) presents the cross-sectional view of the die attach solder layer, where voids can be clearly observed. Figures 4(c) and 4(d) are the microscopic view of the molding compound and TCIL, respectively. The TCIL's measured thermal expansion property is illustrated in Fig. 4(e), where the nonlinear behavior can be observed. Figure 5 shows the metallurgical details of die attach in the Semikron SKiM module. The sintered Ag layer for bonding includes Al, Mg, Si, and oxygen additives. After sintering, there is a transition zone from die bottom metallization to the Ag layer in which the constitution elements, including titanium, nickel, Al and Ag, are gradually changed. The same analysis has also been performed on the Ag to substrate interface.

Fig. 2. Toyota LS600 module planar interconnection structure: (a) unit package, (b) cross-sectional view, and (c) shim and dimples.

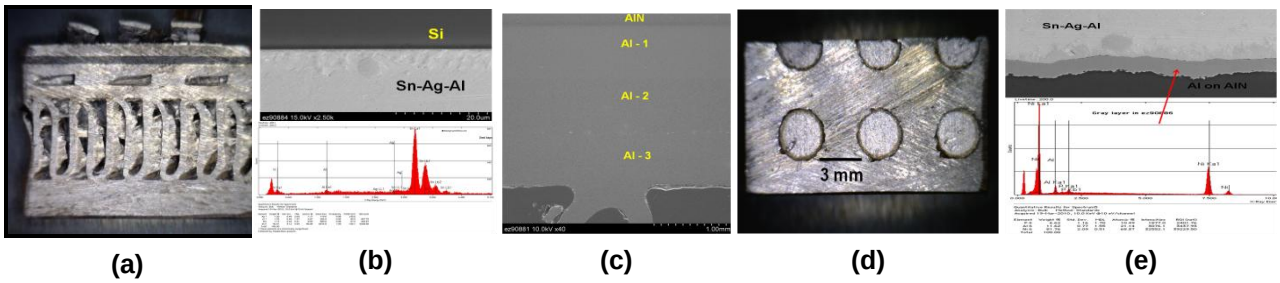


Fig. 3. Toyota Prius III module microstructure: (a) cross section, (b) solder elements, (c)multiple Al plate stack, (d) stress release holes, and (e) metallization finish on DBA substrate.

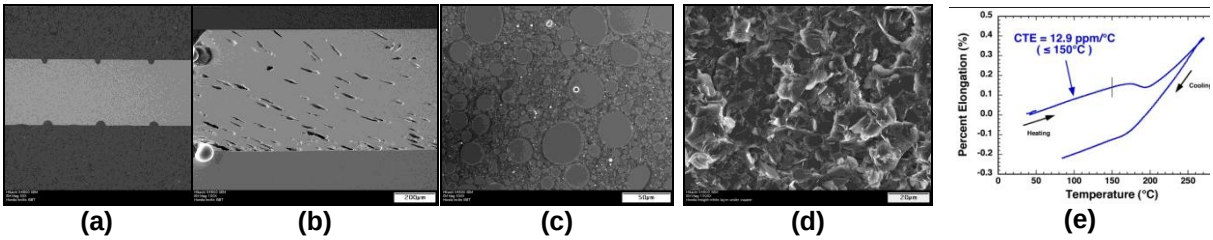


Fig. 4. Honda Insight (Mitsubishi TPM) microstructure: (a) dimple in heat spreader, (b) voids in solder layer, (c) molding component, (d) TCIL, and (e) thermal expansion of molding component.

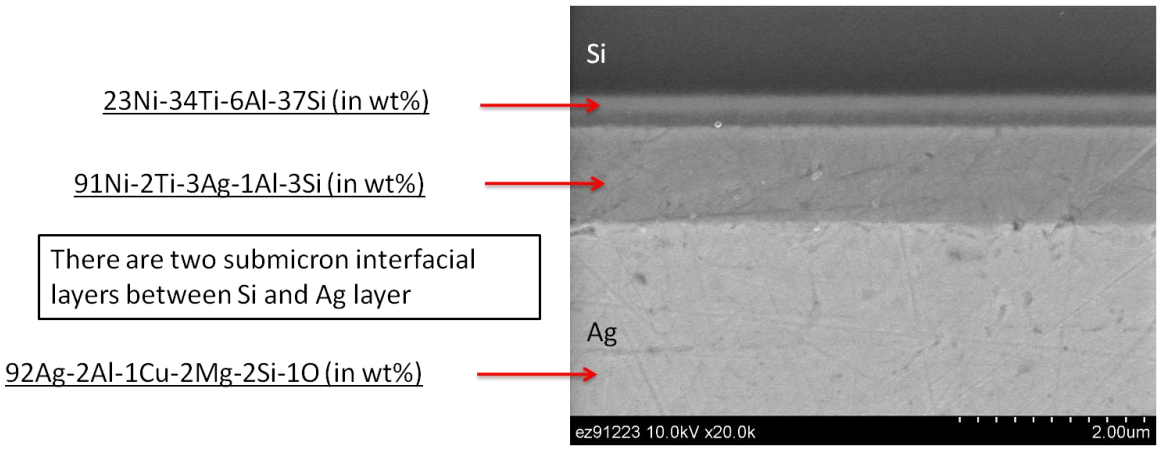


Fig. 5. Semikron SKiM die attach metallurgical scheme.

The parasitic electric parameters (inductance and resistance) with specific packaging electrical interconnection configurations are important characteristics of a module's packaging. They can be obtained by electromagnetic simulation of the packaging structure. Figure 6 shows the simulation results for the module in the 2007 Toyota Camry Hybrid. The electrical interconnection consists of bond wires and Cu traces on the DBC substrate, as illustrated in Fig. 6(a). The extracted electric circuit parameters are depicted in Fig. 6(b). The larger these parameters are, the greater the negative impact on system operations.

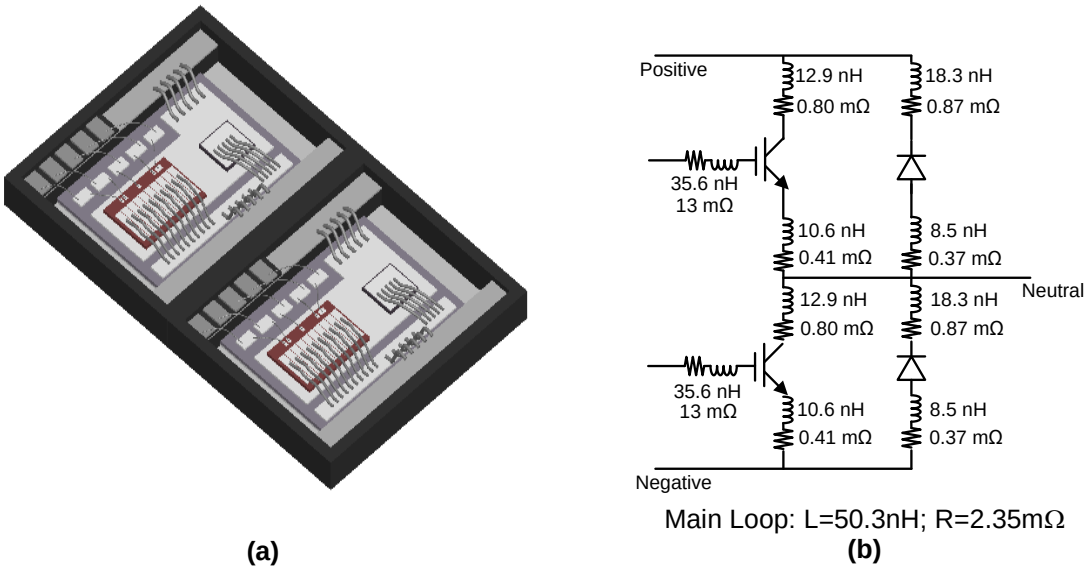


Fig. 6. The electrical parasitic parameters extraction of the 2007 Toyota Camry module: (a) electrical interconnections and (b) parasitic parameters in the converter circuit.

3. New Power Module Packaging Concept

As indicated in the previous section, the automotive power electronics module has undergone intensive development. Each one of these diverse products offers incremental improvements to the baseline, conventional automotive electronics module through different packaging technologies. However, none of them offers comprehensive features that are optimized for all aspects of performance, reliability, and cost effectiveness. To meet targets for advanced automotive power electronics, a more integrated design scheme should be pursued. In FY 2010, we developed a module concept that features (1) easy inverter/converter integration, (2) ultralow thermal resistance, (3) ultralow electrically parasitic parameters, and (4) low manufacturing costs.

The following are the electrical parameters associated with the major commute loops of the ORNL concept packaging module in comparison to the module in the 2007 Toyota Camry Hybrid.

- Parasitic inductance for the ORNL module is 12.8 nH vs 50.3 nH for the Camry module.
- Parasitic resistance is 0.22 mΩ (ORNL) vs 2.35 mΩ (Toyota).

There is a much greater reduction in parasitic inductance and resistance compared to Toyota's wire bonded module because of the special interconnection used in the ORNL design. The smaller electrical parasitic parameters will not just improve the conversion efficiency of the system, but also can reduce use of the semiconductor die, the most costly part in the module, through reduction in both voltage and current rate.

The semiconductor cost can be further reduced through decreasing the thermal resistance of the packaging stack while maintaining the use of the same cooling capability. We have designed two different integration schemes between substrate and cooler. The finite element analysis thermal simulation results demonstrate that 60% improvement of thermal performance can be achieved.

Increasing the operational temperature of semiconductor dies in modules is a promising approach to reduce the power electronics system cost further. Currently, the IGBT and diode are rated for continuous operation at 125°C. Recently this temperature has been increased to 170–200°C for Si switches. Wide

bandgap semiconductor [e.g., silicon carbide (SiC), and gallium nitride (GaN)] switches offer higher temperature capability (>300°C). This advance has thus transferred the challenge to the power device/module packaging because the ambient temperature and temperature excursions are two major sources of module failure. It is well known that different thermal expansion rates of adjacently bonded parts cause fatigue and cracking into the bonding layer because of material CTE mismatches. A successful power module packaging design must consider matching (or minimizing the differences) of all material CTEs. Figure 7 illustrates the thermal properties (thermal conductivity and CTE) of conventional power module packaging materials.

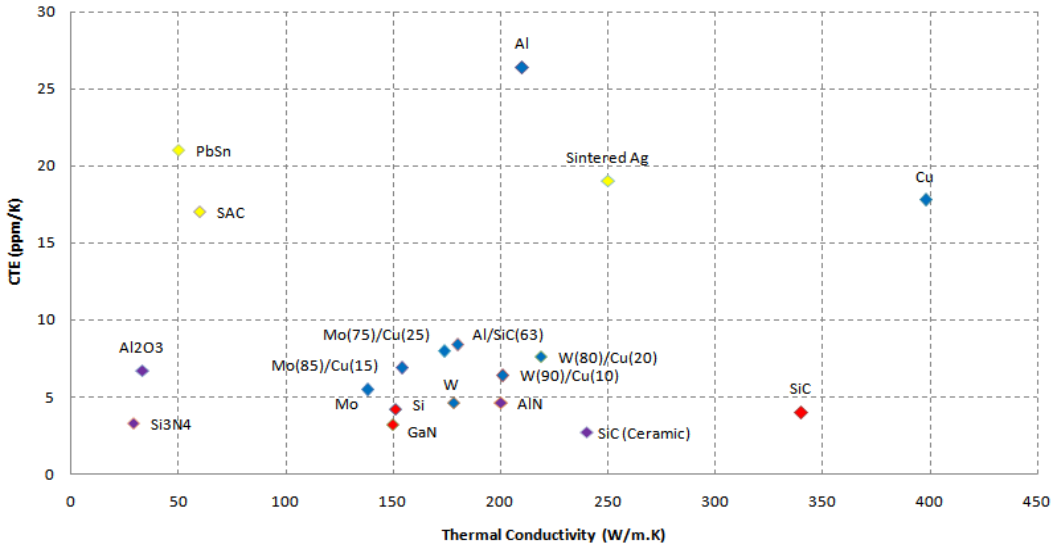


Fig. 7. Thermal properties of power module packaging materials.

The CTE values of Si, SiC, and GaN are in the range of 3.2–4.2 × 10^{-6}/K (or ppm/K). Ceramic materials such as alumina (Al_2O_3), aluminum nitride (AlN), and silicon nitride (Si_3N_4) are used as insulation substrates where the substrate's apparent CTE ranges from 3.3 to 6.7 ppm/K, values close to those of the candidate semiconductors. However, most metals used as electric conductors and/or bonding media possess much higher CTEs; for example, Cu (17.8 ppm/K), Al (26.4 ppm/K), and solder (17–21 ppm/K). There are two ways to deal with CTE mismatch problems. One is to optimize the structure to release or minimize the thermal stress, such as in the Prius III, TPM, etc. Another is to use advanced materials with CTEs closer to the die's such as aluminum silicon carbide, AlSiC, (8.4 ppm/K); MoCu (6.9 ppm/K); and MoW (7.0 ppm/K), especially for high temperature modules.

4. Development of the Silver Sintering Die Attach Technique

Solder and soldering have been widely used for die attach and substrate attach. For automotive applications, the formed joint must withstand large stresses and strains under high power/thermal cycling operating conditions. To meet this high reliability requirement, the Ag sintering joining technique is undergoing scrutiny in-house. Figure 8 shows the experiment equipment and initial samples we have made. A small-scale model sintering facility with local heater and pressure control has been fabricated [Fig. 8(a)]. The heater and piston for pressure application and a sintered bulk Ag disk produced in the facility are shown in Fig. 8(b). The disk is ready for material property examination including modulus of elasticity, CTE, and thermal conductivity as a function of porosity and temperature. These parameters are related to the processing temperature profile and pressure applied; a typical example is shown in Fig. 8(c). Based on the bonding mechanism of Ag sintering, the surface finish metallization plays an important role. Various metallurgical schemes have been studied. The silver pastes from different vendors have been

examined. Figure 8(d) shows a furnace acquired for future module level Ag sintering processing, which will be located in the ORNL Power Electronics Packaging Laboratory.

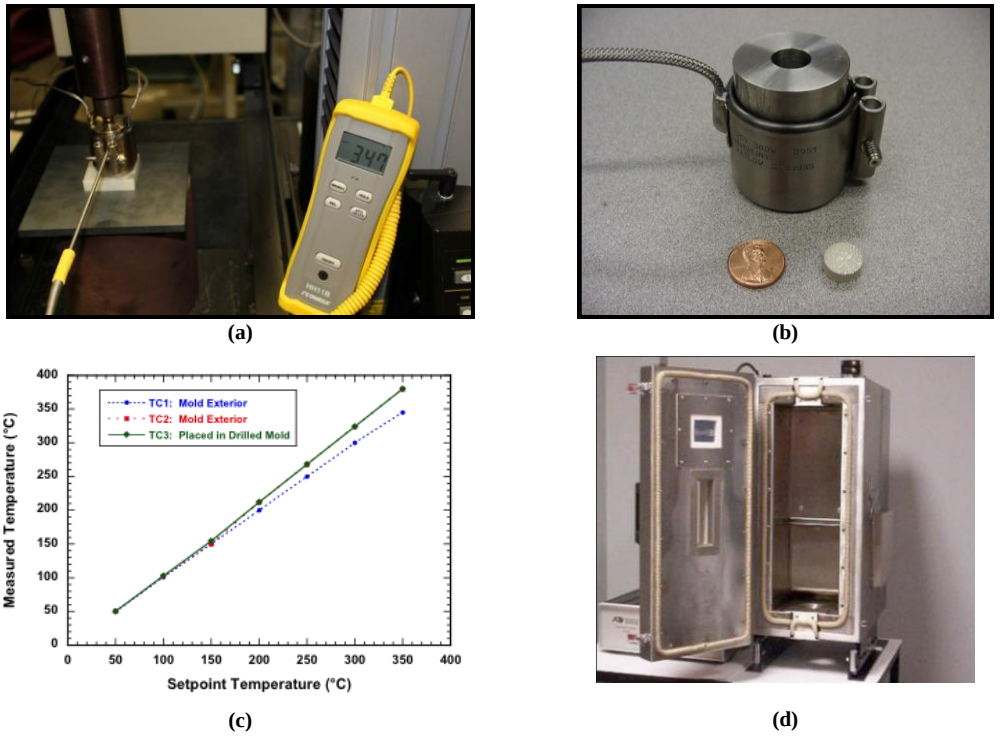


Fig. 8. Silver sintering technology development for die and substrate attach: (a) ORNL model sintering facility, (b) fixture and sintered silver disk, (c) temperature validation, and (d) furnace for module-level fabrication.

5. Integration of Power Electronics Packaging Laboratory

Power module packaging manufacturing is a combination of several hybrid processes, as indicated in Fig.1. To extend ORNL's research capabilities in power modules and power electronics systems, we designed and acquired a suite of equipment for different packaging processes: clean storage/operation station (N_2 purged desiccators cabinet, laminar flow ESD clean bench), chemical processing station (fume hood, etching bath, ultrasonic cleaning, electro-, electro-less plating machine), pattern and selective deposit (spin coating machine, ultraviolet exposure, paste screen/stencil printer), die/substrate attach (vacuum reflow furnace, dual heating reflow oven, pressure-assisted sintering oven), wire bond (thick wire/ribbon bonder), encapsulation (dispensing machine, de-air pump, curing oven), process qualification (microscopic observation, probe station, and curve tracer), and environment chamber (thermal shock and thermal cycling ovens). A dedicated laboratory has been built to facilitate module packaging processing. Figure 9 illustrates the layout in this laboratory with pictures of the major equipment.

Fig. 9. Power module packaging process facilities and layout in a specially built laboratory.

Conclusion

In FY 2010 we launched the power device/module packaging project. Typical existing advanced automotive power modules and their packaging technologies have been examined. The packaging structures, materials, and technologies and their effects on power module performance, reliability, and cost have been analyzed. Based upon these benchmarked results and interpretations, we proposed an innovative power module structure with high power conversion efficiency and cost effectiveness. To realize successful high operational temperatures, some new processing technologies have been explored in-house. In addition, a complete Power Electronics Packaging Laboratory has been designed and constructed. It will become a prestigious platform to enhance the projects within the VTP program. All these accomplishments provide a solid foundation for next year's objectives.

Publications

1. Zhenxian Liang, *ORNL Advanced Power Electronics Packaging Laboratory*, presentation at DOE FreedomCar EETT conference, Aug. 26, 2010.
2. Andy Wereszczak, *Packaging Characterization: Power Module Tear-Down*, presentation at DOE FreedomCar EETT conference, May 27, 2010.

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2. Yasuyuki Sakai, Hiroshi Ishiyama, and Takaji Kikuchi, "Power Control Unit for High Power Hybrid System," in *Proceedings of the 2007 SAE International Conference*, p. 2007-01-0271.

3. Seiji Momota, et al., "Plated chip for hybrid vehicles," *Fuji Electric Review*, Vol. 54, No. 2, 2008, p. 49.
4. Natsuki Nozawa, et al., "Development of Power Control Unit for Compact-Class Vehicle," in *Proceedings of the 2009 SAE International Conference,* p. 2009-01-1310.
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6. T. Ueda, et al.; "Simple, compact, robust and high-performance power module T-PM (transfer-molded power module)," The 22nd IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD), 2010, pp. 47–50;
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Patents

2. Invention Disclosure: Zhenxian Liang, Laura Marlino, Fred Wang, and Puqi Ning, *Power Module Packaging with Double Sided Planar Interconnection and H/E*, ID NUMBER: 201002429 DOE-S Number: S-115,481.

3. Electric Machinery Research and Technology Development

3.1 A New Class of Switched Reluctance Motors Without Permanent Magnets

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Objectives

- Overall Objectives
  - — Develop, design, build, and test an unconventional traction drive that
    - has no permanent magnet material,
    - has lower torque ripple and acoustic noise than that of a conventional switched reluctance motor (SRM), and
    - maintains the low cost, simplicity, and power density of the conventional SRM.
  - — Obtain operational characteristics for finalized design and compare with targets:
    - power density: 5 kW/L (2015 DOE target),
    - specific power: 1.3 kW/kg (2015 DOE target), and
    - motor cost between $7/kW and $4.7/kW (2015 and 2020 targets, respectively).
- FY 2010 Objectives
  - — Develop and refine control scheme.
  - — Perform dynamic simulations.
  - — Conduct structural and acoustic modeling.
  - — Arrive at optimized design.

Approach

- Develop/refine control algorithms.
  - — Develop software solutions needed to operate novel machine.
  - — Investigate potential to introduce novel control techniques.
- Conduct electromagnetic, thermal, and structural/acoustic noise modeling.
  - — Perform various types of finite element analysis (FEA) studies to critique overall design.
  - — Perform acoustic modeling throughout vibration modes.
- Make necessary refinements.
  - — Address any structural, thermal, or vibration issues.
  - — Conduct electromagnetic FEA studies to confirm that mechanical implementations do not compromise performance significantly.
- Fully simulate finalized ORNL SRM design in dynamic simulations.
  - — Determine torque and power versus speed characteristics.
  - — Obtain accurate values for power density and specific power.

- Prepare a summary report to be incorporated into the annual VTP report that describes the
  - control algorithm;
  - FEA results, including torque and power capabilities and operational characteristics; and
  - finalized SRM design and converter architecture.

Major Accomplishments

- Verified through simulations that the design meets 2015 performance targets with less than 5% torque ripple.
- Developed custom software to accomplish various tasks.
  - Two universal dynamic simulators.
    - Parametric: efficient means to optimize control and design parameters.
    - FEA: capable of conducting dynamic electromagnetic and structural simulations.
  - Automated FEA-based geometric optimization.
  - Complex multivariable, multiobjective optimization of control waveforms as a function of speed and torque.
    - Near-zero torque ripple achieved for low and moderate torque levels (up to 150 Nm).
- Designed entire assembly, prepared drawings for fabrication, received all parts, and began assembling model verification prototype.
  - Verified mechanical structural integrity and performed qualitative acoustic analyses.
- Received positive feedback and significant interest from the Electrical and Electronics Technical Team and industry.

Future Direction

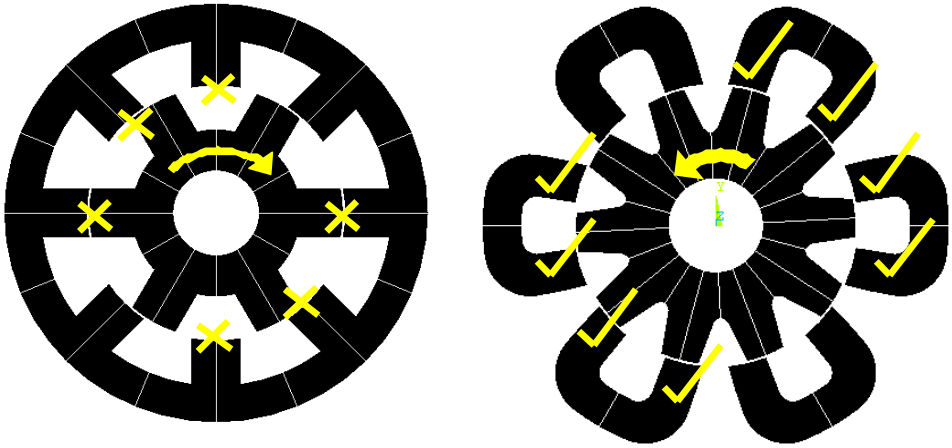
- Finish assembling model verification motor.
- Develop and apply means to obtain characteristics before and during testing.
  - Establish means to comprehensively obtain torque and flux linkage as a function of current and position for use in control algorithm.
  - Provide method to accurately measure torque ripple.
  - Assess impact of noise/vibration damping materials.
- Develop and prepare drive/controller hardware and software.
  - Implement control algorithm on digital signal processing or real-time system.
  - Choose inverter and build corresponding controller interface.
- Design, fabricate, and build final prototype.
  - Incorporate changes into design as determined from first construction and basic testing.
- Conduct comprehensive motor testing in dynamometer test cell.
  - Determine performance capabilities and efficiency characteristics throughout operation range for various operation modes.

Technical Discussion

Because of the high and unpredictable cost and availability of rare earth permanent magnets (PMs), which are used in most hybrid vehicle applications today, many automotive manufacturers have a common interest in the use of electric machines which do not use these PM materials. Although PM motors are not easily surpassed with respect to efficiency and power density, other competitive motor technologies exist which can have lower cost per power rating ($/kW). Of the alternative motor technologies, the SRM offers the simplest rotor configuration, which is advantageous in terms of material cost, manufacturing cost, speed capability, and reliability. The highly nonlinear behavior and unusual control methods associated with the SRM require the use of sophisticated and computationally intensive software programs to fully optimize its design and operation. Therefore, the SRM is a relatively young motor technology, in terms of research and development, as opposed to other technologies such as the induction motor. Two primary drawbacks of the SRM are the level of torque ripple and the acoustic noise inherently

associated with the SRM's doubly salient stator and rotor geometry. The intent of this project is to apply novel design techniques that significantly reduce torque ripple and acoustic noise while maintaining the intrinsic benefits of the SRM.

Existing torque ripple and acoustic noise reduction techniques typically incur significant compromises of things such as peak torque, torque/power density, material/manufacturing costs, and/or design complexity. A conventional SRM with eight stator teeth and six rotor teeth is shown in Fig. 1. If the rotor is assumed to be rotating clockwise, the two stator teeth without a superimposed yellow 'X' are the only stator teeth that would have excited windings if a conventional control scheme were used. That is, only two (25%) of the eight stator teeth are active during this instant. As the rotor position continues to increase in the clockwise direction, coils of two additional stator teeth are excited, and thus 50% of the stator teeth are active at that instant. However, this condition is maintained only for a short duration, and only 25% of the stator teeth are active beyond this short duration, giving a low average of active stator teeth.



(a) **(b)**

Fig. 1. Active stator teeth of a conventional SRM (a) and unconventional SRM (b).

After observing the low amount of active air gap area within the conventional SRM, it seemed that novel concepts could be used to increase the average number of active stator teeth that are producing productive torque in order to more readily distribute the torque production and thereby reduce torque ripple. Because the fundamental means in which torque is produced in an SRM relies on the magnetic saliency of the stator and rotor, it can be difficult to increase the number of active stator teeth without compromising the reluctance ratio between aligned and unaligned rotor positions. This is a result of introducing stator and/or rotor teeth within a closer proximity of each other, thereby promoting detrimental flux flow through undesired paths, which potentially decreases the overall torque capability of the machine. Therefore, the proposed general approach uses separate steel pieces and/or laminations to carry out the tasks mentioned above while seeking to minimize counterproductive flux flow by means of magnetic path isolation. Because the permeability of steel approaches that of air as magnetic saturation increases in the steel, it is not possible to have completely isolated magnetic paths in this type of application, particularly since the SRM often operates in the saturation region. Therefore, these types of hardware approaches must be incorporated carefully in such a way that the natural operation and control of the motor inhibits the detrimental tendencies of leakage and undesired flux paths.

In FY 2009, a wide variety of designs which use this technique were developed and analyzed for feasibility. Based on comparisons of estimated performance, size, cost, and manufacturability, the most

feasible geometry was chosen to be the focus of FY 2010 development efforts. As shown on the right in Fig. 1, 8 of 12 stator teeth are typically active at the indicated rotor position for counterclockwise motoring operation. As the rotor continues to rotate, only 4 of 12 stator teeth are active for a brief period of time and then 8 of 12 stator teeth are active again. Therefore, on average, at least 50% of the stator teeth are active in this unconventional SRM versus roughly 33% in a conventional SRM. While many more characteristics should be considered in making a direct comparison, this quick observation reveals the potential of the design to facilitate greater overlap of torque production among the phases compared with a conventional SRM.

Dynamic Simulators

To have the capability to fully assess the overall impact of the variation of a range of design parameters, two separate universal dynamic simulators were developed. The simulators are universal in the sense that they can simulate various motor designs, even other types of motors, with slight modification to the simulator. One of the simulators carries out the dynamic simulation and corresponding computations within FEA software by means of accessing the FEA solution database for each iteration and applying the appropriate constraints, constants, and relationships for the transient solution. This simulator is well suited for integration with other types of analyses such as integrated structural and thermal FEA. The other simulator is similar in nature, but entails a more parametric oriented approach to the transient solution and relies on parametric data from static FEA solutions. Extensive efforts were made to ensure that the impacts of saturation, mutual coupling, and other interactions between phases were fully realized. It is common for designers to neglect these phenomena, but the acknowledgement of these aspects is particularly important for this unconventional design approach. Both simulators have the capability to work in various modes such as current, torque, or speed regulated operation so that the simulation is conducted as if the design were in actual operation in a vehicle. Figure 2 shows a graphical user interface (GUI) that was developed to provide an effective way to operate the dynamic simulators and generate and edit waveforms which are supplied and returned from the simulator code.

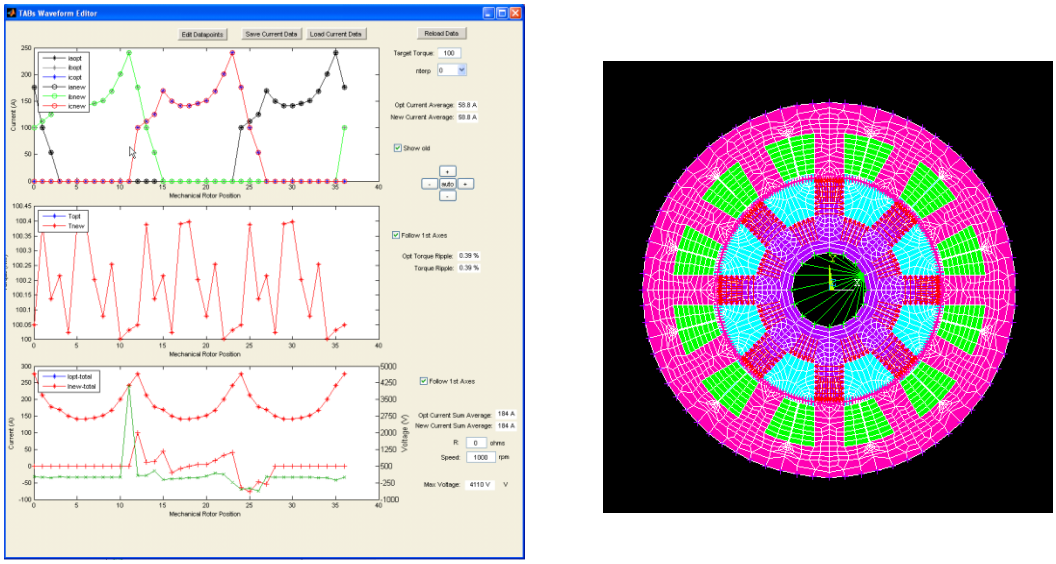


Fig. 2. GUI developed to operate dynamic simulators.

Control Algorithm Development

The parametric simulator is particularly useful for optimizing control conditions such as maximum torque per amp, minimum torque ripple, and maximum efficiency. A considerable amount of effort was devoted to the development of control optimization code for operation with near-zero torque ripple. Since torque

is a function of three currents and position, the currents at each position can be chosen to meet the desired torque reference, provided that current and voltage constraints are not violated. Therefore, this approach requires dynamic modeling to ensure that the required voltage does not exceed the amount available from the dc link. The resulting problem is nonlinear multivariable, multiobjective optimization with nonlinear constraints. Attempts were made to use optimization algorithms including various genetic and neural networking techniques, but computational times were tremendous and there was difficulty in obtaining globally optimal solutions, as local solutions were often presented, despite the use of a global algorithm. Therefore, an algorithm termed the "brute-force" method was developed, based on the unconventional manner in which the problem is approached using this method. The method involves the automated generation of an initial solution for the desired conditions followed by development of a series of solutions that fall within the given constraints. At this point, the brute-force method finds the optimal solution and verifies that it is a global solution, else another iteration is commenced. It is estimated that about 10,000 lines of code were written to carry out this task, in which recursive functionality is used to explore solution regions. The overall result is a collection of reference waveforms for points throughout the entire operation region.

Solutions obtained from the brute-force method were analyzed with the parametric dynamic simulator, with the results for less than 5% torque ripple conditions indicated by the blue trace in Fig. 3. Torque ripple can be defined in various ways, and in this case, it is based on the quadratic mean of the ripple divided by the average torque multiplied by 100. This method was used as opposed to using single values such as the maximum and minimum torque, which do not fully incorporate all aspects of the torque waveform. For example, a torque spike with very short duration could be present in the torque waveform and the latter torque ripple calculation would be greatly affected although the inertia of the system would most likely render the spike to be minimally consequential. A torque level of about 170 Newton meters (Nm) is achievable at low speeds with a torque ripple level of 5%. At 4,000 rpm, the machine is capable of producing 125 Nm, which is a power level of 52.4 kW, with a torque ripple of only 5%. Calculations which include copper and iron losses indicate that the efficiency of the motor under these conditions is about 94.5%. As speed increases, the power capability decreases if the torque ripple is limited to 5%. But at higher speeds, it may be possible to alleviate the torque ripple constraints based on the increased momentum associated with these speeds.

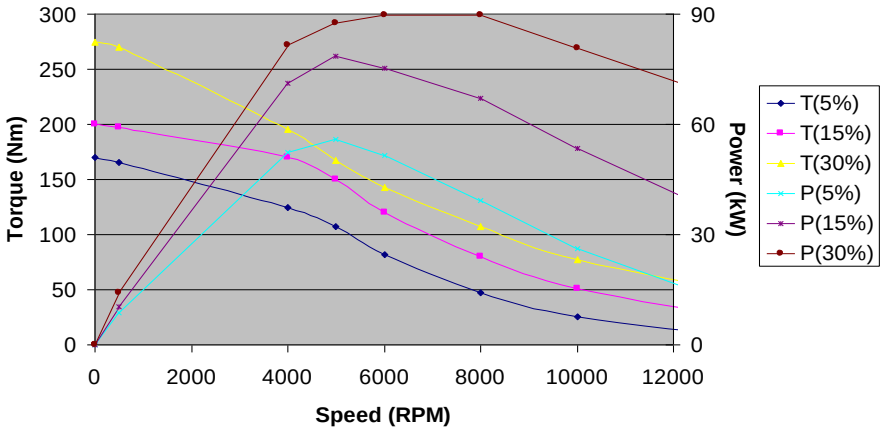


Fig. 3. Torque and power versus speed.

Continuous conduction control can greatly increase the output power of an SRM at moderate and high rotor speeds as a higher amount of current is applied during the torque production region (for the motoring operation mode). This is achieved by not requiring the current in each stator tooth to reach zero during each electrical cycle. Because current is not zero when the rotor rotates beyond the alignment

position, negative torque is applied to the shaft, and thus this control mode does not operate with utmost efficiency, but it can greatly increase the power capability of the machine. This is particularly relevant to vehicle propulsion applications, wherein the average required power is relatively low for normal driving conditions and only short durations of high power demand are required for situations such as passing other vehicles or merging with high-speed traffic.

The additional traces shown in Fig. 3 represent the torque and power capabilities of the machine with torque ripple percentages that are greater than 5%. Simulations indicate that the machine can produce about 75 kW at 8,000 rpm with a torque ripple of 20% and more than 90 kW at 8,000 rpm with a torque ripple of 30%. Simulations also show that the machine is capable of operating beyond 15,000 rpm. The size of the machine used in these simulations matches that of the second generation Prius, with roughly a 10 in. stator outer diameter and a 3.3 in. stack length. This particular design is well suited for an application similar to that of the primary motor of the Camry hybrid electric vehicle (HEV), where a gear reducer is used to increase the torque capability while the high speed operation results in improved power density. These results indicate that this design approach could potentially offer a competitive alternative to PM machines in HEVs.

Structural, Modal, and Acoustic Assessments

Mechanical analyses were conducted to perform design optimization and validation in terms of structural integrity and minimal acoustic signature. Force vector results from electromagnetic FEA studies were used to establish proper loading conditions and boundary conditions for these mechanical FEA studies. As peak loading conditions were applied, stress analyses were conducted on the components within the assembly, shown in Fig. 4. As structural improvements were incorporated into the design in response to these studies, the impacts upon the electromagnetic characteristics were assessed in separate analyses, as necessary.

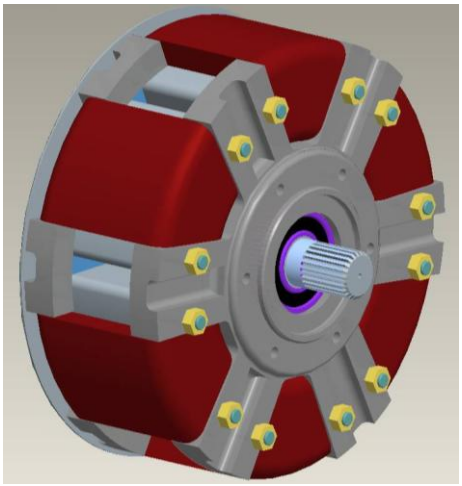


Fig. 4. Phase 1 motor assembly.

Initial studies indicated that a support pin for the stator laminations contained a stress concentration of about 100,000 psi (Fig. 5). As this stress is excessive, a method was integrated into the design which more readily distributes the stress along the stack of laminations and also allows the use of more substantial support hardware, thereby rendering it a stator support structure with maximum stress concentrations which are well below maximum yield strength.

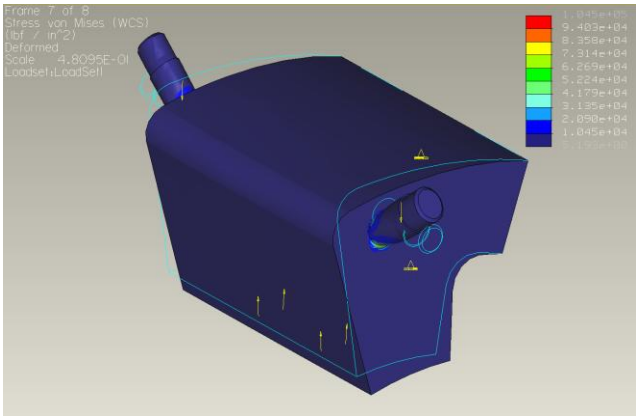


Fig. 5. Support pin stress analysis.

It is important to assess the displacement of the stator lamination stack under maximum load to ensure that it does not deflect and cause catastrophic failure due to interference with the rotor lamination stack. As shown in Fig. 6, the maximum displacement is located in the center of the lamination stack, where the model indicates a maximum deflection 0.0004 in. With an air gap of 0.03 in., the deflection extends about 1.3% into the air gap.

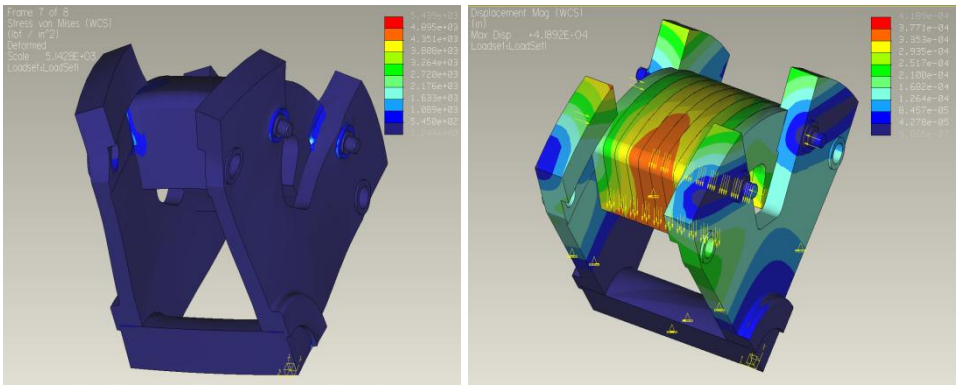


Fig. 6. Displacement analysis of support structure and stator lamination stack.

A separate stress analysis with peak loading conditions was performed on the crossbeam, shown in Fig. 7, which provides lateral support to the structure. Simulation results indicate a maximum stress of about 27,000 psi located in sharp crevices of the component. While these stress concentrations are not extremely high, they can be minimized with an appropriate radius in these locations.

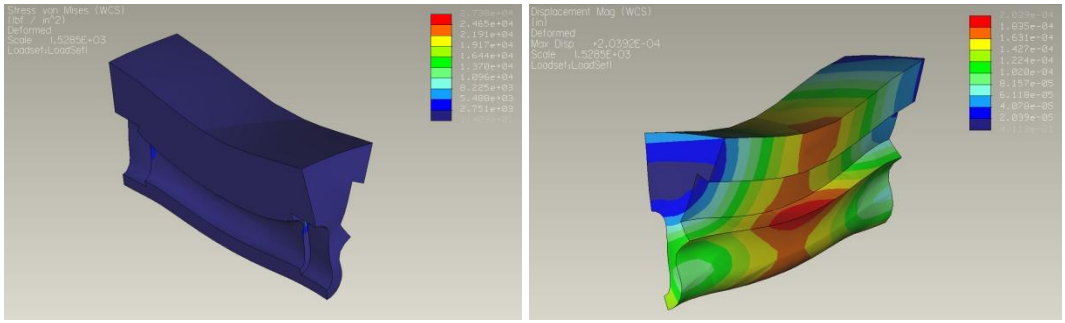


Fig. 7. Crossbeam stress analysis.

Although the rotor shown in Fig. 8 is of the conventional type, stress analysis was performed to assess the impact of centrifugal forces, which are a primary influence in the speed rating of the machine. A particular area of concern was the locating tab on the inner diameter of the lamination, where there is a stress concentration in the corners of the tab. This model was simulated at 20,000 rpm, and the stresses are well below the material yield strength with a factor of safety of about 1.7.

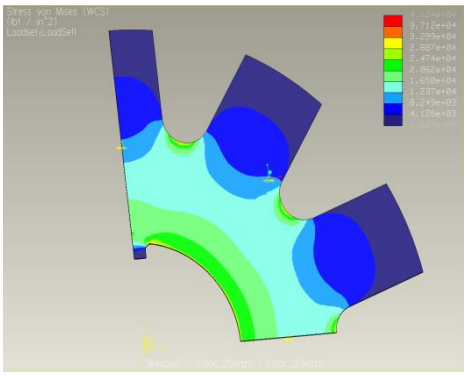


Fig. 8. Stress analysis of rotor lamination stack.

Various modal and qualitative acoustic analyses were conducted after the primary structural optimization efforts were concluded. While various modes exist, focus was placed on modes that correspond with frequencies associated with the operation of the design within the operating speed range. This includes forces which are directly related to the speed of rotation as well as other forces that are indirectly related to the speed of rotation which typically have higher excitation frequencies. The first mode shape of interest, shown in Fig. 9, occurs at 730 Hz. Deflections associated with this mode are essentially axial, and the structure would have good coupling to surrounding air like a speaker cone. However, driving forces for this mode shape should be minimal. For example, this mode shape may be excited if the rotor lamination stack had a significant misalignment with the stator lamination stack.

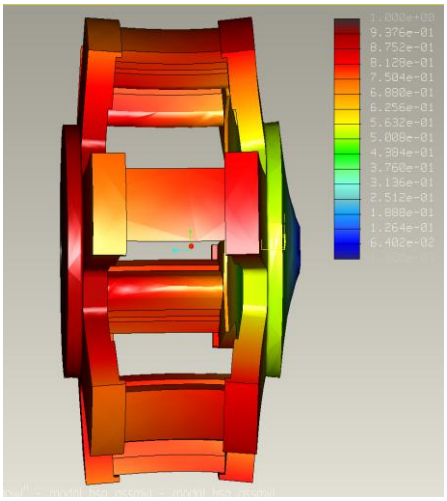


Fig. 9. Mode shape at 730 Hz.

Another mode of interest occurs at 1,250 Hz. As shown in Fig. 10, the deformation is essentially an axial mode with a twisting shape in the Y-Z plane. This mode would be highly attenuated by using a damping compound between the stator pole pieces and an outer shell which encompasses the outer perimeter of the crossbeams. The outer shell (not included in this simulation) would also add stiffness to reduce the amplitude of this mode shape.

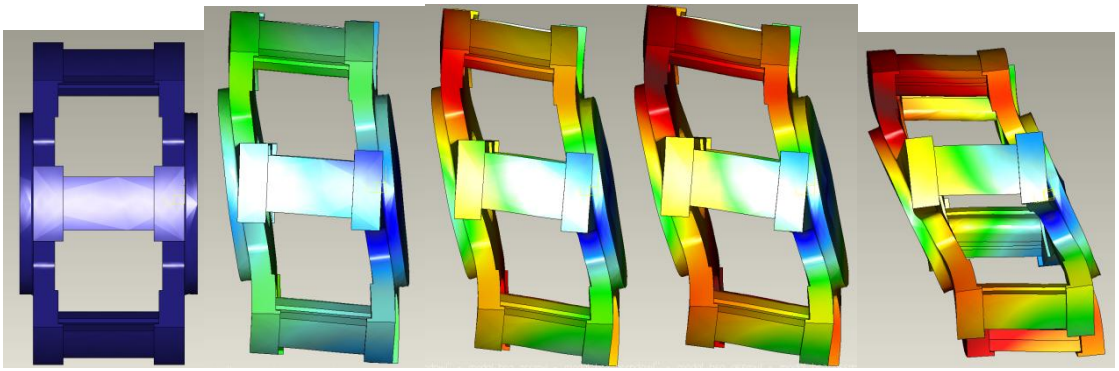


Fig. 10. Mode shapes at 1,250 Hz.

The next mode of interest occurs at 1,600 Hz, and consists of twisting deformations in the X-Y plane, as shown in Fig. 11. This mode would be significantly reduced by a cylindrical sleeve that is intended to be placed around the outer perimeter of the assembly. Damping material between the stator pole pieces and the outer sleeve will also mitigate these modal tendencies. Ultimately, this is a high modal frequency and it is not likely that there will be substantial driving forces within the range of operation of the machine.

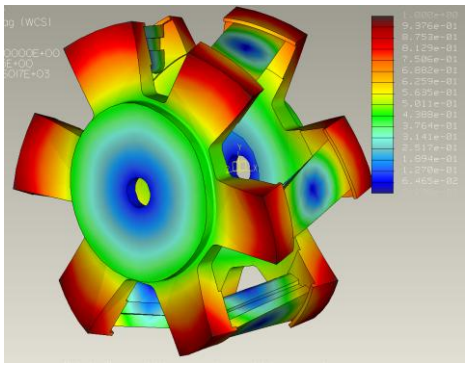


Fig. 11. Mode shape at 1,600 Hz.

Many other modal shapes exist and have been analyzed, and it was determined that there were no modes which caused significant concern in terms of structural integrity and acoustic signature. These studies are particularly useful in the determination of key areas to focus upon during the fabrication and assembly process. More specifically, a better understanding

has been established for the desired characteristics of the damping compounds that will be used throughout the assembly.

Thermal Analyses

A thermal model was developed using the layout shown in Fig. 12, and heat loads used in the analyses were obtained from modeled resistive heat as well as losses associated with hysteresis and eddy current effects. The model consists of the stator piece, which is made of electrical steel, copper windings, an insulation/damping layer, and the outermost cylindrical sleeve. The outermost sleeve provides structural support and is also used as a heat exchanger in the simulations, with heat transfer characteristics comparable to that of a typical water-ethylene glycol heat exchanger with a coolant temperature of 65°C. At low speeds most of the heat is generated by resistive losses in the stator winding, and at high speeds, most of the heat is generated by hysteresis and eddy current losses. Overall, the maximum amount of heat, by far, is generated at low speed, high-current operating points.

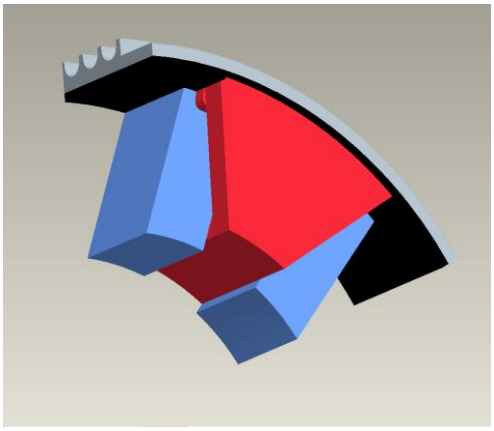


Fig. 12. Model used for thermal analysis.

While a conventional type of heat exchanger is used, this design has the distinct and substantial advantage of having the primary heat source (stator windings) located adjacent to the cooling apparatus. Additionally, the thermal conductivity of copper is at least 10 times that of the steel used in the laminations. Conventional motors of all types typically have stator windings enclosed by the steel laminations, and thus all heat must travel through the back iron of the stator laminations. Nonetheless, the current design approach requires the use of a compound between the stator winding and the outer sleeve for electrical isolation and the longevity of the winding. This compound is the primary inhibitor of heat transfer from the stator assembly to the heat exchanger. Studies were performed to assess the impact of the thickness of the compound. Figure 13 shows the results from two of the many scenarios that were investigated. For the maximum power condition with 5% torque ripple (52 kW), results indicate that a decrease in the thickness of the insulation compound from 0.06 in. to 0.03 in. has very little impact. Under these conditions, the steady state temperature for the 0.03 in. thickness is estimated to be 113°C, well below the temperature rating of the copper windings.

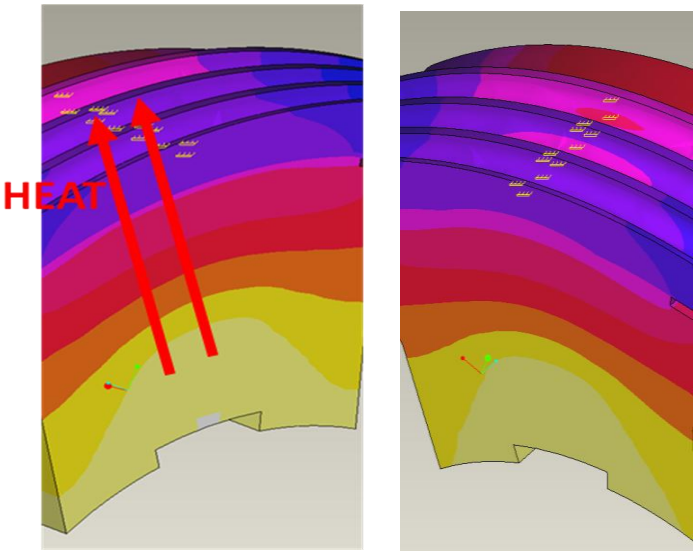


Fig. 13. Thermal gradient for electrical insulation compound thickness of 0.06 in. (left) and 0.03 in. (right).

First Phase Prototype

Although the final prototype is scheduled for fabrication and assembly in FY 2011, it became evident that there would be many benefits from building a preliminary

prototype. This first phase prototype will yield valuable information in various areas of the design and operation of the ORNL motor. From a modeling standpoint, empirical data can be used to verify (and adjust, if necessary) electromagnetic, structural, and thermal simulations. Additionally, quantitative empirical acoustic analyses will provide the opportunity to investigate the impact of various damping compounds. Various components in the first phase prototype, shown in Fig. 14, can be removed and replaced so that the effect of various types of compounds can be assessed. From a controls standpoint, it is important to have accurate motor parameters, which vary with rotor position, three currents, and temperature. ORNL will develop a means to measure these parameters and, because of the overall advantages to the program, will initiate this effort immediately in FY 2011 as opposed to waiting on the fabrication and assembly of the final prototype. Similarly, we will also begin integration and testing of the control algorithm and motor drive in the early part of FY 2011 without the final prototype. Therefore, the time constraint of completion for the final prototype assembly has been alleviated greatly and more effort can be placed on incorporating design improvements as observed throughout the fabrication, assembly, and testing of the first phase prototype.

Fig. 14. First phase prototype.

Conclusion

- Simulations indicate that the design meets 2015 performance targets with less than 5% torque ripple for a motor of the same size as that of the 2004 Prius.
  - Capable of 75 kW with only 20% torque ripple.
  - Capable of 90 kW with only 30% torque ripple.
  - Low cost due to absence of PM material.
- Automated control technique developed for near-zero torque ripple.
- First phase prototype designed, fabricated, and partially assembled.
- Improved upon and maintained characteristics of conventional SRM technology.
  - Significant reduction of torque ripple and acoustic noise.
  - Matches or surpasses performance of conventional SRM.
  - Robust with low manufacturing and fabrication costs.
  - Lower core losses due to localized flux paths.
  - Improved cooling due to unconventional winding technique.

3.2 Novel Flux Coupling Machine Without Permanent Magnets

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Objectives

- Finalize the design for a Novel Flux Coupling Machine without Permanent Magnets (PMs) and complete both electromagnetic and mechanical finite element analyses (FEAs).
- Complete engineering fabrication drawings.
- Analyze means of using field control to achieve a higher power factor, increasing both efficiency and torque capabilities.
- Begin fabrication of the prototype machine.

Approach

- Perform electromagnetic FEA simulations and compare the performance results to current industry standard PM machines.
- Add a field coil to provide an adjustable flux.
- Develop a novel flux path to function like a PM machine without the use of brushes.
- Use a hybrid cooling system with both internal oil channels and external water jackets in the motor housing.
- Perform field control simulations to ascertain the possibilities of achieving a higher power factor, increasing both efficiency and torque.
- Produce engineering fabrication drawings and begin prototype machine fabrication.

Major Accomplishments

- Demonstrated through finite element simulations on the prototype design that the PMs could be eliminated by using the novel stationary, brushless excitation coils, thus contributing to resolution of cost, temperature, performance, and speed issues typically associated with PMs.
- Analyzed 34 design iterations.
- Verified through simulations overall feasibility of the novel machine to meet DOE 2020 motor weight and volume targets.
- Verified significant cost reductions over PM machines can be realized by the novel machine.
- Integrated solid soft magnetic components for the rotor axial flux paths into the design.
- Achieved a design capable of operating at 14,000 rpm.
- Developed a MATLAB analytical program to provide performance versus speed curves under the voltage and current constraints.

Future Direction

- Complete prototype fabrication and testing in FY 2011.
- Compare the simulated results to the test results and develop a path forward for improvements.
- Bring the proven technology to the market.

Technical Discussion

Figure 1 shows a cutaway view of the prototype motor. No PMs are used in the motor; consequently, the permissible temperature of the motor is not restricted by their demagnetization.

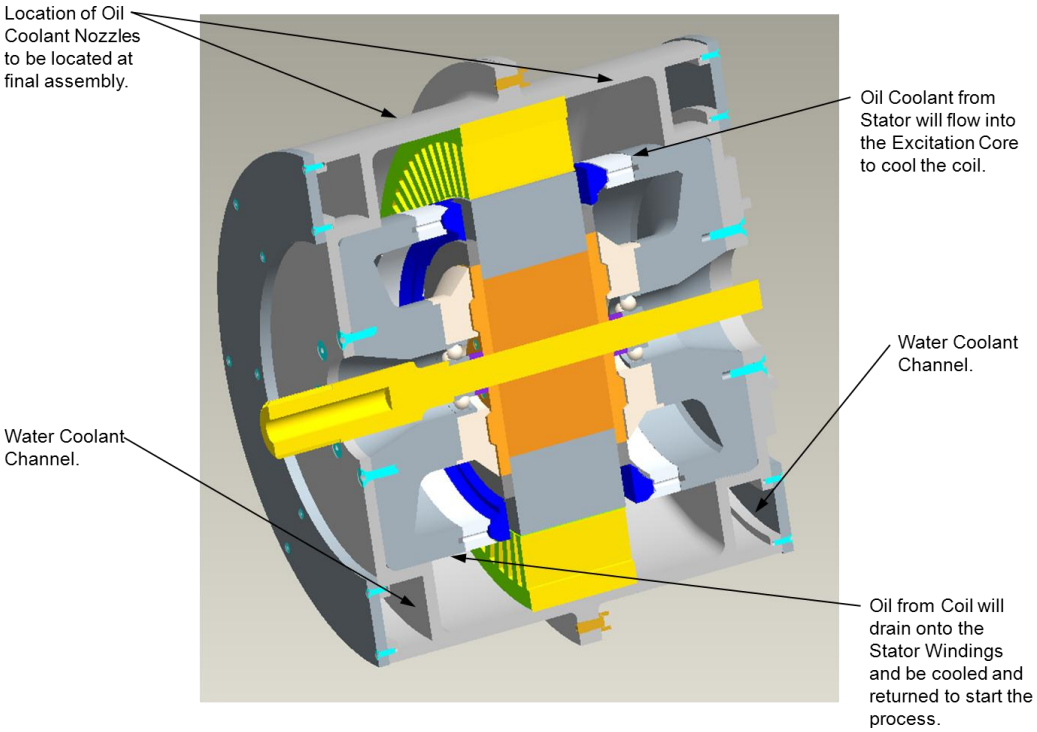

Fig. 1. Motor assembly cutaway view.

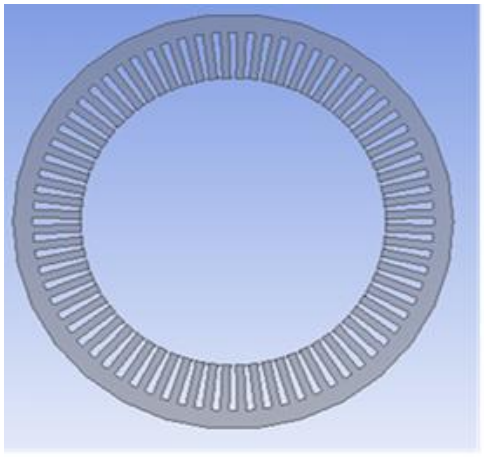

Fig. 2. Stator punching of prototype motor.

The stator punching of the flux coupling motor can be made for either a conventional distributed winding, such as the prototype punching shown in Fig. 2, or for a fractional-slot concentric winding type. The flow of flux is the same as the flux in a conventional two-dimensional stator core (i.e., no magnetic flux is designed to flow through the stator core axially).

The rotor direct current (dc) field flux is produced by two stationary excitation cores that transfer dc flux through the axial air gaps at each side of the rotor. Because the flux is dc, no eddy current is produced in the solid iron.

The inner and outer rings of the excitation core have opposite magnetic polarities. The inner ring of the excitation core carries one polarity of flux which goes through the axial gap to the rotor hub and subsequently distributes radial flux

to the laminated rotor poles as shown in Figs. 3 and 4. This flux then goes into the stator core and returns to the rotor wedges through the radial gap in an opposite polarity. This opposite polarity flux then flows axially to the rotor distributing rings that are only contacting the ends of the rotor wedges (shown in Fig. 5). The other side of a distributing ring is a complete ring without cutoffs. The dc excitation flux then returns to the excitation core to complete its magnetic path.

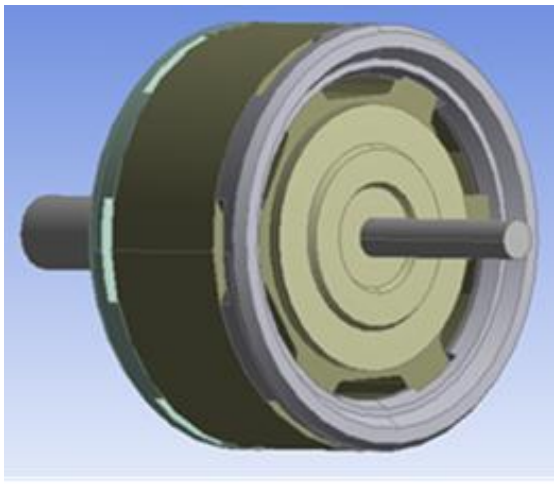

Fig. 3. Rotor of prototype motor.

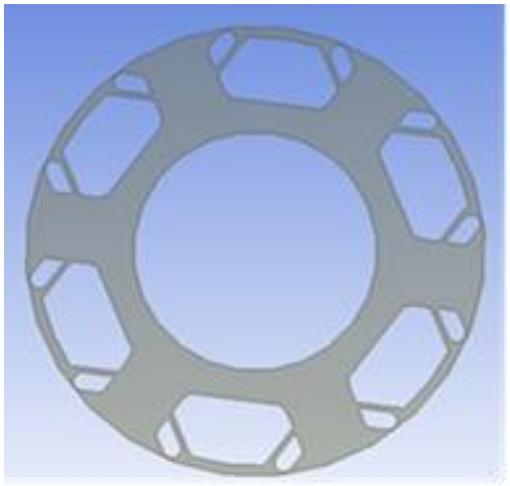

Fig. 4. Rotor punching.

Because the rotor distributing ring is not very thick in its axial direction, the saliency of the distributing ring may transfer to the smooth side of the ring and may produce core losses in the stationary outer ring of the excitation core. As the flux is dc, the local fluctuation of the space harmonics due to the saliency can be mitigated by the use of an equalizer ring made of a wrapped lamination. This will equalize the flux before going into the solid iron excitation core.

The major axial dc flux goes through the rotor solid hub and the rotor solid iron wedges that are located inside the cavities of the rotor punching and shown in Fig. 4. This solid iron path reduces the reluctance associated with the axial path of the laminated core.

Because the rotor solid iron wedges are shielded inside the rotor punching cavities, the high frequency slot harmonic flux is bypassed through the laminations on top of the wedges. This arrangement weakens the space harmonic flux that can go to the wedges. This core loss reduction effect will be measured and studied further FY 2011.

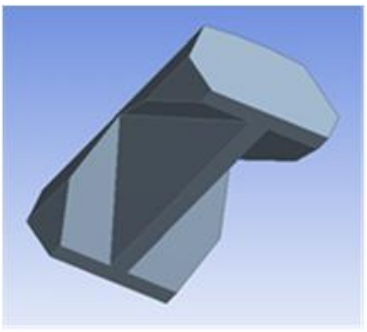

Fig. 5. Rotor solid iron wedge.

The overall motor performance curves for a motor with a wide range of magnetic saturation affected by the change of load and excitation should be calculated through the finite element flux linkages for each phase winding and at each operating point. Unfortunately, this would take excessive computation time and the available research time for this project was very limited. To address this, the saturated full load direct axis and quadrature axis inductances and the no-load flux linkage of the stator winding were computed and used to give a simplified overall estimation of the prototype motor's performance.

Figure 6 shows the simplified performance curves for the prototype motor. The corresponding parameters used in the analysis are peak phase voltage = 375 V, peak phase current = 233 A, stator phase winding flux linkage = 0.0875 Wb, excitation current = 8 A, direct axis inductance Ld = 0.289 H, and quadrature

axis inductance Lq = 0.386 H. The performance versus speed curves include peak phase voltage, power factor, direct axis phase current component, quadrature axis phase current component, peak phase current, motor torque, motor power, load angle delta, and current angle beta.

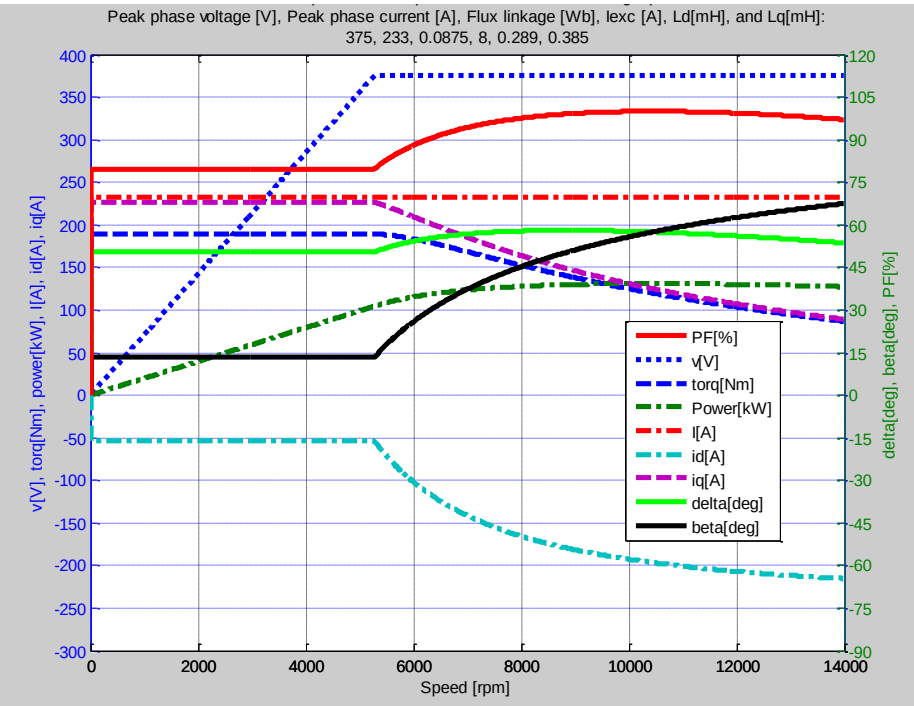

Fig. 6. Simplified motor performance versus speed curves.

As indicated in Fig. 6, the power factor at the highest speed region dips down. It can be improved by reducing the excitation current, resulting in weaker flux linkage (from 0.0875 Wb to 0.0788 Wb) as shown in Fig. 7.

Figure 8 shows the stator winding diagram for the prototype. The winding is capable of two dc bus voltages at either 600 V or 300 V. This is achieved by changing the lead connections. The magnet wire temperature rating was increased from the conventional class H (180°C) to class K (200°C) to take advantage of the elimination of the PM temperature restriction. The winding fill factor is 0.795, compared with 0.762 for the 2007 Camry motor. An optional stator winding would be to reduce the number of wires from 18 to 17, thus reducing the fill factor to a value of 0.751.

The 12-pole stator winding resistance is 0.052 Ohms per phase at 21°C, compared with 0.0354 Ohms for the 8-pole Camry motor. The stator copper loss at a root mean square current of 165 A is 4.2 kW at 21°C and 7.2 kW at 200°C. This is under the peak power condition with an 18 s operation time. The core loss and the efficiency map will be studied in detail in FY 2011 following the prototype motor build and test.

The excitation coil of the prototype motor has 1,000 turns of 19 AWG magnet wire. The resistance value is 10.6 Ohms at 20°C per coil and 18.1 Ohms at 200°C. During normal operation the excitation current is only a few amperes. The total 200°C excitation coil copper loss with 5 A excitation is 0.9 kW.

The torque quality of the prototype motor was evaluated through the torque value at each rotor angular position with the corresponding three-phase stator currents. The simulated results indicate good torque

quality as shown in Fig. 9. For comparison purposes, the torque quality is extremely poor with a 12-pole, 36-slot design of 1 slot per pole per phase.

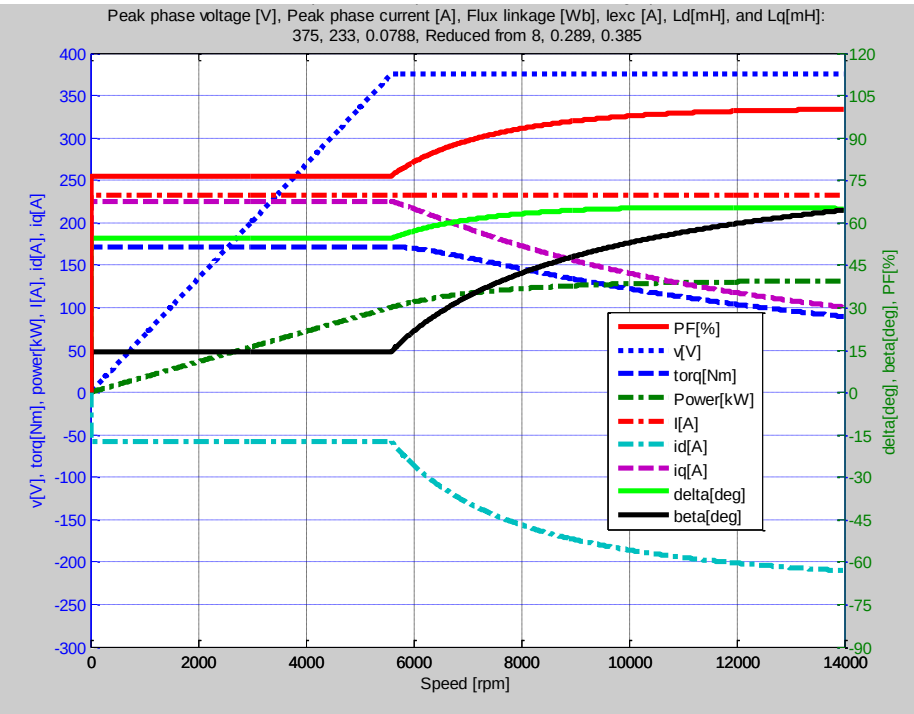

Fig. 7. Adjustable field can improve power factor.

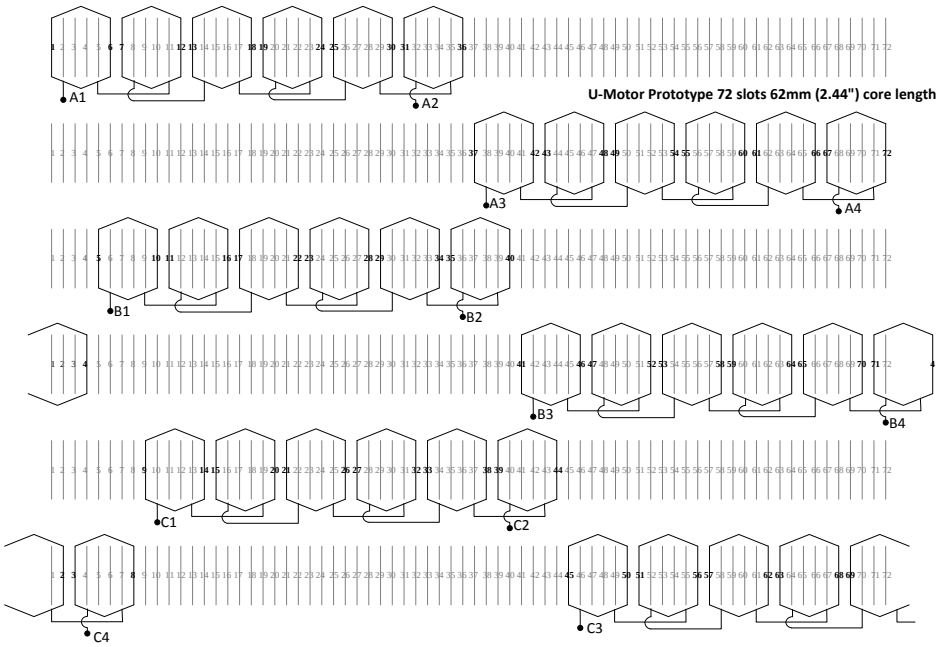

Fig. 8. Stator winding diagram.

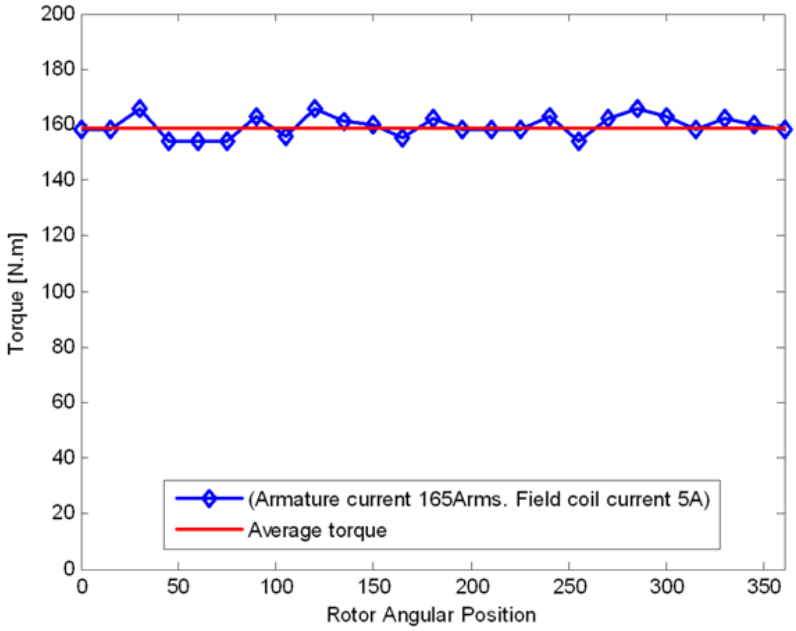

Fig. 9. Torque quality.

To achieve a 14,000 rpm rotor speed various design options were evaluated, many of which ultimately could not meet the stress and displacement requirements. The breakthrough came from shifting the focus from the rotor lamination alone to include the assembly of the flux distributing plate and the rotor hub end plate. ASTM A867, Alloy 2, a 2.50% silicon steel, was selected for the flux distributing plates, the rotor hub, and its end plates. This soft magnetic steel has sufficiently high mechanical strength (85 kSi tensile strength, mill annealed, and 80 kSi annealed for magnetic property) and magnetic properties equivalent to those of M-19 silicon steel.

The finite element simulation for the rotor stress at 14,000 rpm is shown in Fig. 10. The maximum rotor assembly stress at 14,000 rpm is 65,122 psi, located at the assembly of the flux distributing plate and the rotor-hub end plate.

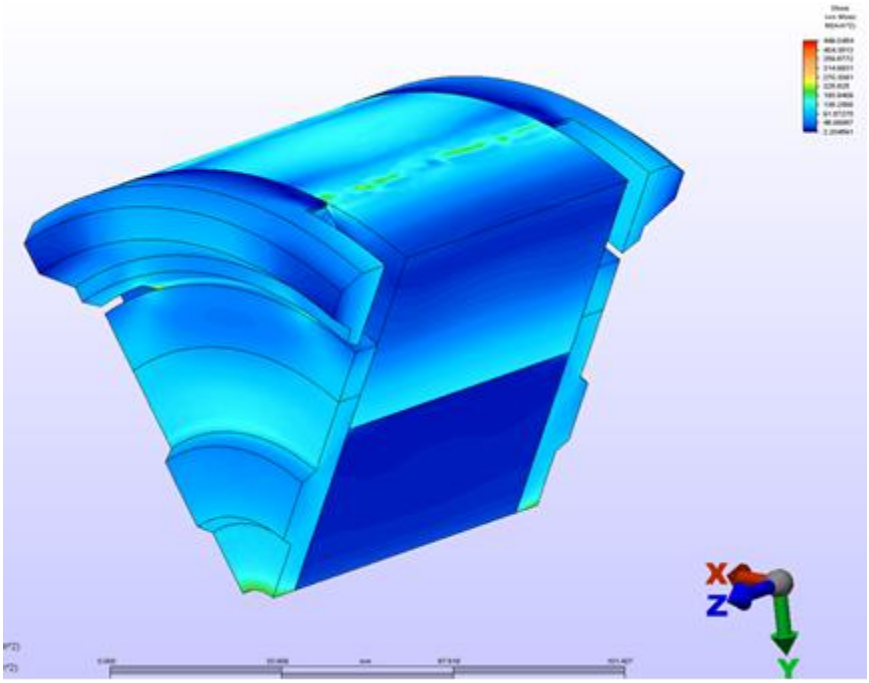

Fig. 10. Maximum Rotor Assembly Stress at 14,000 rpm = 65,122 psi.

The finite element simulation for the rotor displacement at 14,000 rpm is shown in Fig. 11. The maximum displacement of 0.002 in. is located at the rotor pole center of the rotor lamination stack. This displacement is acceptable with respect to the 0.029 in. per side of the radial air gap.

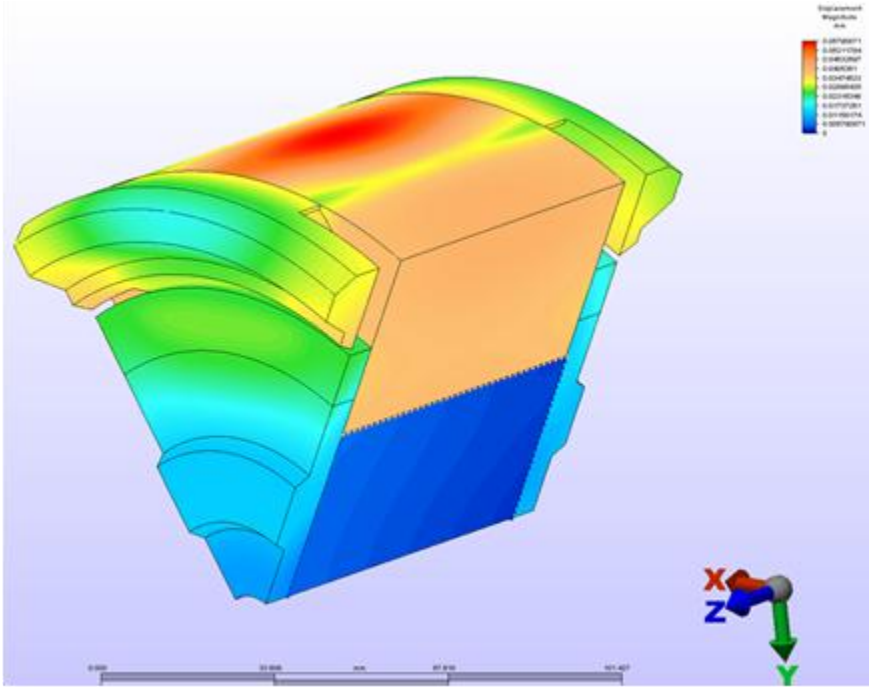

Fig. 11. Maximum rotor assembly displacement at 14,000 rpm = 0.002 in.

Table 1 shows comparisons among the novel flux coupling motor, the 2007 Camry motor, and the DOE FY 2020 targets.

Table 1. Comparisons Among Novel Flux Coupling Motor, Camry, and DOE 2020 Targets

Characteristic	Camry	Novel flux coupling motor	DOE 2020 Targets
Maximum power output (kW)	70 (tested)	115 (computed)	55
Weight (kg)	36.3	55.7	
Volume (L)	13.9	13.6[a]	
Specific power (kW/kg)	**1.9**	**2.1**	**1.6**
Power density (kW/L)	**5.0**	**8.5**	**5.7**
Power factor	0.61–1.00	0.75–1.00	
Cost ($/kW)/(total estimated cost)	**10.7**[b]/($749)	**6.1**[c]/($702)	**4.7**

[a]Volume calculation of new machine based on maximum height, width, and depth of motor components only (i.e., stator core, winding extensions, and rotor excitation cores).

[b]Requires 1 kg of high grade PMs at $90/kg.

[c]Includes additional cost of 11 kg steel and 3 kg copper wire (+$40.00) but eliminates 1 kg magnet (-$90.00).

Conclusion

- The prototype engineering design drawings for the novel flux coupling motor were completed, and the parts are being machined and fabricated.
- The prototype motor will be completed in early FY 2011.
- From the simulation results, the PM-less motor is feasible to meet the FreedomCAR 2020 motor targets for weight and volume while significantly reducing costs compared to current PM motors.
- Motor performance can be improved by using brushless adjustable field excitation.
- The breakthrough in the mechanical design enabled the motor speed to reach up to 14,000 rpm.
- Higher motor operating temperatures can be achieved. This benefit will be evaluated through the prototype tests in FY 2011.
- The prototype test results will help us to evaluate the shielding effects of the solid rotor wedges and the improvements needed for this type of flux coupling motor.

Publications

1. John Hsu and Randy Wiles, "Novel Flux Coupling Machines Internal Design Review," presentation to ORNL and outside industry reviewer, May 15, 2010, NTRC, Knoxville, Tennessee 37932.
2. John Hsu and Randy Wiles, "Novel Flux Coupling Machines," Presentation No. Ape-005, 2010 U.S. DOE Hydrogen Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, June 7–11, 2010.

References

1. Nicola Bianchi and Thomas M. Jahns, "Design, Analysis, and Control of Interior PM Synchronous Machines," Tutorial Course Notes, IAS (copyright 2004).
2. J. S. Hsu, "High Strength Undiffused Brushless Machine and Method," US Patent 7,518,278, April 14, 2009.
3. J. S. Hsu, "Electric Machine for Hybrid Motor Vehicle," US Patent 7,270,203, Sept. 18, 2007.

Patents

Three 2010 patents were granted to this project by the U.S. Patent and Trade Mark Office.

1. John S. Hsu, "Permanent Magnet Machine and Method with Reluctance Poles and Non-Identical PM Poles for High Density Operation," U.S. Patent No. 7,719,153, May 18, 2010.
2. John S. Hsu, Laura D. Marlino, and Curtis William Ayers, "Method of Making Hermetic Seals for Hermetic Terminal Assemblies," U.S. Patent 7,695,663, April 13, 2010
3. John S. Hsu, and John W. McKeever, "High Pressure, High Current, Low Inductance, High Reliability Sealed Terminals," U.S. Patent 7,683,264 B2, March 23, 2010.

4. Systems Research and Technology Development

4.1 Benchmarking Competitive Technologies

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Objectives

- Provide status of nondomestic hybrid electric vehicle (HEV) technologies through assessment of design, packaging, fabrication, and performance during comprehensive evaluations.
  - — Compare results with other HEV technologies.
  - — Distribute findings in open literature.
- Support FreedomCAR program planning and assist in guiding research efforts.
  - — Confirm validity of the program technology targets.
  - — Provide insight for program direction.
- Produce a technical basis that aids in modeling/designing.
- Foster collaborations with the Electrical and Electronics Technical Team (EETT) and Vehicle Systems Analysis Technical Team (VSATT) on benchmarking activities.

Approach

- Choose vehicle subsystem.
  - — Evaluate potential benchmarking value of various HEVs.
  - — Consult with original equipment manufacturers (OEMs) as to which systems are most beneficial.
- Tear down power converter unit (PCU) and electronically controlled continuously variable transmission (ECVT).
  - — Determine volume, weight, specific power, and power density.
  - — Assess design and packaging improvements.
  - — Conduct tests on magnets and capacitors.
- Prepare components for experimental evaluation.
  - — Develop interface and control algorithm.
  - — Design and fabricate hardware necessary to conduct tests.
  - — Instrument subsystems with measurement devices.
- Evaluate hybrid subsystems.
  - — Determine peak and continuous operation capabilities.
  - — Evaluate efficiencies of subsystems.
  - — Analyze thermal data to determine assorted characteristics.

Major Accomplishments

- Selected the 2010 Toyota Prius for evaluation based on anticipated automotive manufacturer interest in the system due to the integrated cooling technique used in the PCU.
- Conducted design/packing studies of the 2010 Prius PCU and ECVT and determined various improvements and tradeoffs when compared to the 2004 Prius and Camry hybrid designs.
- Bypassed the 2010 Prius PCU motor inverter controls to allow full control over testing conditions.
- Mounted intensive efforts to disassemble and evaluate key components within the PCU/ECVT.
- Assessed mass, volume, power density, and specific power of various PCU/ECVT components.
- Evaluated efficiency, performance, and continuous capabilities of the 2010 Prius subsystems.
- Communicated effectively with EETT and VSATT to develop project direction and test plan and convey test results.

Future Direction

- Focus benchmarking efforts on technologies of interest to DOE, EETT, and VSATT.
- Adopt approaches similar to those of previous benchmarking studies while working to meet the universal need for standardized testing conditions.

Technical Discussion

Much like the 2007 Camry and 2008 Lexus LS 600h PCU designs, the size and proportions of the 2010 Prius PCU, shown in Fig. 1, are similar to those of a conventional 12 Vdc car battery. The 2010 Prius PCU weighs 13.0 kg versus about 17.4 kg and 17.9 kg for the 2007 Camry and 2008 LS 600h PCUs, respectively. A reduction of mass is expected when considering the lower power rating of the 2010 Prius. Another explanation for the reduction in mass is that the 2010 Prius uses a lightweight aluminum cooling infrastructure, whereas the 2004 Prius and 2007 Camry designs use a cast aluminum heat exchanger. Interestingly, the 2010 Prius PCU volume of 16.2 L is significantly greater than that of the 11.7 L and 13.7 L volumes of the Camry and LS 600h PCUs.

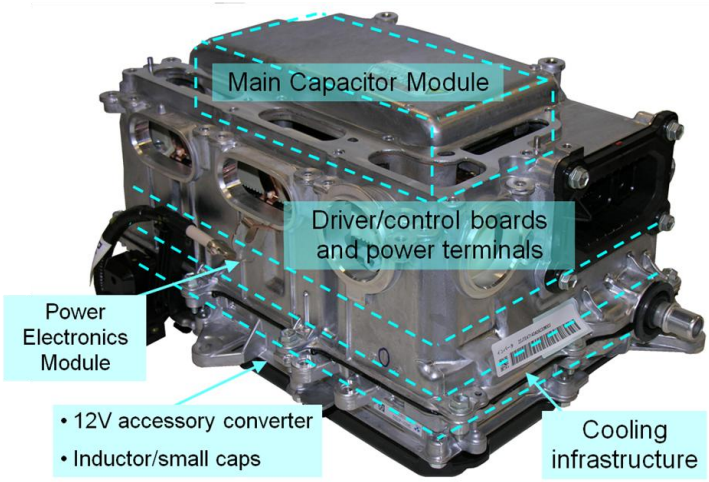


Fig. 1. Compartments of the 2010 Prius inverter and converter assembly.

It should be noted that both second and third generation Prius PCUs include a 202 V to 12 V direct current-direct current (dc-dc) converter for the accessory voltage supply, replacing the alternator. Connector terminals are connected to the 202 V battery supply, and additional connector terminals provide a fused link from the 202 V battery supply for the external inverter which drives the air conditioning (A/C) compressor. This small, three-phase inverter for the compressor is located within the

2004 Prius PCU. One coolant port is located below the interface to the vehicle electronic control unit (ECU) and the other coolant port is located on the opposite end of the PCU. The ethylene-glycol and water mixture flows from the PCU output port through a heat exchanger on the ECVT and subsequently to a radiator which is separate from the high temperature internal combustion engine (ICE) coolant radiator. Motor and generator interconnections differ significantly: in the Camry design only three bolts secure the cable harness to the PCU whereas the 2010 Prius and LS 600h designs include bolts which secure the cables directly to terminals in addition to the mechanical support from cable harness bolts.

Within the 2010 Prius PCU are components associated with a bidirectional dc-dc converter, motor inverter, and generator inverter; their general locations are shown in Fig. 2. Contrary to the Camry PCU design described in reference [1], but similar to the LS 600h {reference [2]}, the 2010 Prius controller, power supply, and driver electronics for the bidirectional dc-dc converter and inverters are grouped together onto two printed circuit boards located in the uppermost compartment (Fig. 2). The Camry PCU design includes four separate printed circuit boards dedicated to these functions, and the bidirectional dc-dc converter printed circuit boards and power electronics are located in a separate compartment. The main capacitor module shares the uppermost compartment and includes many small capacitors which are combined to serve as two large capacitors, one at battery level and one on the output of the boost converter. Similar to the 2004 Prius, the main capacitor module is a separate unit and is not molded with the housing of the PCU, as are the Camry and LS 600h capacitor modules. Attached to the side of the main capacitor module is a small 54 kΩ ceramic resistor that is connected across the high voltage (HV) dc link capacitor terminals and is located on the side of the PCU. The resistor, sized the same as those in the Camry and LS 600h, functions as a voltage bleed off for the capacitor and may contribute some filtering effects.

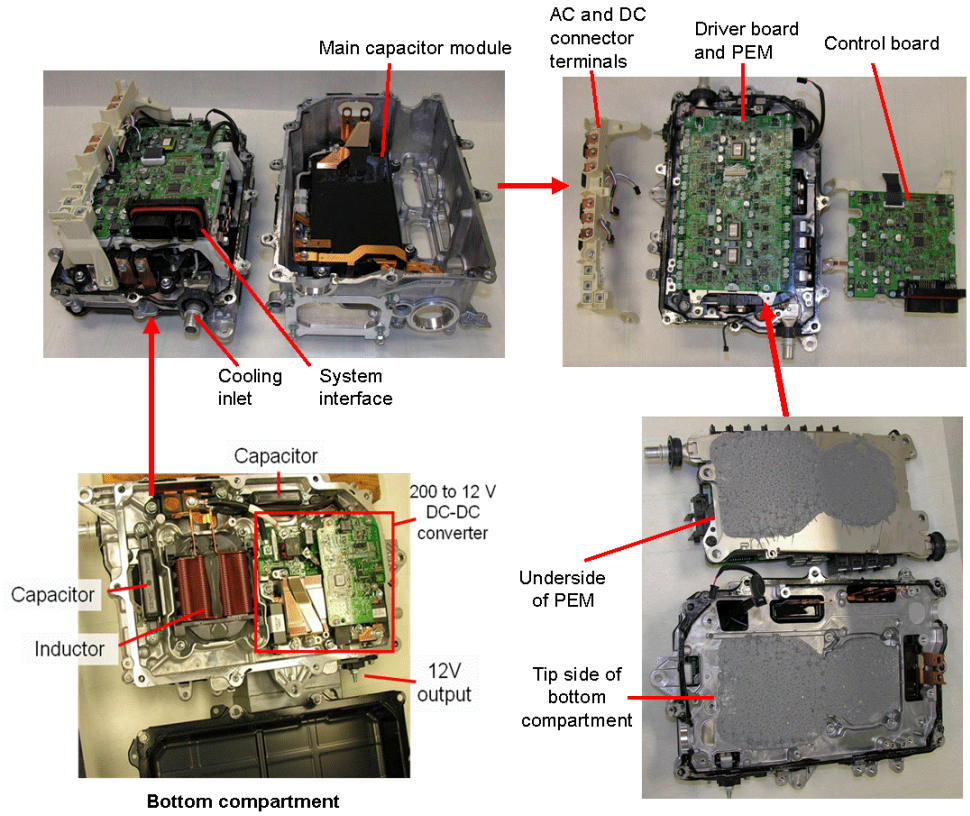


Fig. 2. 2010 Prius PCU teardown.

The 2010 Prius and LS 600h power electronics devices are located in the compartment below the controller and driver electronics, and the bidirectional dc-dc converter power electronics are grouped together with the inverter power electronics. While the power electronics module (PEM) and cooling infrastructure are one unit, separate sections are shown in Fig. 2 because the lowermost compartment also uses the heat exchanger. The lowermost compartment houses the 200 V to 12 V dc-dc converter as well as the large inductor and small capacitors associated with the bidirectional dc-dc boost converter which supplies the motor and generator inverters.

Because the nickel-metal hydride battery is rated at 27 kW, it is assumed that the bidirectional dc-dc converter will not operate at power levels exceeding 27 kW. Similarly, it is assumed that the motor inverter has a peak power rating that matches the measured power rating of the motor. A 201.6 Vdc battery supplies power to the PCU, which is connected to the low voltage (LV) side of the boost converter. A 470 V, 315 μF, capacitor is connected across the input with a 225.6 μH inductor between the battery and the boost converter PEM. A small 53.8 kΩ resistor is in parallel with an 860 V, 0.562 μF, capacitor, which is integrated into the main capacitor module. Additionally, separate 900 V, 0.8 μF, and 950 V, 0.562 μF, filter capacitor modules are located in the bottom portion of the PCU, and a 750 V, 888 μF, smoothing capacitor, which is connected to the HV side of the boost converter, is a part of this parallel configuration. This HV bus serves as the dc link for the motor and generator inverters. The boosted voltage ranges from 202–650 Vdc depending on driving conditions such as desired acceleration and required regenerative braking and is controlled accordingly by commands from the motor-generator (MG) ECU and the vehicle ECU.

Power Converter Unit Teardown

Figure 2 shows the 2010 Prius PCU with the upper half of the housing removed and placed beside it. Eleven bolts hold the assembly together with a compound similar to room temperature vulcanizing silicone applied to the mating surfaces to seal the unit. The main capacitor module is secured in the housing with four bolts, and the small white ceramic resistor is fastened to the side of the module. The copper bus bars (near the bottom-right side of Fig. 2) connect directly to the hybrid battery supply. The common bus bar immediately enters the capacitor module while the positive input traverses the width of the PCU and then enters the capacitor module and is also connected to the inductor in the bottom compartment by means of long vertical bus bars.

The control/interface circuit board and the dc input, dc output, motor, and generator connection terminals were removed, as shown in the upper left portion of Fig. 2. This circuit board, shown on the right in Fig. 2, is multilayered and includes power regulation electronics; two identical MG microprocessors; a boost-converter microprocessor; two Tamagawa AU2802 integrated circuits for MG speed/position detection; and hardware for vehicle communication, MG current measurement, safety interlock devices, and temperature feedback. The design of this circuit board is very similar to that of the 2007 Camry. The circuit board seen in the middle portion of Fig. 2 is the driver/power supply board, and it is also similar to that of the Camry. The driver board includes regulated isolation power supplies; isolated driver electronics; hardware to prevent faults and overlapping; and voltage, current, and temperature sensing circuitry for each insulated gate bipolar transistor (IGBT). There are 22 groups of five pins for driving and sensing purposes for each IGBT.

The ac and dc connector terminals are visible in Fig. 2. As copper bus bars extend from the motor and generator inverter outputs, two of the three phases pass through black current transducers before reaching the connection terminals at the top of the assembly. Two interlock devices are located on the connection terminal assembly to disable the system if the terminal cover or battery connector is removed. In the lower right portion of Fig. 2, the PEM with integrated cooling has been removed and placed beside the bottom compartment. Input and output ports for the cooling system have rubber seals to prevent moisture

from entering into the interior of the PCU assembly. A significant amount of gray thermal grease is used between the bottom side of the cooling structure and the bottom compartment. Four small, cylindrically shaped pieces are associated with the four bolts that are used to mount the large inductor in the bottom compartment. The footprint of the 200 V to 12 V dc-dc converter is larger than the inductor footprint, and more thermal grease is used in this area of the mating surface. Two separate capacitor modules (900 V, 0.8 µF, and 950V, 0.562 µF) have two copper bus bars which extend vertically from the bottom compartment. The bus bars are substantially thick (probably to reduce inductance and resistance) and bolt directly to the PEM. Three copper bus bars are grouped together, two of which are for each terminal of the inductor. The other bus bar provides a common for the 200 V to 12 V dc-dc converter, and the positive supply for this converter is connected to the input terminal of the inductor, which is visible in the lower left portion of Fig. 2. The location of the two capacitors is indicated, and the top of the inductor is also visible in this image. In all of the previous PCU designs, the inductor is completely enclosed with potting compound, with no copper visible. The output of the inductor is connected to the middle point of the dc-dc converter leg and the leg is in parallel with the motor and generator inverter legs, thereby connecting directly to the dc link. Circuitry for the 12 V converter is also indicated in this image.

Mass and volume measurements were made for the 2010 Prius motor inverter, dc-dc converter, and their subcomponents; however, for certain components the dimensions and volumes are approximate as the geometries are sometimes irregular. Many of the components of the PCU are shared between the inverters and dc-dc converter. Thus, the mass and volume of these items were tallied separately and then divided accordingly. As explained in more detail in publication [1], based on device count about 55% of the power electronics are dedicated to the motor inverter, 27% to the generator inverter, and 18% to the dc-dc converter. Because the devices in the bidirectional dc-dc (boost) converter are larger, the percentage of PEM area devoted to each component is about 49%, 29%, and 22% for the motor inverter, generator inverter, and dc-dc converter, respectively. It is therefore reasonable to distribute the mass and volumes of the shared items across the motor inverter, generator inverter, and dc-dc converter according to the percentages 50%, 30%, and 20%, respectively. For example, about 50% of the driver board is dedicated to the motor inverter because about 50% of the IGBTs are included in the motor inverter. Likewise, 20% of the mass and volume of the shared items is attributed to the dc-dc converter. The large capacitor module is the largest and heaviest PCU component.

The peak density and peak specific power of both the motor inverter and the bidirectional dc-dc converter were calculated to be 11.1 kW/L and 16.6 kW/kg and 5.7 kW/L and 5.3 kW/kg, respectively. Because the mass of the 2010 Prius PCU is much lower than that of the other systems, the inverter specific power is significantly higher than that of the Camry, and especially the 2004 Prius. Even so, the specific power calculation seemed quite large upon initial inspection. However, considering that about 2 kg is devoted to the accessory converter, the mass of the inverters and boost converter sum up to only 11 kg. The LS 600h has the highest power density since the power capability of the LS 600h motor inverter is much higher than that of the other systems while their sizes are relatively similar. Because the 2010 Prius PCU volume is reasonably high, the inverter power density is lower than that of the LS 600h and Camry. Although the power capability of the 2010 Prius bidirectional dc-dc converter increased by about 35% in comparison with the 2004 Prius, the mass only increased by about 6% and the volume decreased by about 6%. Thus, there was an improvement of the specific power and peak density of the boost converter, but not as significant as that of the motor inverter.

The main capacitor of the 2010 Prius PCU is shown in the upper left portion of Fig. 2. The 2010 Prius and LS 600h capacitor modules contain both capacitors, which are connected to the HV and LV side of the bidirectional boost converter, whereas the corresponding Camry capacitors are housed in separate modules. The main capacitor was x-rayed to determine capacitor characteristics. The x-ray shows that there are three discrete submodules in parallel that form the 888 µF capacitor, with each submodule having a capacitance of 296 µF. The equivalent Camry and 2004 Prius capacitor has 12–87 µF and 8–

142 µF submodules in parallel to provide a total capacitance of 2,098 µF and 1,130 µF, respectively. The x-ray also shows that there are two 157.5 µF submodules which are in parallel and form the 315 µF battery level filter capacitor. The cells which form these capacitors span the entire width of the module, whereas the Camry and 2004 Prius capacitors are much smaller and only span half of the module's width. The LS 600h cells are also small, yet they are vertically oriented. The fuse for the 202 V supply to the A/C compressor is secured to the side of the capacitor module. The small 0.562 µF capacitor is on the opposite end of the module.

A primary function of these capacitors is to attenuate voltage transients and surges which are associated with the buildup and collapse of the energy stored in the 329 µH inductor (shown in Fig. 2). The lower switch (three IGBTs in parallel) of the dc-dc converter cycles at 5 or 10 kHz with a variable duty cycle to build up and store energy in the inductor. As the duty cycle is varied, the output voltage of the inductor also varies accordingly. Because of the inherent voltage ripple and potentially high voltage produced by the collapsing inductor field, these capacitors serve to stabilize the battery voltage and dc link voltage and protect the power electronics devices from potential overvoltage conditions. The inductor has two coils in series, and the core was secured with bolts and immersed in a potting compound.

A total of 22 IGBTs and antiparallel diodes are located in the PCU, all sharing the same dc link. As indicated in Fig. 3, the motor, generator, and bidirectional boost converter power electronics are combined into one package. All the upper devices are displayed in the lower half of the image, and likewise, all of the lower devices are seen in the upper half of Fig. 3. The motor inverter comprises 4 IGBTs and diodes in each phase, with 12 IGBTs and 12 diodes in its entirety. The generator has only two IGBTs and diodes for each phase, with a total of six IGBTs and diodes. While the boost converter devices only total up to four IGBTs and diodes, they are much larger than those of the motor and generator inverters. Coolant hose connections are located on each end of the heat exchanger, allowing coolant to enter one side and absorb heat as it traverses across the width of the PEM and exits the other port. As seen in Fig. 4, the cooling infrastructure runs beneath the drive and sense pins of the IGBTs, thereby facilitating flow along the length of the PEM before passing through the thin cooling channels. This promotes more uniform heat transfer among the power electronics devices. A thermistor is located on the coolant inlet just inside the PCU. Although the thermistor is secured to the coolant inlet, the actual sensing device is not flush with the aluminum surface of the inlet.

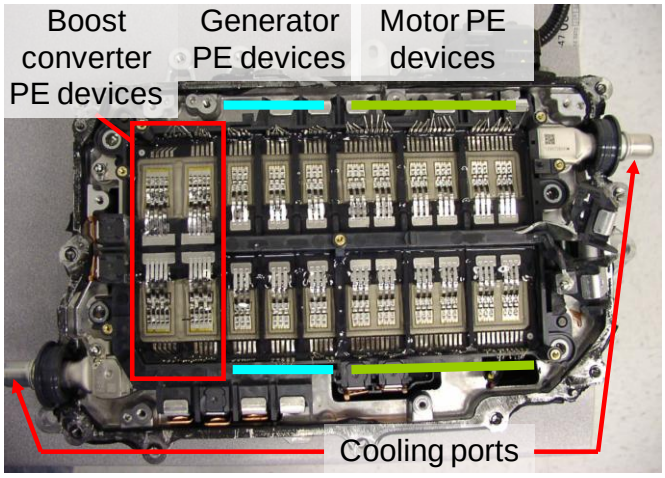


Fig. 3. 2010 Prius PEM.

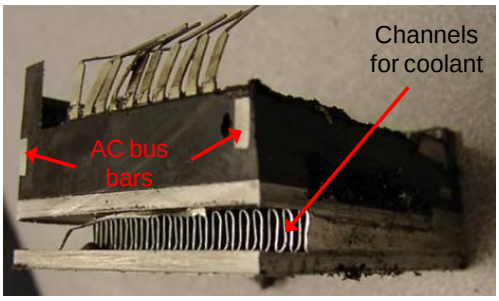


Fig. 4. Cross section of 2010 PEM.

One of the most noticeable discrepancies between the 2010 Prius PEM and previous PEM designs is the orientation of the power electronics devices. In the 2010 Prius, the power electronics devices are oriented in a manner such that the drive and sense pins are on the outer perimeter of the module. While this likely presents opportunities to improve the layout of the driver circuitry, it more importantly allows more phase legs to be placed along the length of the dc bus bar. The Camry and 2004 Prius designs have the motor and generator inverters on opposite sides of the dc bus, with the three-phase outputs also on opposite sides and on the outer periphery of the PEM. By contrast, the upper and lower IGBTs of each inverter are on opposite sides of the dc bus in the 2010 Prius. The black dividers between each phase are thicker on the top than on the bottom portion in the 2010 Prius PEM (Fig. 3). This is because the alternating current (ac) bus bars (indicated in Fig. 4) are molded in this black material and are fed to the two three-phase terminal outputs on the side of the PEM.

To help portray the layout, it is advantageous to trace the path from the positive dc link through one phase leg to the negative dc link. There are two layers of ribbon bonds on each side of the dc link; three on the top layer and three on the bottom layer, which is slightly visible in Fig. 5. The bidirectional boost converter uses five ribbon bonds per device. There are also several layers of bus bars for the dc link and ac outputs, extending completely through the middle of the PEM, a few of which are visible in the left side of the cross section in Fig. 5. In Fig. 5, the bottom bus bar on the right side of this group of bus bars in the middle is the positive dc link, which is connected with the three lower ribbon bonds to the collectors of the upper phase legs (all on the right). If the IGBT is activated, current flows out the emitter through the three upper ribbon bonds to the upper bus bar. The collector of the lower IGBT (shown in Fig. 3) is connected by three lower ribbon bonds to this horizontally oriented bus bar, as is the ac output bus bar, which is vertically oriented and placed between each phase. If the lower IGBT is activated, current passes through the IGBT and out the emitter to the three upper layer ribbon bonds which attach to the negative dc link.

The 2010 Prius layout appears to be more orderly and is advantageous in ways such as fewer attachment points and shorter overall conductor length, perhaps improving the parasitic parameters of the devices in addition to the improved parasitic parameters of ribbon bonds versus wire bonds. While there are some inherent benefits to this packaging approach, there are also some negative aspects. For example, the 2007 Camry PEM contains six IGBTs and diodes for each phase leg of the motor inverter (versus four for the 2010 Prius). In the Camry PEM described in reference [1], a third IGBT is located beneath the dc link bus bars in the middle. An interesting comparison could be made if three more phase legs were added (one for each phase) to the 2010 Prius motor inverter to make an even comparison with the Camry PEM. It seems to be that the 2010 Prius packaging approach requires parallel IGBTs to be placed along the length of the dc link. This is one particularly attractive aspect of the LS 600h design, which consists of vertically oriented PEMs. Nonetheless, the 2010 Prius PEM sufficiently includes the bidirectional boost converter, as opposed to having separate modules such as those of the Camry and 2004 Prius.

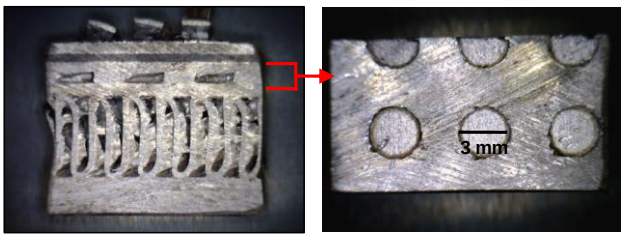
Fig. 5. Cross-section of the 2010 boost converter power devices.

External dimensions of the 2010 Prius, 2007 Camry, 2008 LS 600h, and 2004 Prius power electronics devices were measured for comparison. The size and appearance of the LS 600h IGBTs and diodes are similar to those of the bidirectional dc-dc converter of the Camry. The square area of silicon (Si) for each IGBT has decreased from 131.9 mm^2 to 109.4 mm^2, and the total square area of Si used on the motor inverter has decreased from 1,583 mm^2 to 1,313 mm^2, a 17% reduction in moving from the 2004 Prius to the 2010 Prius design.

The 2004 Prius IGBT consists of a planar gate structure and includes areas in the drift region below the emitter "n+" and "p" regions which do not pass as much current as the drift region areas below the gate. This inefficiency is due to the shape of the inversion layer which is formed when using a planar gate structure. The Camry, LS 600h, and 2010 Prius IGBTs consist of a trench gate structure which forms a more uniform inversion layer during on-state operation, and therefore higher current densities are created in the drift region. All IGBTs include leads for semiconductor junction temperature measurement feedback, gate voltage control, current measurement, and emitter voltage feedback. These signals are used to control the devices and prevent fault conditions from occurring.

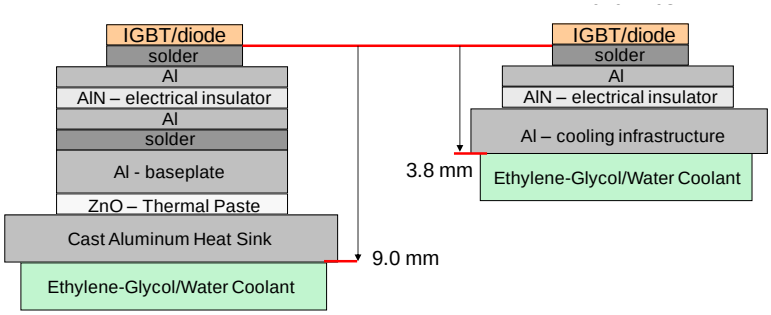
An overall view of the layers within the PEM is given in Fig. 6. Despite the sacrifice of thermal conduction characteristics, numerous 3 mm diameter holes are introduced to alleviate stresses associated with thermal expansion, which are particularly high at the interface of materials with differing coefficients of thermal expansion. Figures 6(a) and 6(b), cross sections through the vertical and horizontal planes of the module, show these perforations (red indicator).

Figure 7 shows a comparison of the thermal conduction paths in the 2004 and 2010 Prius from the power electronics devices to the ethylene-glycol-water coolant. Both systems have the power electronics devices soldered directly to an aluminum substrate and both use aluminum nitride (AlN) ceramic insulators for electrical isolation from the cooling infrastructure. Below the AlN insulators, the 2010 Prius has an aluminum layer which has been brazed to the cooling infrastructure, while the 2004 Prius PEM has an aluminum layer below the insulator that has been soldered to a thick aluminum baseplate, which is bolted to a cast aluminum heat sink with zinc oxide thermal paste between the baseplate and heat sink to fill any voids between the mating surfaces. Ultimately, the length of the conduction path from the bottom of the power electronics devices is 3.8 mm for the 2010 Prius versus 9.0 mm for the 2004 Prius, a 58% decrease in length. Additionally, a solder layer and thermal paste layer have been eliminated, both of which have relatively low thermal conductivities (compared to aluminum), and therefore the overall thermal conductivity has greatly increased.



(a) **(b)**

Fig. 6. Cross-sectional views of extracted 2010 Prius PEM: (a) side; (b) top.



(a) **(b)**

Fig. 7. Comparison of thermal conduction path in 2004 Prius (a) and 2010 Prius (b).

ECVT Teardown

The overall functionality of the 2010 Prius ECVT, shown in Fig. 8, is similar to the Camry and Prius, yet there are significant differences between the subsystem designs. All systems use the sun gear of a planetary gear that is connected to the generator with a hollow rotor shaft, through which a shaft connected to the ICE passes and connects to the planetary carrier. The ring of the planetary gear is connected directly to the motor output in the 2004 Prius and to the motor through a high-speed reduction gear in the 2010 Prius and 2007 Camry. The 2010 Prius, 2004 Prius, and Camry planetary rings drive the differential output through a series of drive gears.

One of the most noticeable differences between the 2010 Prius electric motor (Fig. 9) and previous Toyota designs is the design of the rotor. While the PMs are in a 'V' shaped orientation, the x-ray in Fig. 9(b) indicates the presence of large openings in the rotor laminations. These openings certainly reduce the overall mass of the rotor and may have other design implications such as effecting the reluctance component of the torque, which could be impacted by these large interior air gaps. Additionally, the design may have reduced eddy current losses at the shaft, as the large voids would deter flux transients from occurring in this area. An additional design feature of interest is the small inner diameter of the rotor lamination, and thus the outer diameter of the rotor shaft. Previous designs consist of a rotor shaft with a much larger outer diameter. The outer diameter of the LS 600h motor, 2010 Prius motor, and Camry motor stator laminations are 7.88 in., 10.395 in., and 10.395 in., respectively. Stator lamination stack lengths for the LS 600h, 2010 Prius, and Camry motor are 5.33 in., 2.0 in., and 2.4 in., respectively. As the diameters of the 2010 Prius and Camry motor stators and rotors are identical, the stator core mass per unit stack length (without copper) of the 2010 Prius stator is roughly equal to that of the Camry; 10.36 kg/2 in. = 5.18 kg/inch versus 12.38 kg/2.4 in. = 5.16 kg/inch, respectively. However, the rotor mass per unit length of the 2010 Prius is slightly lower than that of the Camry; 6.7kg/2 in. = 3.35 kg/inch versus 9.03 kg/2.4 in. = 3.76 kg/inch.

Another significant design difference in the ECVT is the generator shown in Fig. 10. While the rotor is similar to previous Toyota designs (note the large inner diameter), the stator is significantly different, with 12 stator teeth versus a typical count of 48 teeth and concentrated windings all encapsulated within a mold. The light grey mold was analyzed for material composition, and it is composed of 58.11% Al, 39.42% O, and 2.47% Na, by mass with fibers that are 49.3% O, 30.1% Si, 12.22% Al, and 8.34% Ca, by mass.

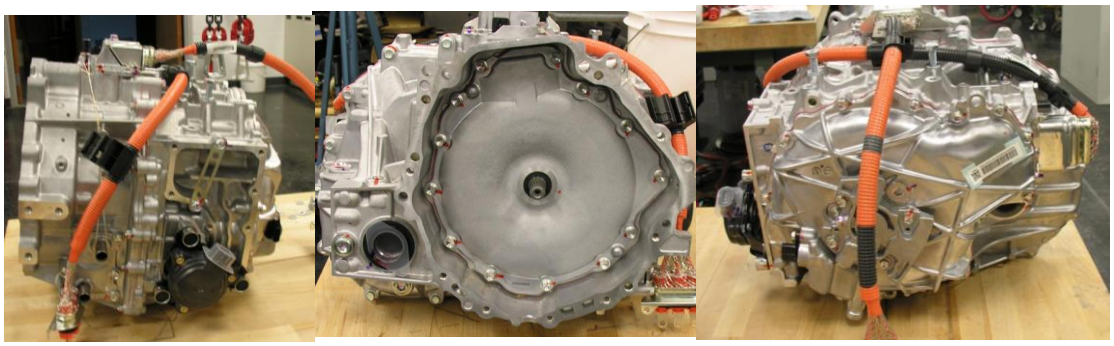
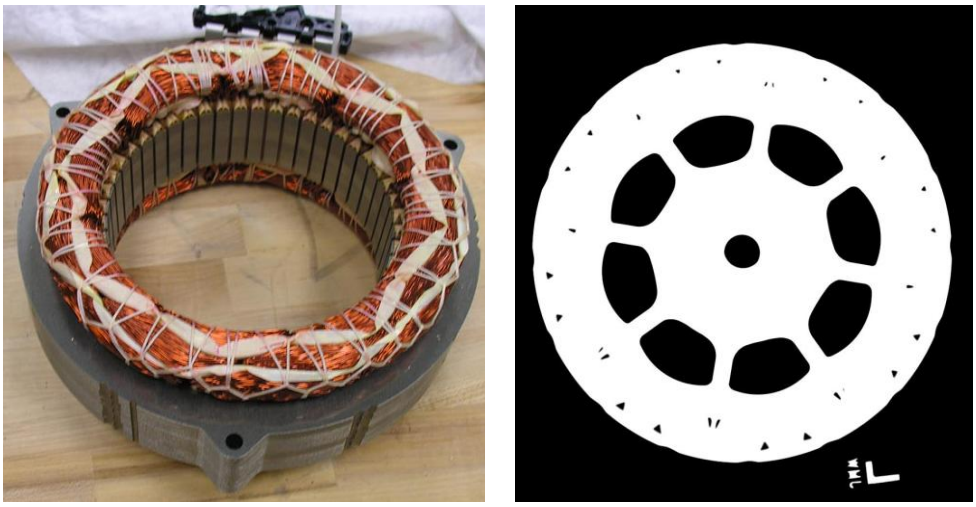


Fig. 8. 2010 Prius ECVT



(a) **(b)**

Fig. 9. 2010 Prius motor stator (a) and x-ray of motor rotor (b).

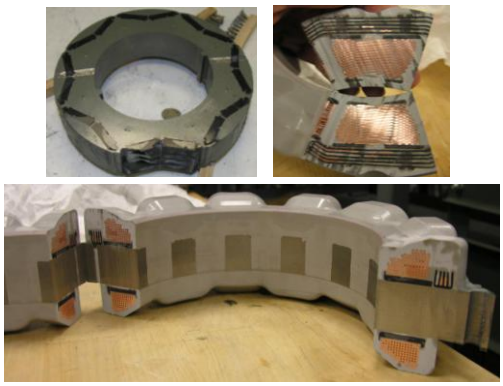


Fig. 10. 2010 Prius generator.

A comparison of the specific power and power density of four HEV systems, the 2010 Prius, 2004 Prius, 2007 Camry, and Lexus LS 600h, is provided in Table 1. Note that the heat exchanger and speed reducer were accounted for in the motor mass and volume calculations. The results indicate that the peak power density of the 2010 Prius motor has improved over that of the 2004 Prius but is significantly lower than that of the Camry. This is because the motor volume is relatively similar with only a 0.4 in. reduction of stack length, yet the peak power is lower. Mass reductions in the 2010 Prius yield nearly equal specific power numbers in comparison with the Camry motor. The LS 600h has high values of power density and specific power. Peak power capabilities were used in these calculations, and the use of continuous ratings may yield closer results for the motor assessments. However, it is difficult to generalize continuous power ratings as they are based upon a variety of conditions such as coolant temperature, stator temperature limit, and motor speed. Nonetheless, the double-sided cooling technique has an apparent advantage over previous designs.

Table 1. Comparison of Specific Power and Power Densities for Various HEV Components

Component and parameter	2010 Prius (60 Kw)	Lexus LS 600h (110 Kw)	2007 Camry (70 Kw)	2004 Prius (50 Kw)
Motor				
Peak power density (kW/L)	4.8	6.6	5.9	3.3
Peak specific power (kW/kg)	1.6	2.5	1.7	1.11
Inverter (excluding generator inverter and buck/boost converter)				
Peak power density (kW/L)	11.1	17.1	11.7	5.7
Peak specific power (kW/kg)	16.6	14.8	9.3	5.7

Experimental Evaluation

We conducted various evaluations to determine PCU and ECVT operational characteristics such as efficiency, continuous capability, and performance. Initial tests included measurement of back electromotive force voltage, no-load losses, and locked rotor torque. These tests provide parameters and characteristics of the motor which are useful for approximating the capabilities of the motor. Secondary evaluations included efficiency, performance, and continuous analyses upon the subsystems. Before any tests could be conducted, the ECVT had to be modified to provide access to the motor shaft. The only shafts externally accessible are the engine input shaft and the differential output shafts. Although the differential gear is indirectly connected to the motor, power measurements through these gears would not be accurate enough to make precise motor efficiency calculations. A shaft was designed and fabricated to provide external access to the motor rotor. The fabricated shaft was fed directly to a speed and torque transducer. The other side of the torque transducer was coupled to a speed reduction gearbox. The

gearbox is capable of handling speeds up to 18,000 rpm and the dynamometer can operate at power levels of up to 400 hp. All hardware on the high speed portion of the shaft was designed to have face mount couplings, which prevents alignment issues and provides extra safety as the shafts are shorter and aren't exposed.

Extensive efforts were made to ensure that the ECVT modification did not impact cooling or lubrication characteristics by inadvertently hindering or enhancing oil flow. The system depends greatly on proper oil circulation for heat conduction and lubrication. Oil is circulated with a mechanically driven trochoid oil pump and an electrically driven trochoid oil pump. Consideration of proper shaft support was also an important part of the process to ensure that no bearings were overloaded. A heat exchanger located at the side of the ECVT is in series with the inverter. Thermocouples were tactically placed to monitor stator, inner/outer case, and oil temperatures both near and far from the heat exchanger. Additional instrumentation was added to the ECVT and PCU, and a data acquisition system was developed to collect thermal, mechanical, and electrical data such as coolant temperatures, heat sink temperatures, torque, speed, currents, and voltages. These data were collected and fed into an immense spreadsheet and saved for future use. An optimal control scheme was developed to ensure the most efficient operation of the motor throughout the entire operation range. The controller uses speed, position, and current feedback to regulate the output conditions supplied by the inverter. The OEM motor inverter controls were bypassed to allow full control over the inverter, enabling uninhibited testing of the system over various operating conditions.

Efficiency measurements of the motor and inverter were taken over the entire operation range of the motor. The efficiency contour map in Fig. 11 represents the steady state efficiency characteristics of the motor for efficiencies above 60%. The peak efficiency is 96%, and efficiencies above 88% are spread over a large area of the operating region. For much of the high torque regions, a coolant temperature of ~10°C was used to permit extensive testing in this region. Otherwise, the torque levels nearing 200 Nm could only be maintained for extremely short periods of time before reaching stator temperature limits. Figures 12, 13, and 14 show the combined motor and inverter efficiency maps for dc link voltages of 650 Vdc, 500 Vdc, and 225 Vdc, respectively. The same scale was used in all of these figures to portray the phenomenon of improved efficiencies for lower dc link voltages. The peak combined efficiency for 650 Vdc in Fig. 12 is 95%. Although the peak combined efficiency for 500 Vdc is only 94%, this peak efficiency region has shifted to a lower speed and efficiencies are ultimately higher than that of the 650 Vdc efficiency map in low speed and medium torque regions. Similarly, the combined efficiency map for 225 Vdc has higher efficiencies than that with 500 Vdc and 600 Vdc in low speed and low torque regions of the map. The primary reason for this is the inverter efficiency, where switching losses decrease with decreasing voltage. Additional data, further analyses, and more elaborate documentation of the findings and results from the FY 2010 benchmarking efforts can be found in [1] in the publications list at the end of this section.

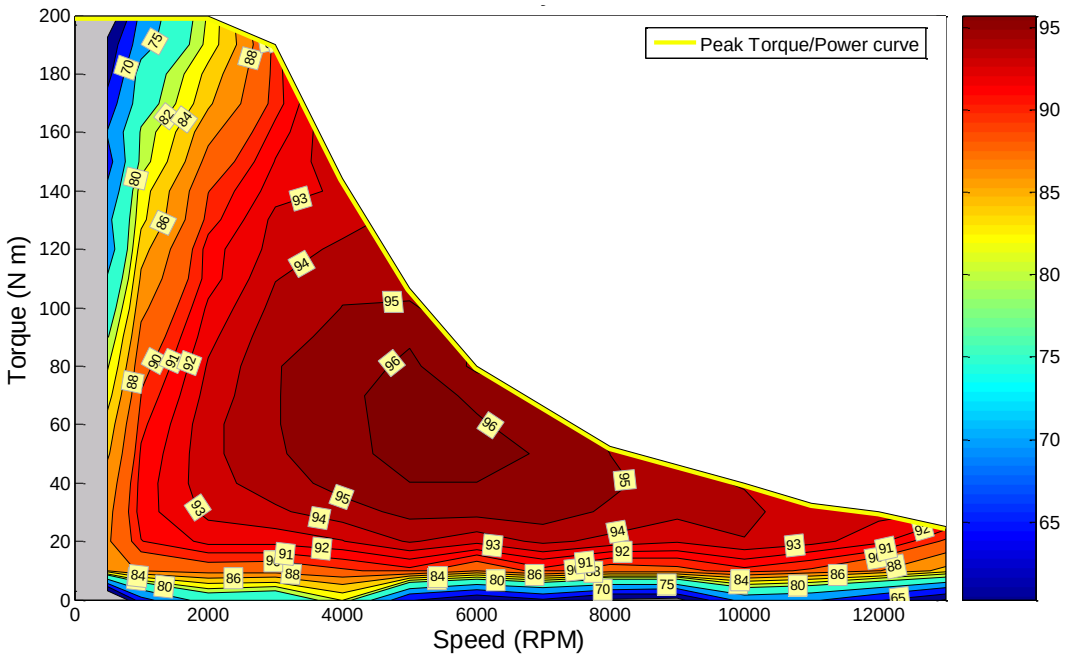


Fig. 11. 2010 Prius motor efficiency map for 650 Vdc.

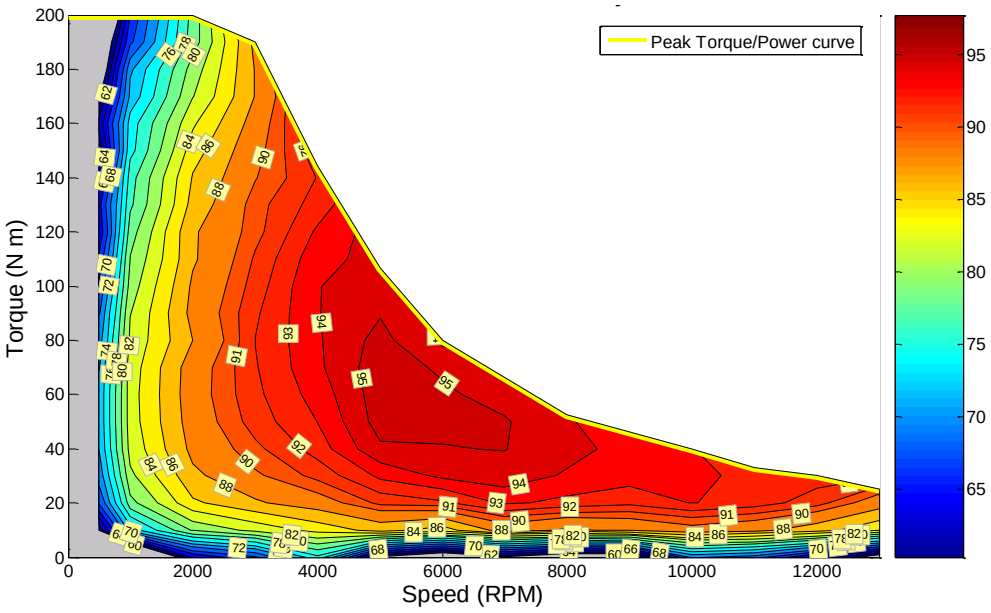


Fig. 12. 2010 Prius combined motor-inverter efficiency map for 650 Vdc.

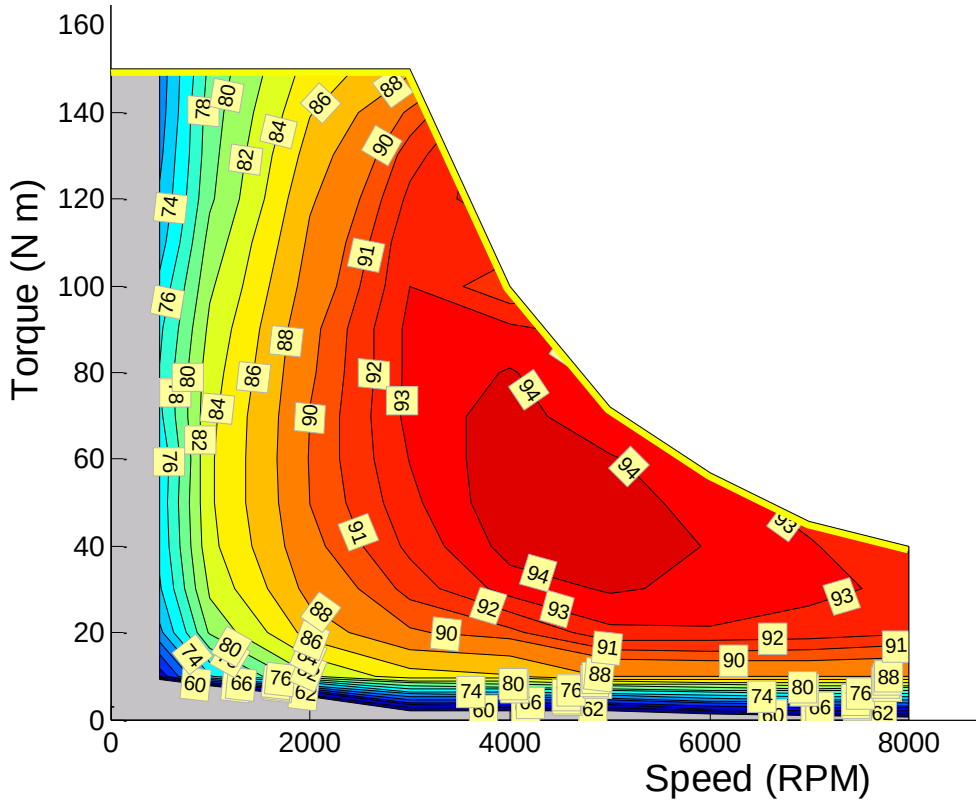


Fig. 13. 2010 Prius combined motor-inverter efficiency map for 500 Vdc.

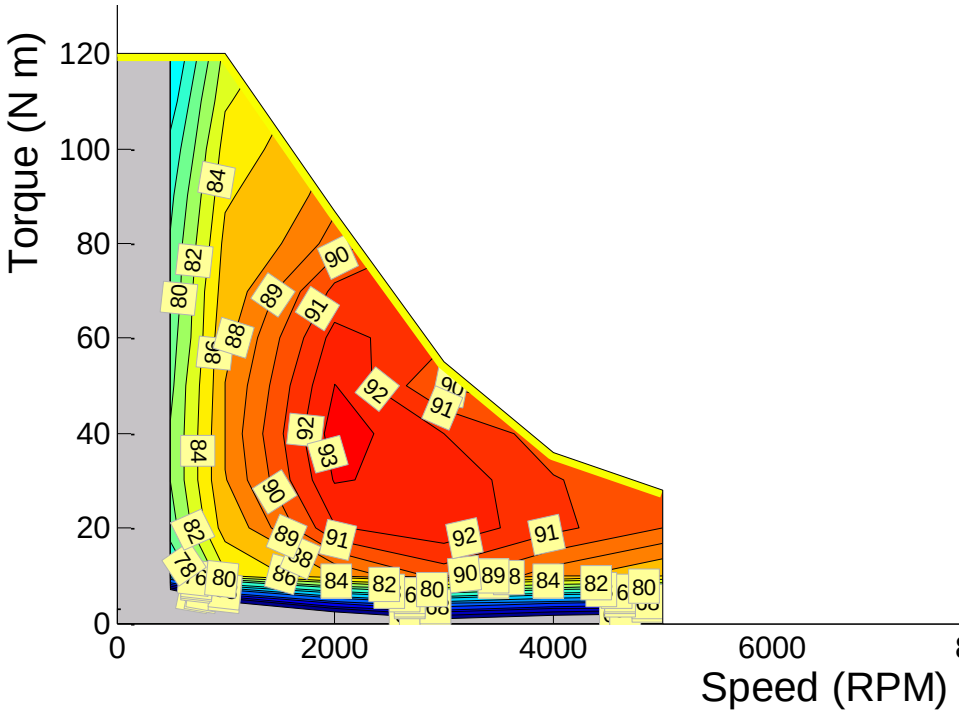


Fig. 14. 2010 Prius combined motor-inverter efficiency map for 225 Vdc.

Conclusions

Our evaluation of the 2010 Toyota Prius uncovered the following.

- Benefits of the integrated cooling technique used in the 2010 Toyota Prius lead to a significant increase in specific power in comparison with the Camry (78% increase), while the power density actually decreased slightly.
- Reduced IGBT and diode count in boost converter, which was integrated into the same module as motor and generator inverters, leading to lower costs.
- Cooling technique not as effective as LS 600h double sided cooling technique but is likely more cost effective.
- Motor stator rotor has similar PM arrangement to other models used for comparison, but overall lamination is significantly different.
- Motor lamination stack length is 2 in. versus 2.4 in. for the Camry.
- Power density of the 2010 Prius motor is slightly lower than that of the Camry and LS 600h.
- Specific power of the 2010 Prius motor, while higher than that for the 2004 Prius, is still slightly lower than that of the Camry and LS 600h.
- Motor efficiencies are above 90% for a great portion of the operation range, even more so than the Camry.
- Low dc link voltages facilitate increased efficiency for low speed and moderate torque operation regions because of reduced inverter switching losses.
- High torque and high power operation points are best suited with 650 Vdc operation.
- Peak efficiencies reached 96% for the motor.

Publications

1. T. A. Burress, et al., *Evaluation of the 2010 Prius Hybrid Synergy Drive System*, ORNL/TM-2010/253 Oak Ridge National Laboratory, 2010.

References

2. T. A. Burress, et al., *Evaluation of the 2007 Toyota Camry Hybrid Synergy Drive System*, ORNL/TM-2007-190, Oak Ridge National Laboratory, 2007.
3. T. A. Burress, et al., *Evaluation of the 2008 Lexus LS600h Hybrid Synergy Drive System*, ORNL/TM-2008/185, Oak Ridge National Laboratory, 2008.

4.2 High-Power-Density Integrated Traction Machine Drive

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Objectives

- Overall objective is to develop a reliable, fault-tolerant, integrated modular motor drive (IMMD) capable of operating at 200°C junction and 150°C ambient temperatures.
- For FY 2010, the objectives are to
  - design a demonstrator version of the IMMD with fault-tolerant controller using the most promising configuration to verify performance characteristics including power density and fault tolerance and
  - evaluate silicon (Si) insulated gate bipolar transistor (IGBT) and suitable packaging at 200°C, considering device characteristics, loss, cooling, and reliability.

Approach

- Analyze alternative fault-tolerant machine and controller configurations to identify the most promising candidates for future demonstration in prototype hardware.
- Apply the results of the initial analysis to design and build a preliminary10 kW prototype integrated traction drive in FY 2011 followed by a full-scale 55 kW (peak) prototype unit in FY 2012 and FY 2013.
- Evaluate selected Si IGBT for operation at 200°C, considering device characteristics such as loss, thermal limits, and reliability. These devices will potentially be used in device modules for IMMD to be developed in FY 2011 and FY 2012.
- Develop suitable phase-leg device module packaging concept through analysis and simulation, aiming for 200°C junction and 150°C ambient operation. The device module concept will be the basis for prototyping in FY 2011 and implementation in IMMD in FY 2012 and FY 2013.

Major Accomplishments

- Analyzed and compared a variety of alternative modular motor configurations, leading to identification of a 6P, 10 pole permanent magnet (PM) machine as the most promising configuration for further development.
- Analyzed and compared several alternative distributed controller configurations, leading to selection of a heterarchical control architecture as the best candidate for achieving fault-tolerant operation.
- Tested static and switching characteristics of IGBT at various temperatures, concluding that device losses are acceptable for operation at 200°C, but the ruggedness of the devices needs further evaluation.

- Designed a baseline 10 kW phase-leg power module package through die selection, material selection, layout design, parasitic extraction, and thermal characterization. The commercial two-pass tube cold plate is selected for cooling the phase-leg power module. Thermal performance of the packaging design with liquid cooling was analyzed. The effects of different coolants (water-glycol and transmission oil) and 150°C ambient on junction temperature were compared. The results show the baseline device module can meet the required power and temperature performance need for IMMD.

Future Direction

- In FY 2011, build and test a 10 kW demonstrator IMMD to evaluate drive system performance and fault tolerance; develop the 10 kW phase-leg power modules needed for implementing the full power IMMD. The modules should be based on low cost Si and able to operate in ambient temperatures of 150°C with junction temperatures up to 200°C.
- In FY 2012 and 2013, scale up the power level of the IMMD technology and combine with the high temperature modules to achieve high-density integrated traction motor drive.

Technical Discussion

1. Machine Performance Comparisons

1.1 Optimal Slot/Pole Combinations for Different Numbers of Phases

In this section, the set of criteria for choosing the optimal slot/pole combination for different numbers of stator phases is presented. The basic building block of the IMMD consists of a stator pole-piece fitted with a concentrated winding and a dedicated power converter unit. Considering the nature of the application, the optimal slot/pole combinations can be chosen according to the following criteria.

1. Choose a high value of the fundamental winding factor K_{w1} to maximize torque production.
2. Choose the highest least common multiple (LCM) of the number of slots, N_s, and the number of poles, N_m, to minimize cogging torque. LCM(N_s,N_m) indicates the number of cogging torque periods per full mechanical rotation.
3. Choose the greatest common divisor (GCD) of N_s and N_m that is greater than one and even. GCD(N_s,N_m) indicates symmetries in winding layout and magnetic pull between the stator iron and the rotor magnets.
4. Consider the magnetic motive force (MMF) space harmonic distribution to minimize the rotor losses.

Table 1. Key Metrics of Machines with Different Phase Numbers

	3P	4P	5P	6P
Poles	10	14	14	10
Slots	12	16	15	12
SPP	2/5	2/7	3/14	1/5
LCM	60	112	210	60
GCD	2	2	1	2
Winding factor	0.933	0.962	0.980	0.966
Max elec. freq. (Hz)	1167	1633	1633	1167
Overrating factor (%)	n/a	33	25	20
Number of modules	6	8	5	12

Reference [1] includes tables presenting the synchronous winding factor, LCM(N_s,N_m), and GCD(N_s,N_m) for 3, 4, 5, and 6P slot/pole combinations that support fractional-slot concentrated windings. These tables were used as a source for Table 1, which presents optimal slot/pole combinations for fractional slot concentrated winding (FSCW) surface PM (SPM) machines. Phase numbers between 3 and 6 were selected, and basic performance features of these

designs were compared to a baseline 12 slot, 10 pole, 3P SPM machine (Table 1). These designs are referred to as 3P, 4P, 5P, and 6P, where the number represents the number of phases.

Table 2 presents the key machine dimensions and magnet characteristics that were held constant for all of the machine designs. Figures 2 to 5 provide key graphical information for each of these four machine designs including a machine cross-sectional view, a plot of the winding function for a single phase winding, and a plot of the spatial harmonic components that are present in the winding function. The highlighted entries in Table 2 identify the strengths of each candidate. The 3P design has a relatively low electrical frequency and an even value of GCD. Since the 6P design has the same stator and rotor structure as the 3P design, their characteristics are quite similar. However, the higher winding factor and reduced torque ripple of 6P are advantages due to the increased number of phases. The slot/phase/pole (SPP) value of 2/7 is highlighted for the 4P design because previous work has shown that the families of SPP=2/5 or SPP=2/7 are particularly well suited for high speed SPM machine achieving optimal flux weakening conditions [3]. The 5P design has the highest LCM value and winding factor and the minimum number of modules.

Table 2. Machine Dimension and Material Constraints

Stator OD (mm)	274	Rotor OD (mm)	142
Active axial length (mm)	75	Magnet thickness (mm)	11
Air-gap thickness (mm)	1	Magnet remanent flux density (T)	1

1.2 Effects of Stator MMF Space Harmonics on Candidate Design Performance

Because the stator MMF distributions of FSCW machines generally contain a rich set of spatial harmonics, the magnet eddy-current losses in modular PM machines are typically larger than those in conventional PM brushless ac machines. The torque in modular PM machines is produced by the interaction of a higher-order synchronous harmonic component with the permanent magnets. Harmonic component analysis of the phase winding functions was conducted to compare the spatial harmonics. In the comparison, a constraint was introduced requiring the same magnet flux-linkage in all of the candidate designs. With this constraint, the amplitude of the synchronous frequency component in Figs. 1–4 is the same for all of the candidate designs. As a result, all the machines produce the same torque when the windings are excited with a current that is inversely proportional to the number of phases.

1.3 FEA Validation of Machine Performance

Finite element analysis (FEA) was used to design the four candidate machines presented in Figs. 1–4 and to analyze their performance. Table 3 provides a summary of the key performance predictions for the candidate machines.

Figure 5(a) presents comparisons of the predicted phase back-EMF waveforms for all 4 machines operating at maximum speed (14,000 rpm), emphasizing the electromagnetic similarities of these four machines. The predicted average torque for these machines is plotted in Fig. 5(b) as a function of the phase current, with both variables plotted in per-unit to simplify the comparisons. All four machines begin to exhibit the effects of magnetic saturation at elevated phase current amplitudes between 1.5 and 2.0 pu, although the nonlinearity is mildest for the 3P machine. Finally, Fig. 5(c) compares the predicted torque ripple for the four machines during peak torque operation (i.e., 55 kW at 2800 rpm), demonstrating that the torque ripple is modest for all the machines (note the suppressed zero in the torque axis), with the highest ripple appearing in the 3P machine.

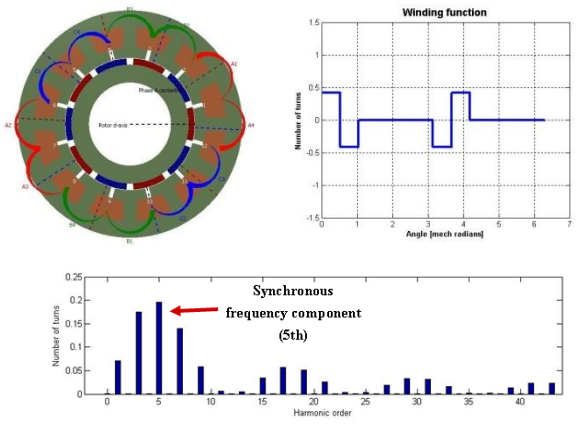


Fig. 1. Three phase (3P) machine: 12 slots/10 poles.

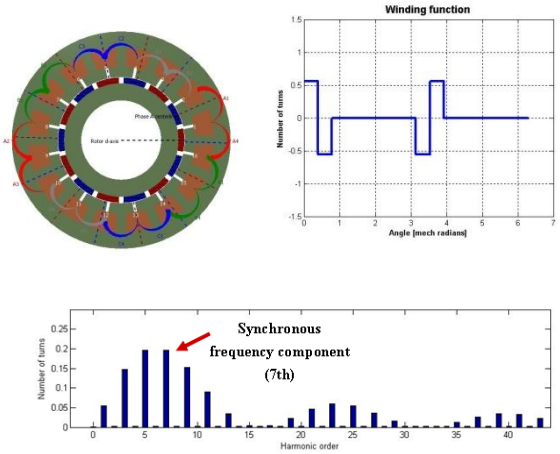


Fig. 2. Four phase (4P) machine: 16 slots/14 poles.

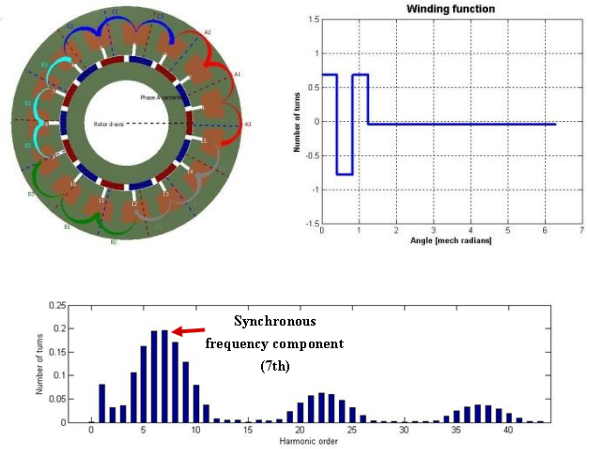


Fig. 3. Five phase (5P) machine: 15 slots/14 poles.

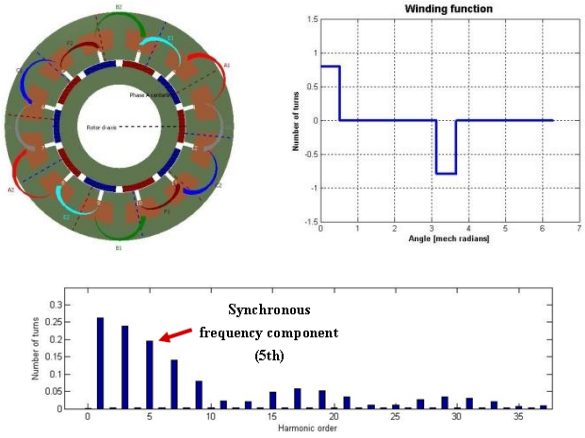
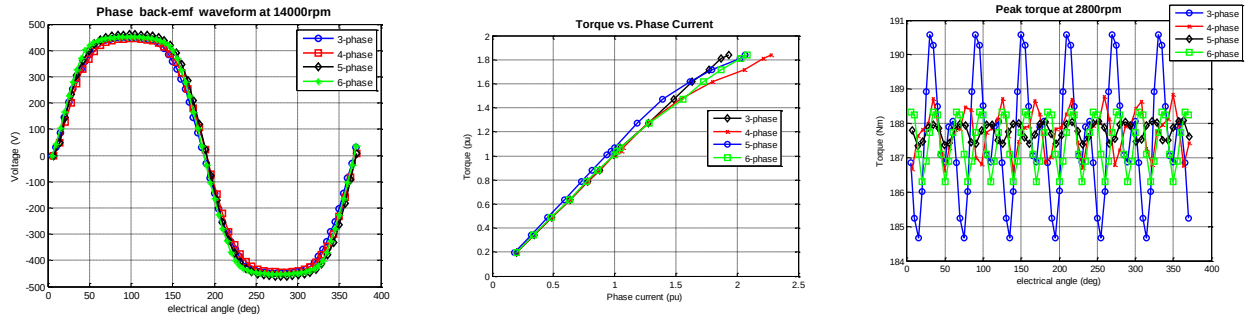


Fig. 4. Six phase (6P) machine: 2 slots/10 poles.

Table 3. Comparative Machine Performance Metrics

Feature	3 Phase	4 Phase	5 Phase	6 Phase
Series turns/phase	32	32	33	32
Rated current density @ A/mm^2	5.64	5.69	5.16	5.75
Peak current density @ A/mm^2	10.89	11.84	11	11.74
Rated current (A rms)	150	118	82.2	76.6
Phase back EMF @ 14,000 rpm (V_{peak})	458	455	460	458
Torque ripple @ peak power conditions (%)	5.9	2.0	0.7	2.3
Copper mass (kg)	6.8	7.8	10.4	13.6
Iron mass (kg)	19.1	18.3	18.1	19.2
Magnet mass (kg)	2.3	2.2	2.2	2.3
Total mass (kg)	28.2	28.3	30.7	35.1
Peak PM flux linkage (mWb)	71.5	53.8	43.4	35.9



(a) **(b)** **(c)**

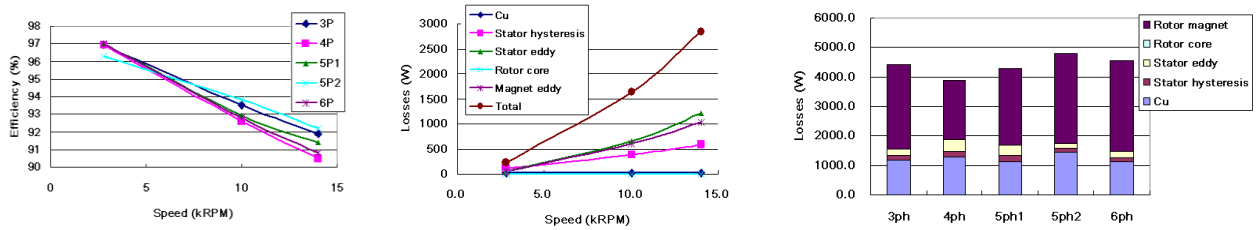
Fig. 5. (a) FEA-predicted phase back-EMF waveforms at 14,000 RPM; (b) predicted torque vs. phase current plot in per unit; and (c) predicted torque ripple during peak torque operation.

1.4 Soft Magnetic Composite Stator Core Replacement

The preliminary evaluation of soft magnetic composite (SMC) material was carried out in a non-optimal fashion. Instead of developing new machine designs tailored to the SMC material properties, the M19 material in the laminated-core designs was simply replaced with SMC material. The results of this material replacement exercise showed that the predicted average torque produced using the SMC core is 11% lower than that of the same machine with 0.35 mm-thick M19 laminations. In addition, the predicted core loss of the SMC core is higher than the loss of conventional laminated cores using M19 steel by 40 to 50% at maximum speed.

1.5 Predicted Machine Losses and Efficiency

The predicted efficiencies of the candidate machine designs with different phase numbers were evaluated at three operating points at speeds of 2,400, 10,000, and 14,000 RPM using sinusoidal current excitation. Figure 6(a) shows the predicted efficiency values vs. speed for partial load (20% of rated torque) conditions, exhibiting efficiency values that monotonically decrease from values in the vicinity of 90% at low speeds to values in the range of 91 to 92% at the maximum speed of 14,000 rpm. Figure 6(b) shows the corresponding loss breakdown for the 5P1 machine (note that 5P1 and 5P2 correspond to two 5P designs with different stator winding configurations), indicating that losses in the stator core and magnets increase with speed and dominate the losses at high speeds. Figure 6(c) provides more details about the predicted loss breakdown in the five machines under peak output power conditions (55 kW at 2800 rpm), indicating that magnet losses dominate under this condition.



(a) (b) (c)

Fig. 6. (a) Predicted efficiency at 20% rated torque vs. speed for machines with 3 to 6 phases; (b) predicted loss components of 5 phase machine vs. speed at 20% rated torque; and (c) predicted loss breakdowns at 55 kW and 2,800 rpm.

1.6 Results of Comparative Machine Evaluation

The results of the analytical machine study were carefully evaluated in order to select the most promising candidate machine for the 10 kW preliminary prototype drive planned for construction and testing in FY 2011. The selection is made more complicated by the fact that no single configuration emerged as being the best in every category, which requires considering engineering tradeoffs. After the evaluation process, the decision was made to select a variant of the 3P machine reconfigured with 6 phases instead of 3 as the preferred candidate for further development. As noted in Table 1, the 3P machine actually uses 6 separate phase modules, making it possible to operate this machine as a 6P unit if each module is treated as an independent phase module. Figure 1 shows that each of these 6 phases occupies a 60 degree arc along the stator periphery.

The major factors favoring the 3P (or 6P) machine over the other candidates for this application include its even GCD value of 2, which eliminates unbalanced magnetic pull on the rotor, lower machine mass, and lower fundamental frequency (1.16 kHz) at maximum speed that is critical to achieving high efficiency values at elevated speeds. Although its winding factor and LCM values are not the highest among the candidate machines, the overall evaluation of the 6P configuration gave it a net advantage over the other alternative machine configurations that ultimately led to its selection as the preferred topology for further development.

2. Fault-Tolerant IMMD Controller Development

Two alternative controller architectures that were evaluated and compared for the IMMD application are hierarchical and heterarchical controllers presented as block diagrams in Fig. 7. Of these two architectures, the hierarchical controller [Fig. 7(a)] represents the more familiar and conventional control configuration adopted in many machine drives. In this hierarchical controller, a master centralized controller is in charge of controlling the machine operation, interacting directly with the encoder (or resolver), IGBT gate drivers, current sensors, and user interface. Clearly, if the centralized controller fails, the whole system fails, making this hierarchical controller architecture a poor choice for fault tolerance.

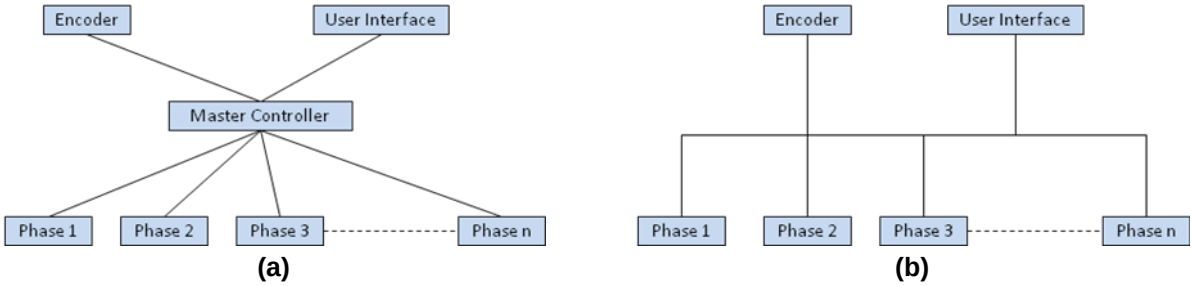


Fig. 7. Two alternative controller architectures for the IMMD: (a) basic hierarchical control architecture and (b) basic heterarchical control architecture

In the alternative heterarchical controller [Fig. 7(b)], each phase module has its own dedicated controller. All of the phase controllers are connected to each other as well as to the drive sensors (i.e., rotor position sensor and current sensors) and user interface via a digital network. In contrast to a master-slave configuration, the individual controllers in the heterarchical architecture operate in parallel as independent peers, with each controller having control of only its own associated module. If one of these controllers fails, all of the *n-1* remaining phase module controllers are able to continue operating.

A block diagram using this type of controller configuration to implement field-oriented control for a 5P IMMD is shown in Fig. 8. Although shown for a 5P machine, this configuration can be generalized to control an *n*-phase machine in the same manner.

The incremental encoder will have its A, B, and index pulse pins connected to the on-chip quadrature encoder module in each controller by means of a 3 wire digital bus. The individual phase current readings are available to each modular controller through an *n*-wire analog bus, and each modular controller's on-chip A/D converter will have real-time information from all of the phase current sensors available through this analog bus. An on-chip UART or CAN module will be used to connect each controller to the user interface and to exchange other information among the phase module controllers. Although not shown in Fig. 8, a ring topology could be adopted for the digital network.

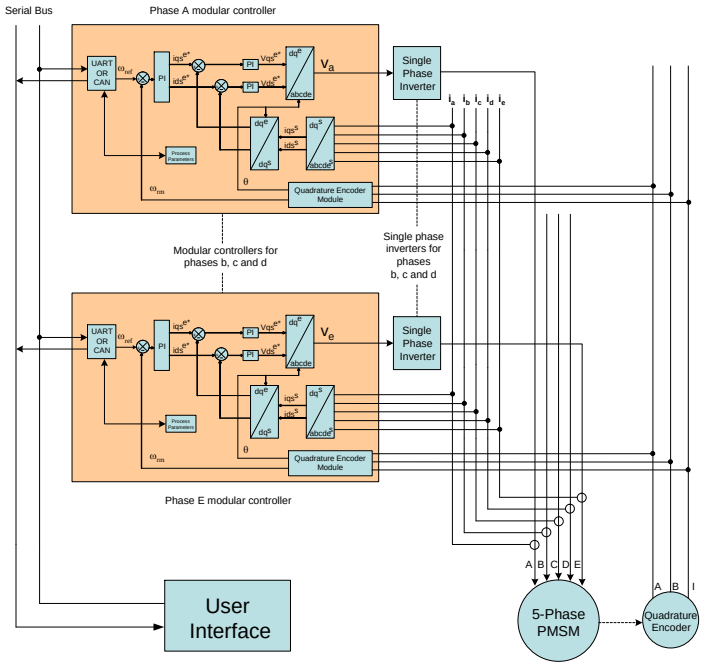


Fig. 8. Heterarchical controller implementation for field-oriented control of a 5 phase IMMD.

Controller/DSP Selection for IMMD Fault-Tolerant Control

A variety of 16 and 32 bit microcontrollers offered by leading semiconductor manufacturers were reviewed for the IMMD application. After careful consideration, the Texas Instruments Piccolo 32 bit TMS320F28035 microcontroller was selected as the best candidate for this project.

3. Si IGBT Operation at 200°C

IMMD offers a promising new approach for integrating motor drive power electronics into the machine housing in a modular fashion. To be integrated into the machine housing, the power electronics need to work in ambient temperatures up to 150°C. For low cost, it is desirable to use Si devices. Given that the current commercial Si devices usually have a maximum junction temperature rating of 150°C, with some devices rated at 175°C, it is desirable to investigate the possibility to push the Si device junction temperature to 200°C with increased loss-handling capability and higher power density. [9]

An IGBT with soft, fast recovery antiparallel diode from Infineon (IKW40N120H3) is selected for characterization and thermal study of IGBT operating at high temperatures (Fig. 9). Table 4 shows the basic parameters in the datasheet. The main issues with Si device operating beyond 150°C to 200°C include excessive loss and possible thermal runaway due to excessive leakage current, the change of the safe operating area boundaries due to the decreased latching current and second breakdown, and corresponding long-term reliability issues. [10] In this report, IGBT is investigated in terms of static and switching characteristics, device losses, and thermal limits.

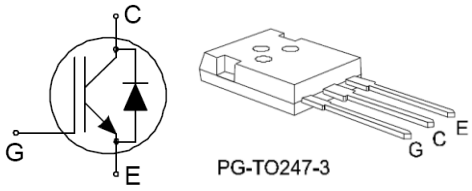


Fig. 9. IKW40N120H3-Si IGBT with antiparallel diode.

Table 4. Specifications of IKW40N120H3

Type	V_{CE}	I_C	V_{CEsat}, T_{vj}=25°C	T_{vjmax}	Package
IKW40N120H3	1200V	40A	2.05V	175°C	PG-TO247-3

3.1 IGBT Static Characteristics

Figure 10 shows the static characterization setup. Figure 11 shows the IGBT output characteristics at 200°C. RCE(on) represents the on-state resistance and VT0 represents the threshold voltage, both significant parameters for conduction loss. Table 5 shows the parameters of IGBT output characteristics at different temperatures. As the temperature rises, the on-state resistance increases because of mobility reduction while the threshold voltage decreases. As a result, the conduction loss has a positive temperature coefficient when Ic is large.

Fig. 10. Static characterization setup with curve tracer.

Table 5. Parameters of IGBT Output Characteristics at Different Temperatures

	25°C	100°C	175°C	200°C
V_{T0}	1V	0.9V	0.8V	0.7V
$R_{CE(on)}$	0.026Ω	0.037 Ω	0.049 Ω	0.052 Ω

For the loss calculation, the leakage current is measured when 650 V is applied to the collector and emitter of device under test (DUT). Figure 12 shows the IGBT leakage current as a function of junction temperature. At high temperatures, especially above 175°C, the leakage current increases rapidly (double every 5 degrees), which contributes to the total loss and might cause thermal runaway.

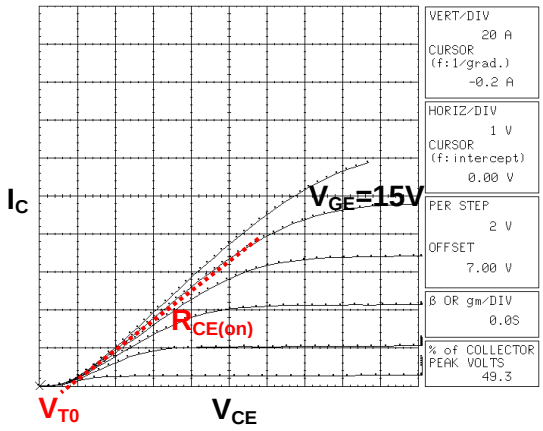


Fig. 11. IGBT output characteristics at 200°C.

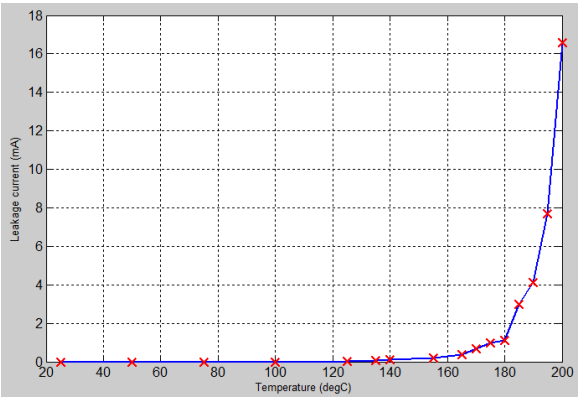


Fig. 12. IGBT leakage current at 650 V as a function of junction temperature.

3.2 IGBT Switching Characteristics

The inductive-load double pulse tester was built to test the switching characteristics of Si IGBT. Figure 13 shows the circuit schematic of double pulse test (DPT) with overcurrent protection. The double pulse is generated by Agilent 33220 arbitrary waveform generator. The DUT is driven by a high speed, high current gate driver IXDD414 from IXYS, with gate voltage from 0 V to 15 V.

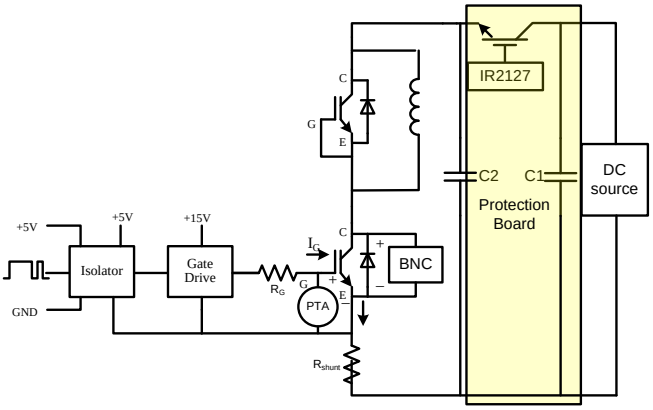


Fig. 13. High temperature experiment setup for switching characteristics test.

To measure the switching characteristics of IGBT at high temperatures, DUTs are connected to the hot plate through the copper connector, as shown in Fig. 14. The glass wool and fan are used to keep the PCB board (especially for shunt resistors and gate drivers) under 50°C. Thermal couples are used to monitor and adjust the temperature of DUT case and PCB. Since the switching loss caused by two pulses is negligible, it is assumed that DUT junction temperature is the same as the case temperature. Figure 15 shows the hardware testbed for high temperature switching experiments.

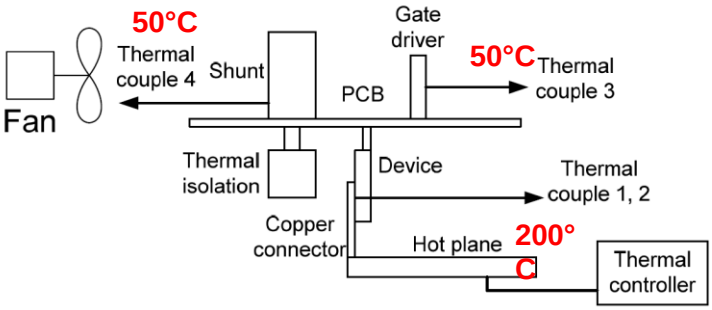


Fig. 14. High temperature experiment setup for switching characteristics test.

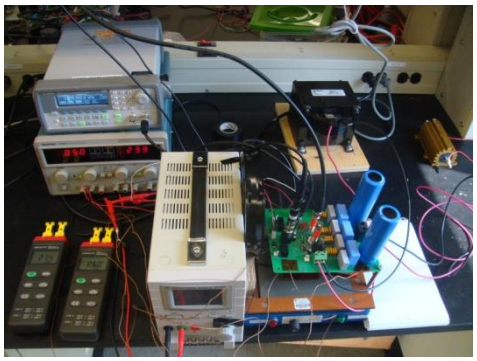


Fig. 15. Hardware testbed for high temperature switching experiments.

With the DPT hardware testbed, the IGBT switching characteristics are tested at 25°C, 100°C, 175°C, and 200°C. The test conditions are: VCC=650 V, IC=40 A, VGE=0.0 V/15.0 V, RG=10.0 Ω. Figure 16 shows the DPT waveforms of IGBT at 200°C.

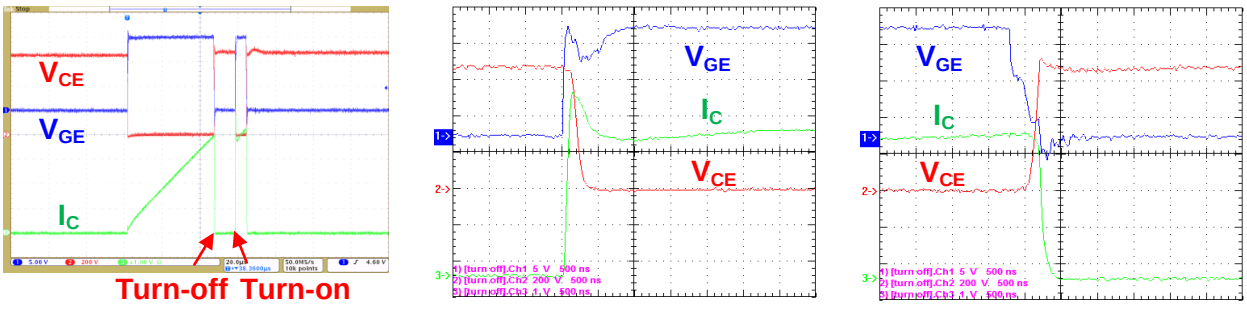


Fig. 16. Waveforms of IGBT switching characteristics at 200°C: (a) double-pulse waveforms, (b) turn on transient, and (c) turn off transient.

Based on the switching waveforms, the parameters of IGBT switching characteristics at different temperatures are calculated and shown in Table 6. The experimental parameters at 25°C and 175°C are very close to that in the datasheet. Both the switching time and switching energy increase as the temperature goes up.

Table 6. IGBT Switching Parameters at Different Temperatures

Parameter	25°C	100°C	175°C	200°C
Turn on delay time $t_{d(on)}$	24.4ns	21ns	23.6ns	20ns
Rise time t_r	60.4ns	62.6ns	78.4ns	80ns
Turn off delay time $t_{d(off)}$	278ns	311.2ns	380ns	400ns
Fall time t_f	38.8ns	79.2ns	120ns	140ns
Turn-on energy E_{off}	3.19mJ	3.99mJ	4.50mJ	4.61mJ
Turn-off energy E_{off}	1.31mJ	2.05mJ	2.83mJ	3.02mJ
Total switching energy E_{ts}	4.50mJ	6.04mJ	7.33mJ	7.63mJ

3.3 Power Losses and Thermal Analysis

To calculate the motor drive losses based on the device characteristics, the specifications of the system are assumed in Table 7.

Table 7. System Specifications

Power rating (for 1 phase leg)	P_B=10 kW	**DC link voltage**	V_{dc}=650 V
Nominal voltage (l-n rms)	V_B=217 V	**Modulation index**	M=0.994
Nominal current (rms)	I_B = 46 A	**Modulation scheme**	Continuous space vector modulation (SVM)

The total loss generated from power devices consists of conduction loss, switching loss, and leakage current loss. In our case, the diode reverse recovery loss is neglected since it is very small. Table 8 and Fig. 17 show the total losses in one phase leg, which increase with temperature.

Table 8. Power Losses in One Phase Leg at Different Temperatures (f_s=5kHz)

(Unit: W)	25°C	100°C	175°C	200°C
IGBT conduction loss	91.66	110.31	131.0	133.28
IGBT switching loss	23.34	31.3	38	39.6
Leakage current loss	0	0	0.65	10.8
Diode conduction loss	3.07	3.22	3.28	3.31
Total loss	118.07	144.86	172.95	186.95
Efficiency (%)	98.82	98.55	98.27	98.13

The device is cooled by the water-ethylene-glycol (WEG) coolant at 105°C. Keeping the junction temperature below 200°C requires a certain thermal transfer ability, which is represented by thermal resistance and depends on the semiconductor material and packaging. Figure 18 shows the temperature curve with the power dissipation line. The rate of the thermal load line is thermal conductance. The cross point of the thermal load line and the zero loss line is the coolant temperature. From Figure 18, the thermal resistance from junction to ambient of IGBT should be no more than 1.04 K/W if the switching frequency is 5 kHz, which provides the baseline for packaging design. Some failures were observed during DPT at 200°C, and the ruggedness of the devices needs further evaluations.

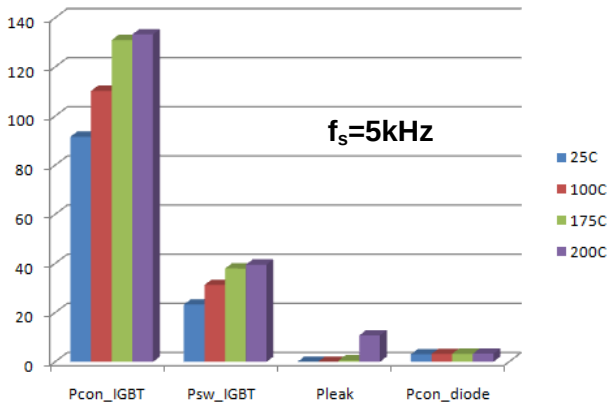


Figure 17. Power losses in one phase leg at different temperatures (f_s=5kHz).

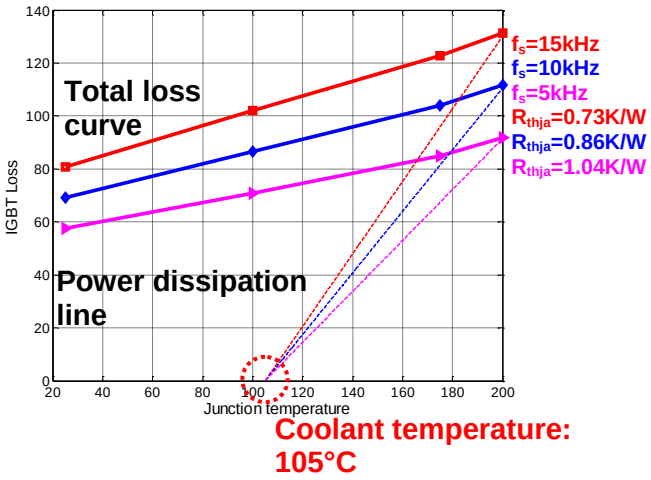


Figure 18. IGBT power losses and thermal analysis at different frequencies.

4. Device Packaging and Cooling

Wire-bonding technology is adopted for the baseline design of the 10 kW phase-leg power module, as shown in Fig. 19. Meanwhile, Table 9 lists the detailed materials selection and the corresponding dimensions. Two Si IGBT and two diode dies from Infineon, with maximum ratings of 1,200 V/50 A/175°C, are selected. To enhance reliability, copper lead frame is used as connection terminal instead of pole connection. Solder Au80Sn20 is used as the die attachment, with an optimized thickness of 200 μm. Essentially, this package is a conventional design [11].

Hence, the baseplate and case are also included, as shown in Fig. 19(c). Note that in future applications we may remove the baseplate to directly connect the substrate to the heatsink to achieve smaller thermal resistance.

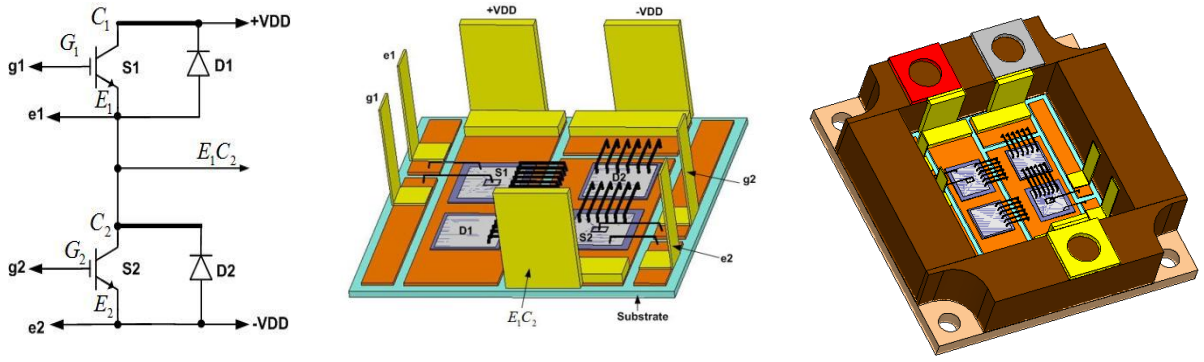


Fig. 19. Baseline design of a 10 kW phase-leg power module: (a) phase-leg schematic, (b) layout design, and (c) power module design.

Thermal resistance of each device from junction to case is of importance for cooling system design because the maximum junction temperature of each device should not exceed 200°C [12]. An FEA simulation tool, Comsol Multiphysics, was used to characterize the thermal performance of the proposed package. Table 10 lists the thermal conductivity values used in the simulation.

Table 9. Materials Selection

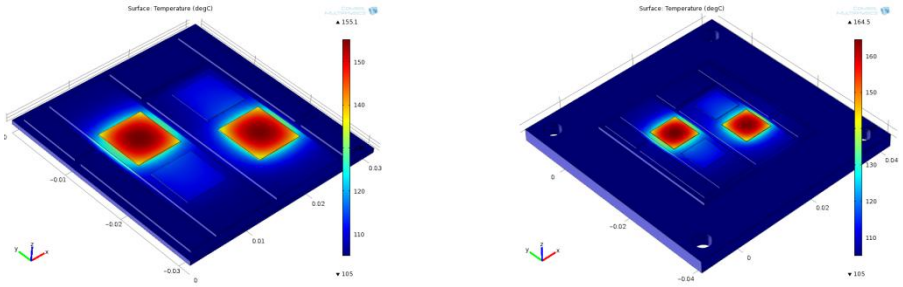
Component	Dimensions (mm)
IGC50T120T6RL	
Emitter pad	7.25 × 6.84 × 0.115
Gate pad	5.36 × 5.74 × 0.004
SIDC42D120F6	1.31 × 0.81 × 0.004
Anode pad	6.5 × 6.5 × 0.12
Substrate	5.78 × 5.78 × 0.004
	30.6 × 30 × (Cu: 0.3, Ceramic: 0.635)
Aluminum wires	Gate pad 5 mils, others 10 mils × 6
Bus	Copper: 1 × 7 × 9
Lead	Copper: 0.2 × 3 × 9
Die attachment	Au80Sn20: thickness 0.2
Base	Copper: 52 × 53 × 3
Encapsulant	Silicone gel
Case	Torlon 5030

Table 10. Thermal Conductivities

Material	Thermal Conductivity W/(m°C)
Al_2O_3	24
Cu	393
Al	237
Au80Sn20	50
Si	90

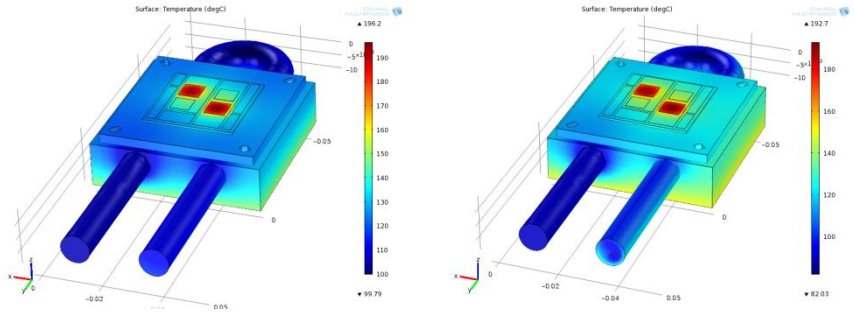
Figure 20 shows the thermal performances of the packaging design without and with baseplate when the modulation index of the inverter is 1.0. As can be seen, the use of the baseplate and the solder layer between substrate and baseplate increase the temperature rise of IGBT about 9.4°C. Here, the IGBT has the largest power loss, and the diode has the smallest loss, hence the temperature rise of the IGBT is the largest.

Thermal management system is another key challenge in motor drive. At present, the inverter and motor use different cooling loops and coolants. Specifically, for inverter cooling, an individual 65°C WEG cooling loop is used, whereas transmission oil circulation with a WEG heat exchanger is used for motor cooling. Our objective is to use one liquid cooling loop and one coolant to cool the inverter and motor together. Figure 21 shows the thermal performance of the packaging design with liquid cooling for two different coolants. In comparison with Figs. 15(a) and 15(b), the junction temperature of the IGBT for the transmission oil (192.7°C) is a little lower than that for WEG (196.2°C). Although the transmission oil has larger dynamic viscosity, the cooling performance of the transmission oil is acceptable in our design due to its lower inlet temperature. Therefore, to further improve the thermal performance of the whole system, we can optimize the packaging design in terms of: (1) selecting high thermal conductivity substrate (e.g., AlN), (2) removing the baseplate, (3) using solder instead of thermal interface material, and (4) designing a more powerful cooling structure (e.g., pin-fin heatsink).



(a) **(b)**

Fig. 20. Thermal performance of the package when IGBT loss is 90 W and diode loss is 10 W. Without baseplate (a), the temperature rise is 50.1°C. With baseplate (b), the temperature rise is 59.5°C.



(a) **(b)**

Fig. 21. Thermal performance of the packaging design with liquid cooling: (a) WEG coolant with inlet temperature 105°C and (b) transmission oil coolant with inlet temperature 90°C.

Conclusion

Significant progress has been made during the first year of this project towards identifying the most promising machine and controller architectures for inclusion in the integrated traction drive system. A variety of fractional-slot concentrated-winding PM machine configuration with 3 to 6 stator phases were evaluated and compared to determine their suitability for this special drive application. After considering all of the engineering tradeoffs, a 6P variant of a 3P, 12 slot, 10 pole machine has been identified as the candidate machine demonstrating the highest potential for achieving the demanding performance objectives of the integrated traction drive system. Also, alternative controller architectures for the integrated traction drive have been evaluated and compared. A heterarchical control architecture is identified as the most promising configuration for achieving the desired high levels of fault tolerance. According to this preferred architecture, the *n-1* healthy controllers are unaffected by the loss of any one of the controllers, providing the basis for a robust control of the integrated traction drive.

The static and switching characteristics of selected Si device have been tested with a hardware testbed built specifically for device characterization at high temperature. The results show that the loss and leakage current at 200°C are acceptable. However, the ruggedness of such devices at 200°C requires further evaluation. Based on the losses and thermal study, an Si-device-based 10 kW phase-leg packaging design together with a 2-pass tube coldplate is proposed. Detailed thermal performance characterization has been conducted for different packaging structures, operating conditions, and coolant selections. The proposed packaging design and cooling approach can maintain the Si IGBT junction temperature below 200°C with the ambient temperature of 150°C.

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