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DEVELOPMENT OF A NOVEL BI-DIRECTIONAL ISOLATED MULTIPLE-INPUT DC-DC CONVERTER

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DEVELOPMENT OF A NOVEL BI-DIRECTIONAL ISOLATED MULTIPLE-INPUT DC-DC CONVERTER

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ACRONYMS

BU	battery-storage unit
dc	direct current
DSP	digital-signal processor
ESL	estimated-series resistance
ESR	estimated-series inductance
EV	electric vehicle
FC	fuel cell
HEV	hybrid electric vehicle
HVS	high-voltage side
IGBT	insulated gate bipolar transistor
LVS	low-voltage side
MOSFET	metal oxide semiconductor field-effect transistor
rms	root-mean square
UC	ultracapacitor
ZVS	zero-voltage switching

1. INTRODUCTION

1.1 BACKGROUND

There is vital need for a compact, lightweight, and efficient energy-storage system that is both affordable and has an acceptable cycle life for the large-scale production of electric vehicles (EVs) and hybrid electric vehicles (HEVs).

Most of the current research employs a battery-storage unit (BU) combined with a fuel cell (FC) stack in order to achieve the operating voltage-current point of maximum efficiency for the FC system. A system block diagram is shown in Fig.1.1. In such a conventional arrangement, the battery is sized to deliver the difference between the energy required by the traction drive and the energy supplied by the FC system. Energy requirements can increase depending on the drive cycle over which the vehicle is expected to operate. Peak-power transients result in an increase of losses and elevated temperatures which result in a decrease in the lifetime of the battery.
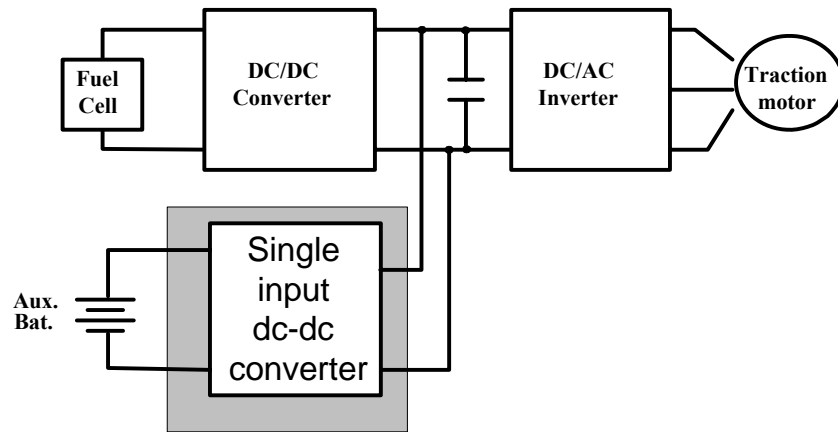
Fig. 1.1. Block diagram of a FC–BU system.

This research will propose a novel two-input direct current (dc) dc to dc converter to interface an additional energy-storage element, an ultracapacitor (UC), which is shown in Fig.1.2. It will assist the battery during transients to reduce the peak-power requirements of the battery.
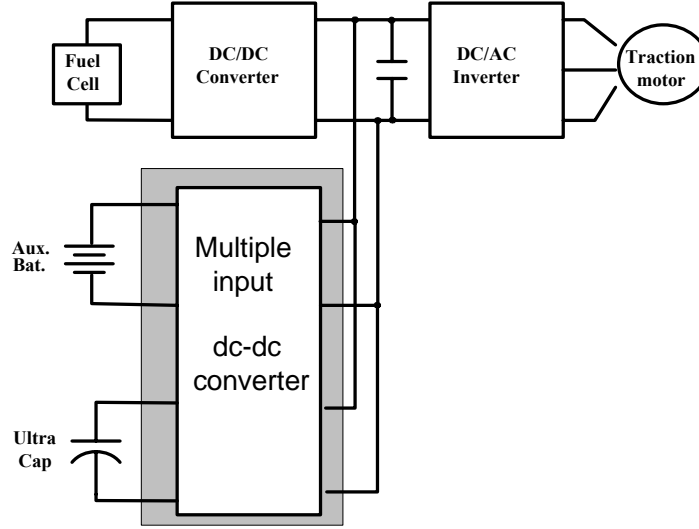
Fig. 1.2. Block diagram of a FC–BU–UC system using a multiple-input dc-dc converter.

1.2 SYSTEM SPECIFICATIONS

Specifications of the two-input bi-directional dc-dc converter (Fig. 1.3) are as follows:

- The nominal voltage at the low-voltage side (LVS) of one input is 12 V, and another input is 16 V. These values can vary from 8–16 V and 12–20 V during charging and discharging.
- The nominal high-side voltage is 288 V, with an operating range from 255–425V.
- Nominal discharging power of the two inputs is 2 kW and 3.5 kW, respectively.
- The nominal output power is 5 kW.
- Bus capacitance C_o is less than 2000 μF.
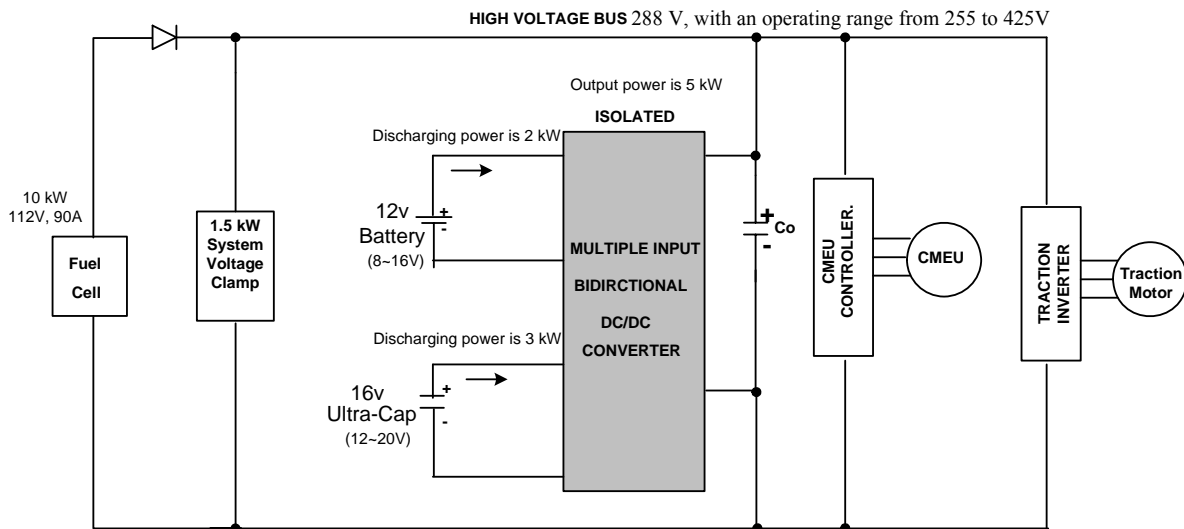
Fig. 1.3. Systematic diagram.

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2. POWER-STAGE TOPOLOGY SELECTION

2.1 MULTIPLE-INPUT DC-DC CONVERTER TOPOLOGIES REVIEW

The current research of multiple-input dc-dc converters is mainly focused on the uni-directional circuit topology for applications in a distributed energy system. There are two types of converter architectures that have been proposed. The first is to put different dc sources in series to implement the multiple-input dc-dc converter [1–2]. Another circuit is to put dc sources in parallel by using the coupled transformer [3–4] or multi-winding transformer as shown in Fig. 2.1 [5]. The common problem with these converters is that power is only allowed to flow in one direction, which is impractical for vehicle application where power needs to flow in either direction.
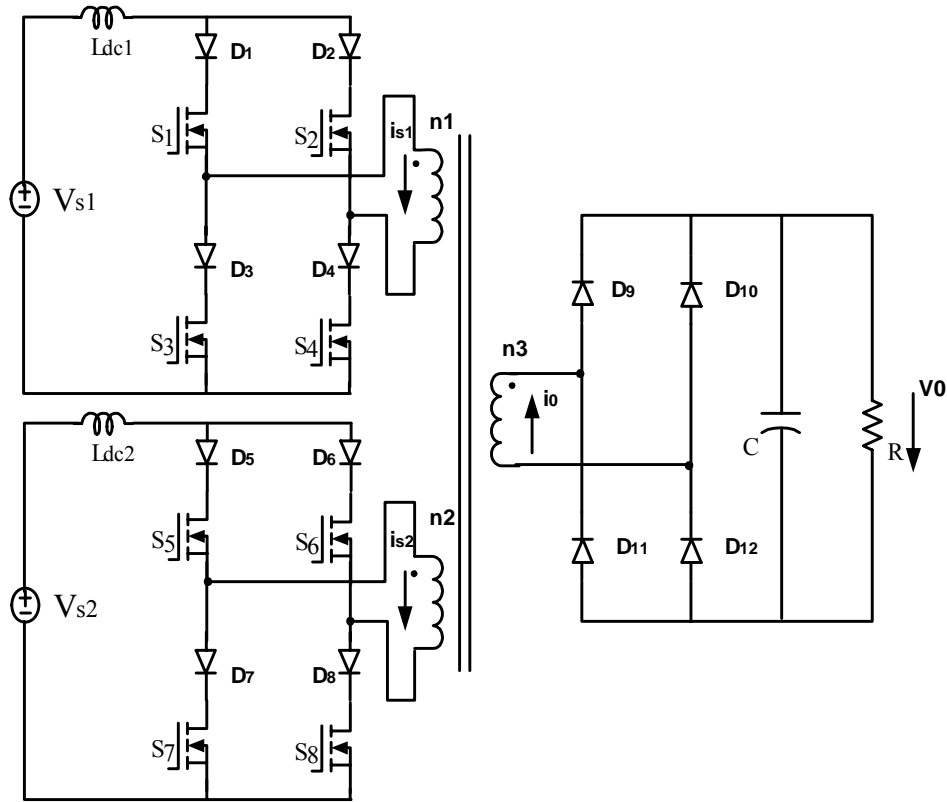
Fig. 2.1. Reported uni-directional multiple-input dc-dc converters by using multiwinding transformer [5].

Recently, a non-isolated bi-directional multiple-input dc-dc converter has been proposed for HEV applications as shown in Fig. 2.2 [6]. However, this circuit has several disadvantages. First, it lacks electric isolation. Second, it requires high-voltage BU and UC tanks. Limitations to the use of UC tanks are primarily due to the UCs low-cell voltage at their present stage of development, as well as cell-leakage current that may result in voltage imbalances in a stacked unit. This problem becomes worse for high-voltage UC tanks. In addition, high-voltage BUs and UCs will ultimately increase the cost and weight of the energy system.

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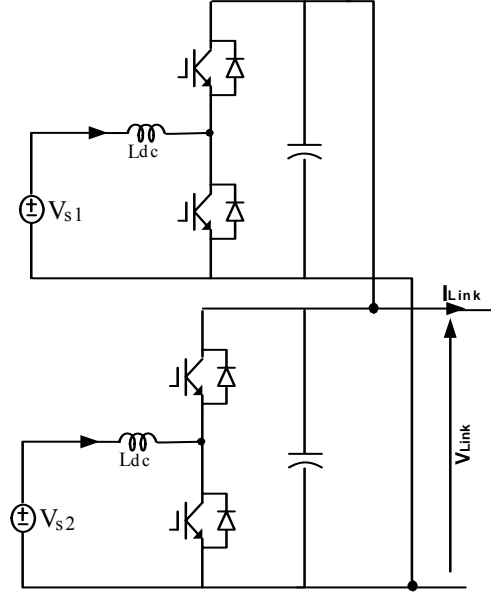
Fig. 2.2. Reported non-isolated bi-directional multiple-input dc-dc converters [6].

2.2 PROPOSED TWO-INPUT DC-DC CONVERTER

Figure 2.3 shows the proposed two-input zero-voltage switching (ZVS) isolated bi-directional dc-dc converter. It is an extension of a single-input dual half-bridge topology [7].
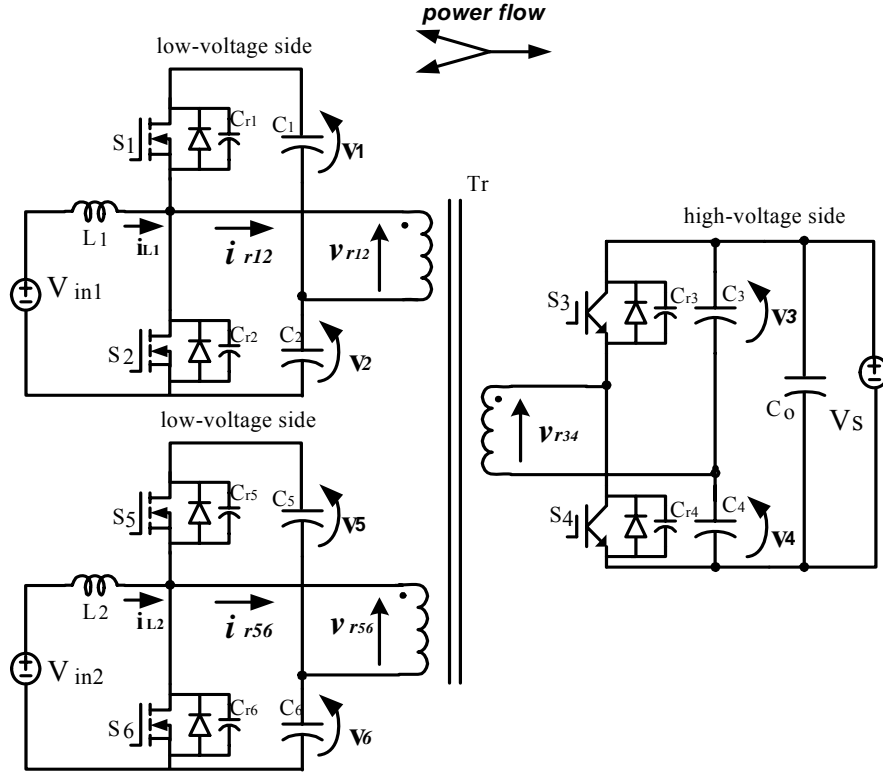
Fig. 2.3. Proposed two-input ZVS isolated bi-directional dc-dc converter.

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The proposed topology has the following innovations:

- Electrical isolation can be achieved naturally.
- Magnitude of dc input voltages may be low and either similar or dissimilar.
- DC sources can deliver power individually, simultaneously, and bi-directionally.
- The soft-switching technology is achievable across a wide operating range.
- Minimum number of devices and simple control.
- High efficiency, lightweight, and high-power.

In addition, the combined storage unit (UC and battery) interfaced with this converter can increase the life cycle of energy-storage elements and reduce the cost of EVs.

3. OPERATION PRINCIPLE

3.1 INTRODUCTION

Figure 3.1 illustrates the "Δ" type and "Y" type circuit model of a three-winding transformer. The primary-referred equivalent circuit based on the "Y" type transformer model is redrawn in Fig. 3.2. The circuit consists of two current-source input-stage circuits, a three-winding coupled transformer, and a common output-stage circuit. This converter can be applied in FC vehicles to connect three ports: 12V to approximately 42V battery, UC bank, and the load. The load will be connected to a traction-motor drive through an inverter and the dc-bus voltage of a high-voltage side (HVS) that can reach from 288 V to approximately 400 V. The transformer here has three functions: (1) combine input dc sources in magnetic form; (2) provide electrical isolation; and (3) step-up voltage from the LVS to the HVS.

When power flows from the LVS to the HVS, the circuit works in boost mode to keep the HVS at a desired high value which can be referred to as the acceleration mode in FC vehicle applications. In the other direction of power flow, the circuit works in buck mode to recharge the energy-storage elements from the FC or from absorbed regenerative energy which corresponds to cruise and braking modes respectively. In this section, the power-stage description and operation-principle analysis will be described for both the boost and buck mode respectively.

$$Ir12 = Ir13 + Ir15 \qquad Lr13 = (Lr12*Lr34 + Lr34*Lr56 + Lr56*Lr12)/Lr56$$
$$Ir56 = Ir53 - Ir15 \qquad Lr15 = (Lr12*Lr34 + Lr34*Lr56 + Lr56*Lr12)/Lr34$$
$$Ir34 = Ir13 + Ir53 \qquad Lr53 = (Lr12*Lr34 + Lr34*Lr56 + Lr56*Lr12)/Lr12$$
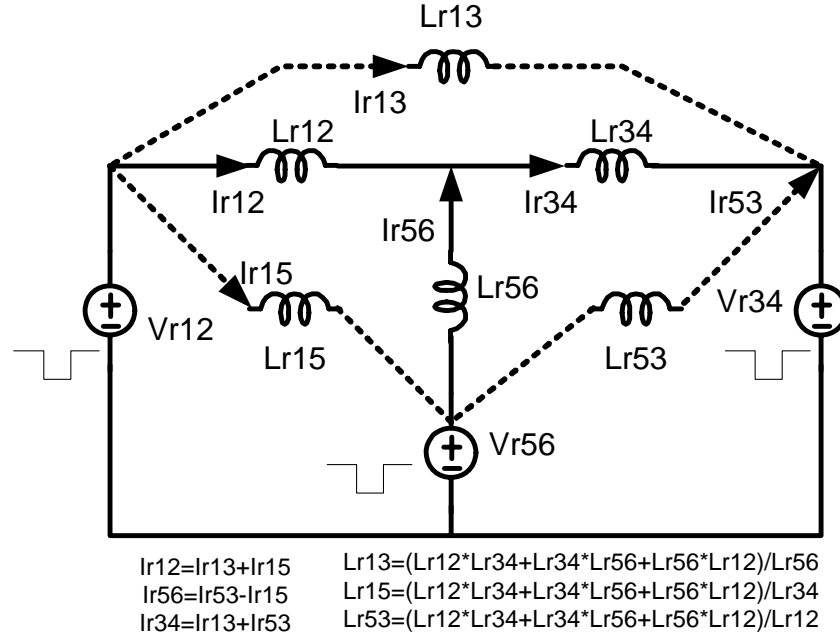
Fig. 3.1. Circuit model of a three-winding transformer including "Δ" type and "Y" type model.
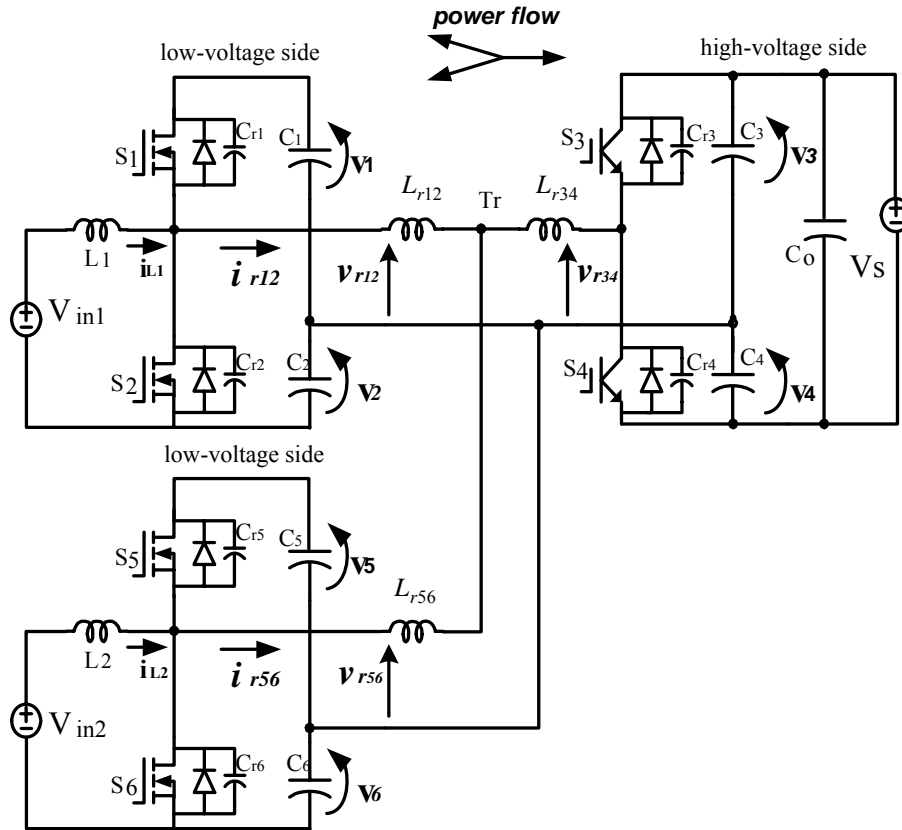
Fig. 3.2. Primary-referred equivalent circuit based on " Y " transformer model.

3.2 SOFT-SWITCHING OPERATION IN BOOST MODE

Figure 3.3 illustrates the key waveforms in boost mode where the energy is transferred from each of the LVS to the HVS. Each LVS generates a square-wave voltage (v_{r12} and v_{r56}) on the primary side of the transformer. The HVS half-bridge generates a square-wave voltage (v_{r34}) on the secondary side of the transformer. The amount of power transferred is related to the phase-shift of square-wave voltages. The current waveforms in Fig. 3.3 are plotted depending on the phase-shift and voltage relationship. The interval t_0 to t_{20} of Fig. 3.3 describes the various stages of operation during one switching period in boost mode. The converter operation is repetitive in the switching cycle. One complete switching cycle is divided into 20 steps. To aid in understanding each step, a set of corresponding annotated circuit diagrams is given in Fig. 3.4 with a brief description of each step.
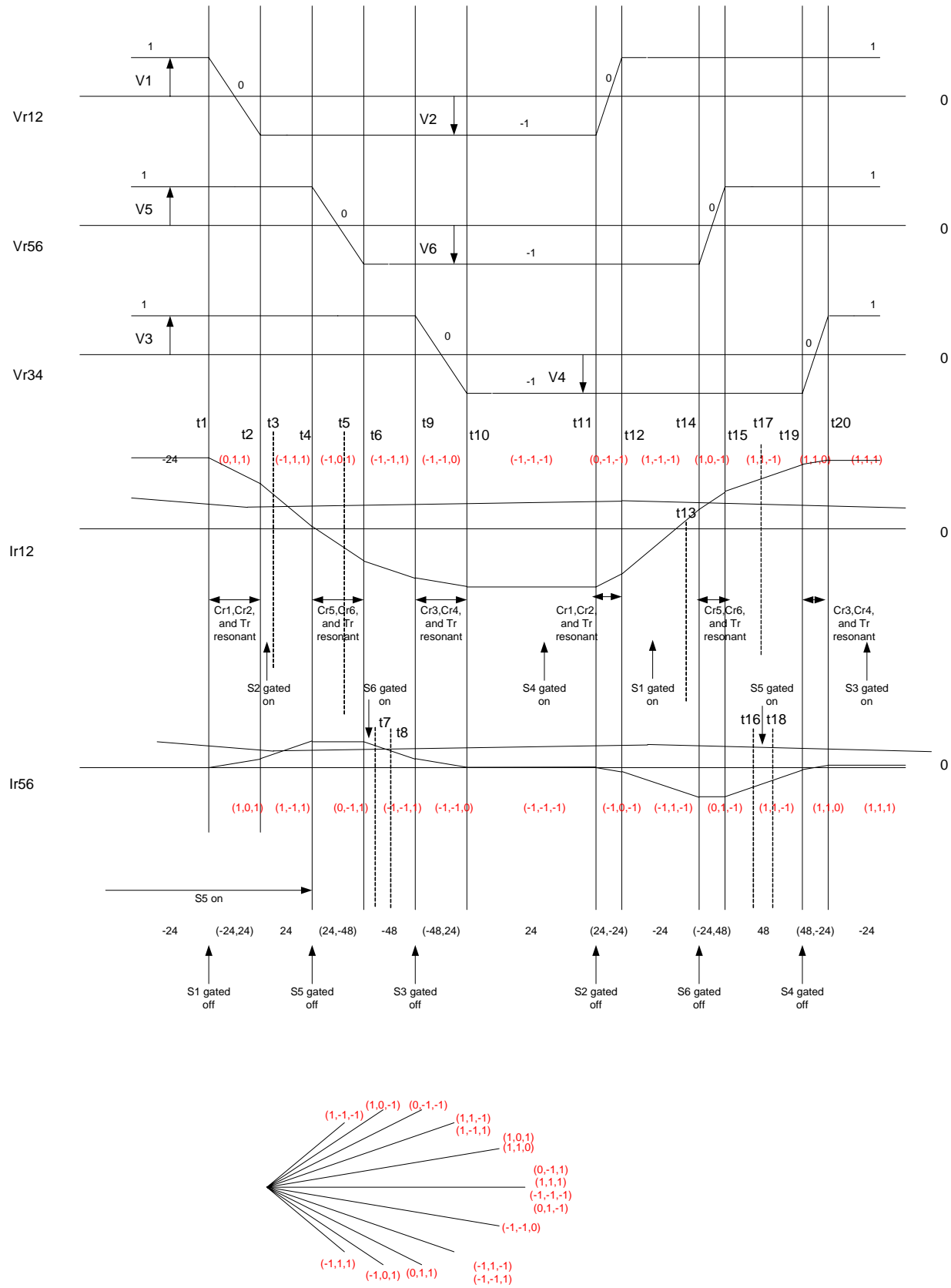
Fig. 3.3. Waveforms and switching timing of a boost mode.

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(a)   Before t1   Initial state

(b)   t1 - t2   Open S1 and resonant start   IL2 intend to increase

(c)   t2-t3   Resonant stoped, D2 intend to conduct Vcr1=V12, Vcr2=0, S2 is ready to turn on   IL2 increasing

(d)   t3-t4   IL1>Ir12, S2 turned on and take over current   IL2 still increasing

(e)   t4-t5   IL1>Ir12, S2 turned on and take over current, ir12 continue decreasing   Resonant start

(f)   t5-t6   Ir12 cross below zero, S3 open to take current   Resonant continue

Fig. 3.4. Communication step diagrams during a switching cycle in boost mode.

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(g)   t6-t7

Resonant stop, D6
intend to conduct, S6 is
ready to turn on

Ir12 continue to increase

(h)   t7-t8

Ir12 continue to increase

IL2>Ir34, S6 turned on and take over
current, ir34 continue decreasing

(g)   t6-t7

Resonant stop, D6
intend to conduct, S6 is
ready to turn on

Ir12 continue to increase

(h)   t7-t8

Ir12 continue to increase

IL2>Ir34, S6 turned on and take over
current, ir34 continue decreasing

(k)   t10-t11

Ir34 decrease

D4 conduct , Ir12 decrease

(l)   t11-t12

S2 turned off, Cr1 and Cr2
resonant start

Ir34 increase

Fig. 3.4. Communication step diagrams during a switching cycle in boost mode (cont'd).

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(m) t12-t13

Resonant stoped, D1 conduct , Ir12 continue decrease, S1 is ready to turn on

Ir34 increase

(n) t13-t14

Ir12 cross below zero, S4 conduct to take current

Ir34 continue increasing

(0) t14-t15

S6 turned off, Cr5 and Cr6 start to resonant

Ir12 continue to increase

(p) t15-t16

Ir12 continue to increase

Resonant complete, D5 conduct, S5 is ready to turn on

(q) t16-t17

Ir12 continue to increase

Ir34 increase above zero

(r) t17-t18

IL1<Ir12, S1 turned on and take over current

Ir34 increase above zero

Fig. 3.4. Communication step diagrams during a switching cycle in boost mode (cont'd).

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Fig. 3.4. Communication step diagrams during a switching cycle in boost mode (cont'd).

3.3 SOFT-SWITCHING OPERATION IN BUCK MODE

Because the half-bridge topology of the two sides is symmetrical, the soft-switching operation principles in buck mode are similar to those in boost mode. Figure 3.5 describes one switching cycle in buck mode. Due to the reversed power-flow direction, the phase of V_{r34} is leading V_{r12} and V_{r56}. The buck-mode operation can be divided into 20 steps. To aid in understanding each step, a set of corresponding annotated circuit diagrams is given in Fig. 3.6; however, the description of each step can be analogously inferred and will not be discussed here.
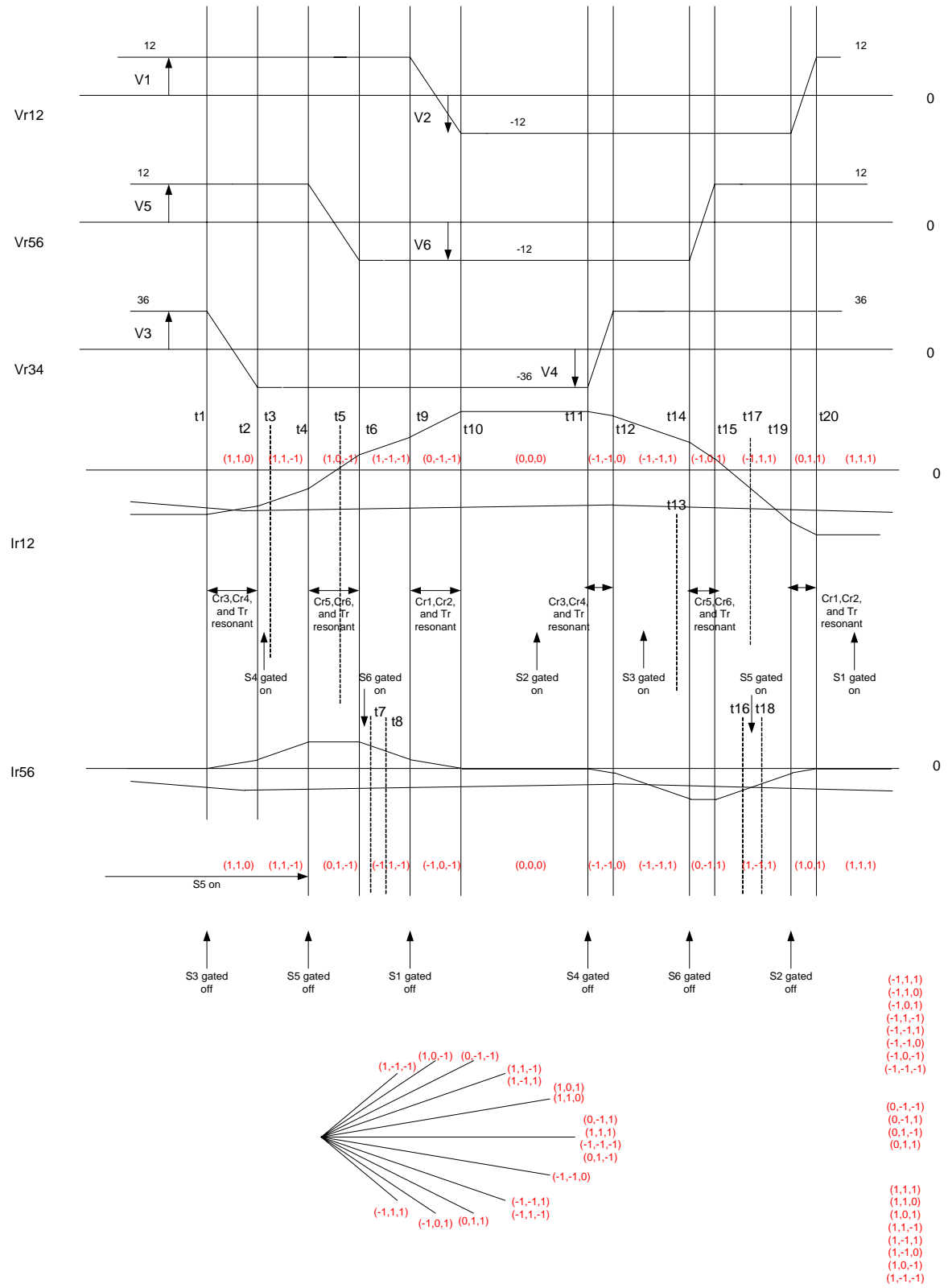
Fig. 3.5. Waveforms and switching timing of buck mode.

(a)

(b)

Open S3 and resonant start

t1 - t2

IL2 intend to increase

(c)

Resonant stoped, D2 intend to conduct Vcr1=V12, Vcr2=0, S2 is ready to turn on

IL2 increasing

(d)

IL1>Ir12, S2 turned on and take over current

IL2 still increasing

t3-t4

(e)

IL1>Ir12, S2 turned on and take over current, ir12 continue decreasing

Resonant start

t4-t5

(f)

Ir12 cross below zero, S3 open to take current

t5-t6

Resonant continue

Fig. 3.6. Communication step diagrams during a switching cycle in buck mode.

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Fig. 3.6. Communication step diagrams during a switching cycle in buck mode (cont'd).

Resonant stoped, D1
conduct , Ir12 continue
decrease, S1 is ready
to turn on   (m)

t12-t13

Ir34 increase

t13-t14

(n)

Ir12 cross below zero, S4
conduct to take current

Ir34 continue increasing

Ir12 continue to increase

(o)

S6 turned off, Cr5 and Cr6
start to resonant

t14-t15

Ir12 continue to increase

(p)

Resonant complete, D5
conduct, S5 is ready to turn on

t15-t16

Ir12 continue to increase

(q)

Ir34 increase above zero

t16-t17

IL1<Ir12, S1 turned on
and take over current

(q)

Ir34 increase above zero

t17-t18

Fig. 3.6. Communication step diagrams during a switching cycle in buck mode (cont'd).

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Fig. 3.6. Communication step diagrams during a switching cycle in buck mode (cont'd).

4. STEADY-STATE ANALYSIS AND DESIGN GUIDELINES

4.1 OUTPUT CHARACTERISTICS

If no loss is considered in the converter, the input power equals the output power. The derivation of output power is based on the primary-referred equivalent circuit and the idealized waveforms in Fig. 4.1. The following assumptions are made to simplify the analysis:

- The inductance of L_1 and L_2 is large enough to maintain the currents flowing through them and the assumption is made that they are constant.
- All switching devices are considered ideal.
- The output filter capacitors C1–C6 are large enough that $V_1 \sim V_6$ is considered constant.
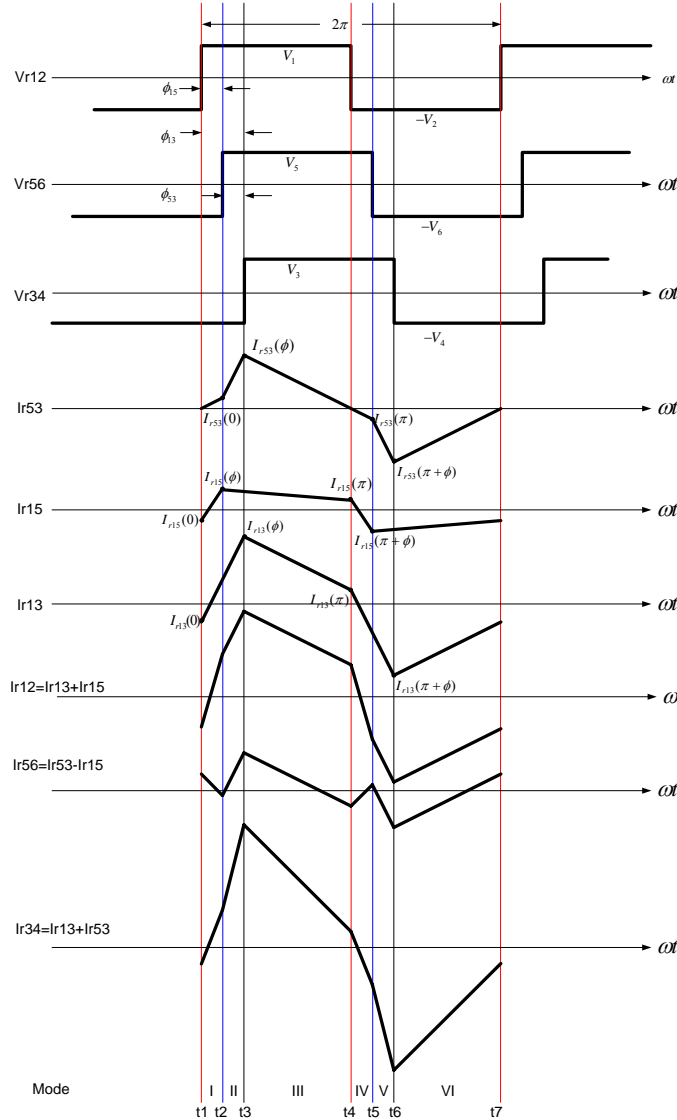
Fig. 4.1. Idealized voltages and current waveforms of a transformer on the condition that
$$v_1 = v_2 = v_5 = v_6 < v_3 = v_4.$$

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According to Fig. 4.1, there are six operating modes in one switching period. The transformer current I_{r13}, I_{r53}, and Ir_{15} is a function of $\theta = \omega t$, where ω is the switching frequency. In mode I

$$
\begin{cases}
I_{r13}(\theta) = \dfrac{V_1 + V_4}{\omega L_{r13}}\theta + I_{r13}(0) \\[2ex]
I_{r53}(\theta) = \dfrac{-V_6 + V_4}{\omega L_{r53}}(\theta - \pi - \phi_{13}) + I_{r53}(\pi + \phi_{13}) \\[2ex]
I_{r15}(\theta) = \dfrac{V_1 + V_6}{\omega L_{r15}}\theta + I_{r15}(0)
\end{cases}
\tag{1}
$$

Stage I ends at $\theta = \phi_{15}$. In mode II

$$
\begin{cases}
I_{r13}(\theta) = \dfrac{V_1 + V_4}{\omega L_{r13}}\theta + I_{r13}(0) \\[2ex]
I_{r53}(\theta) = \dfrac{V_5 + V_4}{\omega L_{r53}}(\theta - \phi_{15}) + I_{r53}(0) \\[2ex]
I_{r15}(\theta) = \dfrac{V_1 - V_5}{\omega L_{r15}}(\theta - \phi_{15}) + I_{r15}(\phi_{15})
\end{cases}
\tag{2}
$$

Mode II ends at $\theta = \phi_{13}$. In mode III

$$
\begin{cases}
I_{r13}(\theta) = \dfrac{V_1 - V_3}{\omega L_{r13}}(\theta - \phi_{13}) + I_{r13}(\phi_{13}) \\[2ex]
I_{r53}(\theta) = \dfrac{V_5 - V_3}{\omega L_{r53}}(\theta - \phi_{13}) + I_{r53}(\phi_{53}) \\[2ex]
I_{r15}(\theta) = \dfrac{V_1 - V_5}{\omega L_{r15}}(\theta - \phi_{15}) + I_{r15}(\phi_{15})
\end{cases}
\tag{3}
$$

Mode III ends at $\theta = \pi$. In mode IV

$$
\begin{cases}
I_{r13}(\theta) = \dfrac{-V_2 - V_3}{\omega L_{r13}}(\theta - \pi) + I_{r13}(\pi) \\[2ex]
I_{r53}(\theta) = \dfrac{V_5 - V_3}{\omega L_{r53}}(\theta - \phi_{13}) + I_{r53}(\phi_{53}) \\[2ex]
I_{r15}(\theta) = \dfrac{-V_2 - V_5}{\omega L_{r15}}(\theta - \pi) + I_{r15}(\pi)
\end{cases}
\tag{4}
$$

Mode IV ends at $\theta = \pi + \phi_{15}$. In mode V

$$\begin{cases} I_{r13}(\theta) = \dfrac{-V_2 - V_3}{\omega L_{r13}}(\theta - \pi) + I_{r13}(\pi) \\[3mm] I_{r53}(\theta) = \dfrac{-V_6 - V_3}{\omega L_{r53}}(\theta - \phi_{15} - \pi) + I_{r53}(\pi) \\[3mm] I_{r15}(\theta) = \dfrac{-V_1 + V_6}{\omega L_{r15}}(\theta - \pi - \phi_{15}) + I_{r15}(\pi + \phi_{15}) \end{cases} \qquad (5)$$

Mode V ends at $\theta = \pi + \phi_{13}$. In stage VI

$$\begin{cases} I_{r13}(\theta) = \dfrac{-V_2 + V_4}{\omega L_{r13}}(\theta - \pi - \phi_{13}) + I_{r13}(\pi + \phi_{13}) \\[3mm] I_{r53}(\theta) = \dfrac{-V_6 + V_4}{\omega L_{r53}}(\theta - \pi - \phi_{13}) + I_{r53}(\pi + \phi_{53}) \\[3mm] I_{r15}(\theta) = \dfrac{-V_1 + V_6}{\omega L_{r15}}(\theta - \pi - \phi_{15}) + I_{r15}(\pi + \phi_{15}) \end{cases} \qquad (6)$$

The output power from V_{in1} and V_{in2} are found to be

$$\begin{cases} P_1 = \dfrac{\int_0^{2\pi} I_{r12}(\theta)V_{r12}(\theta)d\theta}{2\pi} = \dfrac{\phi_{13}(\pi - |\phi_{13}|)}{con_{13}}V_{12}V_{34} + \dfrac{\phi_{15}(\pi - |\phi_{15}|)}{con_{15}}V_{12}V_{56} \\[4mm] P_2 = \dfrac{\int_0^{2\pi} I_{r56}(\theta)V_{r56}(\theta)d\theta}{2\pi} = \dfrac{\phi_{53}(\pi - |\phi_{53}|)}{con_{53}}V_{56}V_{34} + \dfrac{\phi_{51}(\pi - |\phi_{51}|)}{con_{51}}V_{56}V_{12} \end{cases} \qquad (7)$$

Where P_1 and P_2 can be transferred power in boost mode or buck mode depending on the sign of the phase-shift angles. The output power P_o is derived by

$$P_0 = P_1 + P_2 = \dfrac{\phi_{13}(\pi - |\phi_{13}|)}{con_{13}}V_{12}V_{34} + \dfrac{\phi_{53}(\pi - |\phi_{53}|)}{con_{53}}V_{56}V_{34} . \qquad (8)$$

When the transferred power is derived, the input-inductor currents and output voltage can be found to be

$$\begin{cases} V_{34} = \dfrac{\phi_{13}(\pi - |\phi_{13}|)R}{con_{13}}V_{12} + \dfrac{\phi_{53}(\pi - |\phi_{53}|)R}{con_{53}}V_{56} \\[4mm] I_{L1} = \dfrac{\phi_{13}(\pi - |\phi_{13}|)}{con_{13}}\dfrac{V_{34}}{D} + \dfrac{\phi_{15}(\pi - |\phi_{15}|)R}{con_{15}}\dfrac{V_{56}}{D} \\[4mm] I_{L2} = \dfrac{\phi_{53}(\pi - |\phi_{53}|)}{con_{53}}\dfrac{V_{34}}{D} + \dfrac{\phi_{51}(\pi - |\phi_{51}|)R}{con_{51}}\dfrac{V_{12}}{D} \end{cases} \qquad (9)$$

Where $con_{13} = con_{31} = 4\pi\omega L_{r13}$, $con_{53} = con_{35} = 4\pi\omega L_{r53}$, and $con_{15} = con_{51} = 4\pi\omega L_{r15}$.

According to Eqs. (1–8), the control variables of the proposed converter are ϕ_{13} and ϕ_{53}. Figure 4.2 describes the output variables P_1, P_2, and V_{34} as functions of these control variables. The interactions between the two input stages exist as expected.
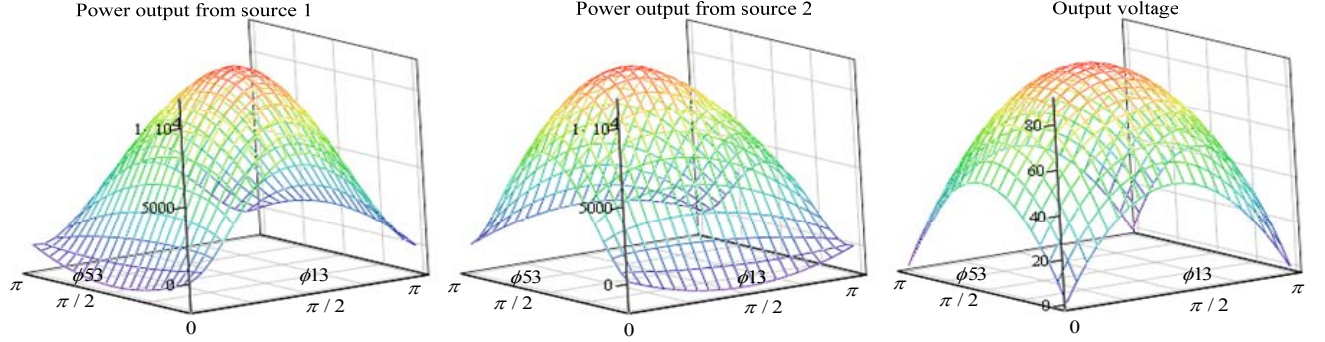
Fig. 4.2. Three-dimensional plot of output power and voltage as a function of control variables ϕ_{13} and ϕ_{53}.

The effects of ϕ_{13} and ϕ_{53} upon output characteristics can be further illustrated in Fig. 4.3. In each subplot, the output variable has four different operation regions divided by certain values of ϕ_{13} and ϕ_{53}. For example, in the first subplot of Fig. 4.3, P_1 and I_{L1} will increase with ϕ_{13} and ϕ_{53} if $\phi_{13} < \phi_{crit13\text{-}P1}$ and $\phi_{53} < \phi_{crit53\text{-}P1}$, which is denoted in the shaded operation region located at the bottom left corner. Critical points are derived from Eqs. (7) and (8). The critical points will depend on the circuit parameters, such as input voltage or transformer-leakage inductance as well as load resistance. At critical points, the corresponding output will reach the maximum value and the values of these three critical points are different. The critical points are not only useful for converter steady-state design, but also important for the closed-loop controller design. The phase-shift angles should be limited in one of the three shaded operation regions based on which output variable is required to be regulated. For example, if both I_{L1} and I_{L2} are required to be controlled, tradeoffs need to be made between them and a smaller value of ϕ_{crit13} and ϕ_{crit53} will be chosen to remain stable. In this case, the shaded area shrinks which means a smaller operation range and degraded output capability.
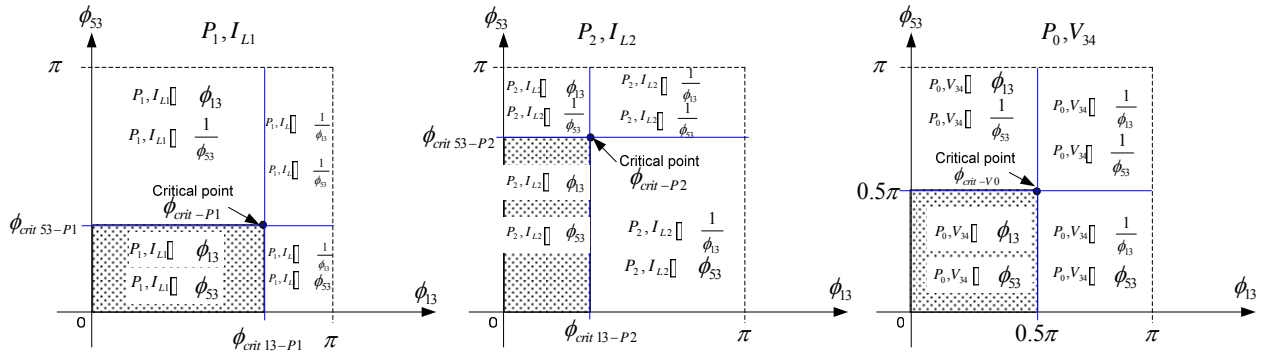
Fig. 4.3. The relation between output characteristics and control variables ϕ_{13} and ϕ_{53}.

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4.2 SOFT-SWITCHING CONDITIONS

The commutation mechanism is similar to the single-input ZVS bi-directional converter; i.e., the turn-off device diverts the current to the corresponding resonant capacitors to realize a zero voltage turn-off and the zero voltage turn-on is achieved by gating on the incoming device while the anti-parallel diode is conducting. However, the soft-switching condition becomes more complicated due to the interactions between the two input stages. The soft-switching condition in boost mode is derived in Eq. (10) where the corresponding times can be referred to from Fig. 4.1.

$$
\begin{cases}
f_1 = I_{r12}(t_4) - I_{L1} > 0 \\
f_2 = I_{r56}(t_5) - I_{L2} > 0 \\
f_3 = -I_{r34}(t_6) > 0 \\
f_4 = I_{L1} - I_{r12}(t_1) > 0 \\
f_5 = I_{L2} - I_{r56}(t_2) > 0 \\
f_6 = I_{r34}(t_3) > 0
\end{cases}
\tag{10}
$$

Functions f_1 to f_6 denote the six conditions corresponding to switches S_2, S_6, S_4, S_1, S_5, and S_3 respectively. They can be derived in terms of the control variables ϕ_{13} and ϕ_{53} that are plotted in Fig. 4.4. The phase-shift angle could be in the range $[-\pi, \pi]$, but only the range $[0, \pi]$ is considered as an example here since $[-\pi, 0]$ is symmetrical to it. As we can see from Fig. 4.4, the soft-switching conditions of S_1 and S_2 will be easier to be met with the increase of ϕ_{13} and the decrease of ϕ_{53}, which means the soft-switching conditions of one input stage is influenced by the control variable of the other input stage. Functions f_2 and f_5 are always positive, which means S_6 and S_5 will remain soft-switching regardless of the values of ϕ_{13} and ϕ_{53}. However, the interactions between the two input stages exist as well. The soft-switching conditions of S_3 and S_4 will be satisfied with large values for ϕ_{13} and ϕ_{53}.

Soft-switching condition 1

Soft-switching condition 2

Soft-switching condition 3

Soft-switching condition 4

Soft-switching condition 5

Soft-switching condition 6
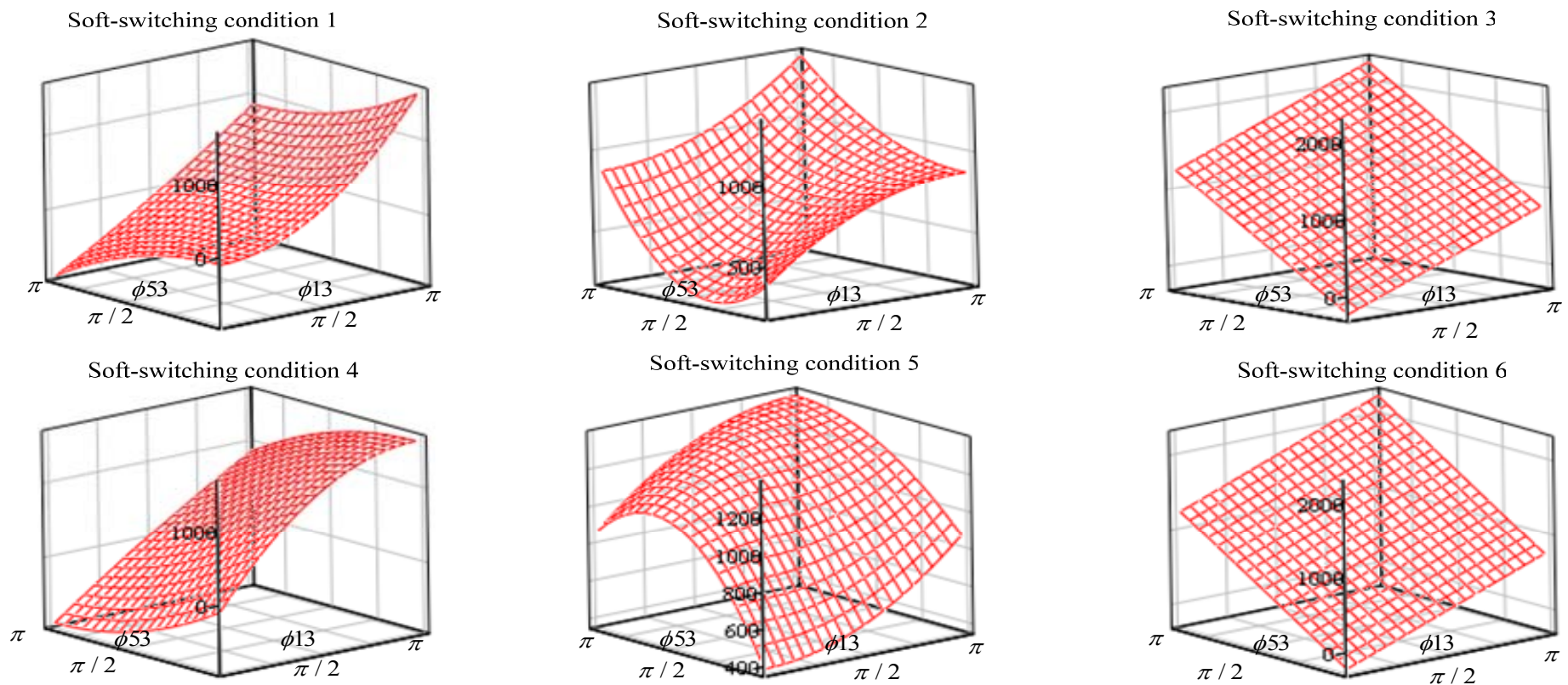
Fig. 4.4. The relation between soft-switching conditions and control variables ϕ_{13} and ϕ_{53}.

4.3 SIMULATION VERIFICATION

The circuit simulation results for boost and buck modes are presented to verify the theoretical analysis. The parameters used for simulation are described as

$$L_1 = L_2 = 5\mu H \ . \tag{11}$$

The switching frequency is f_s = 20 kHz, and the transformer ratios are $N_{12} : N_{56} : N_{34} = 1:1:12$, with $L_{r13} = L_{r53} = 0.3\mu H$, and $L_{r15} = 0.6\mu H$.

The filter capacitors values are $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = 0.01F$ and the resonant capacitors are $C_{r1} = C_{r2} = C_{r3} = C_{r4} = C_{r5} = C_{r6} = 3uF$. The output voltage with transformer ratio is selected to be $v_o = (v_3 + v_4) \times 12 = 288V$.

4.3.1 Boost Mode

Simulated waveforms for the boost mode use $\phi_{13} = 0.35\pi$, $\phi_{53} = 0.25\pi$, $I_{L1} = 295A$, $I_{L2} = 142.5A$, $P_1 = 3540W$, $P_2 = 2565W$, $V_{in1} = 12v$, and $V_{in2} = 18v$. Simulated waveforms are presented in Fig. 4.5.
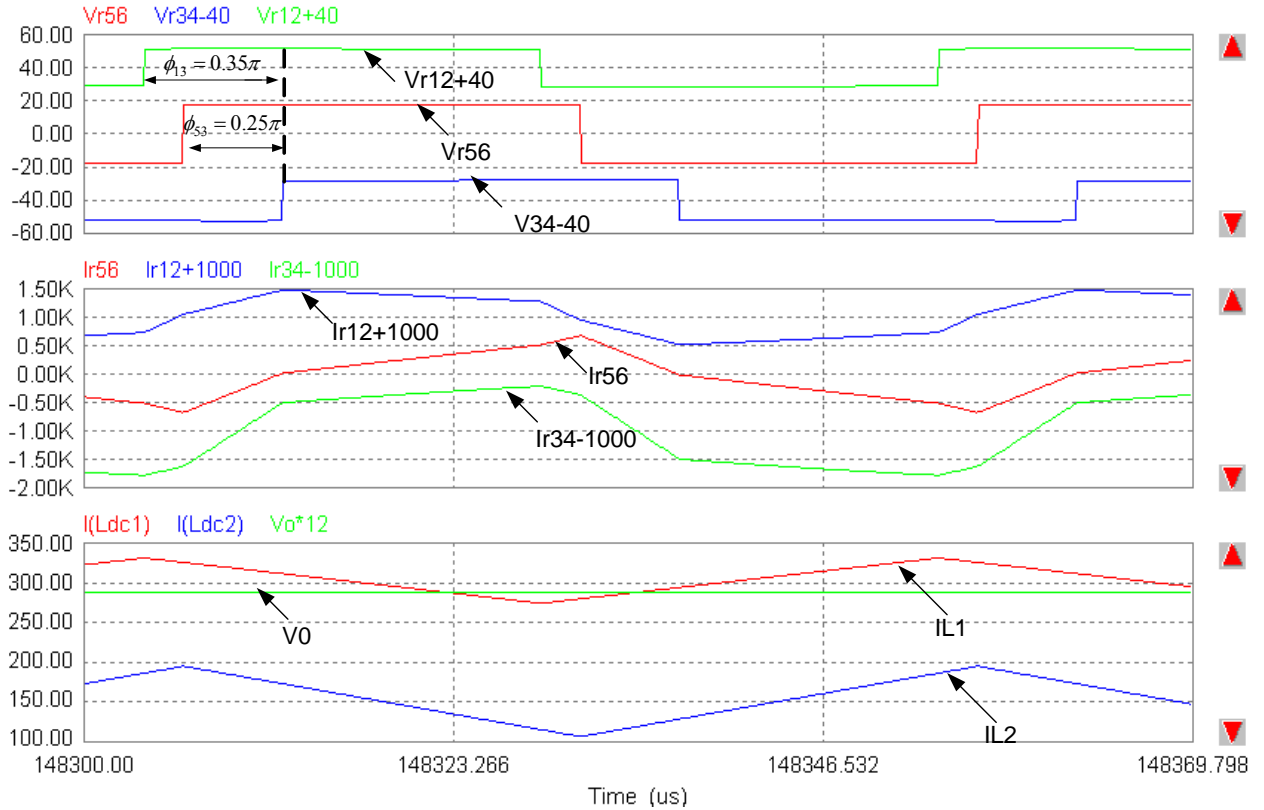
Fig. 4.5. Simulated waveforms for boost mode.

4.3.2 Buck Mode

Simulated waveforms for the buck mode use $\phi_{13} = -0.2\pi$, $\phi_{53} = -0.274\pi$, $I_{L1} = -108.6A$, $I_{L2} = -233.1A$, $P_1 = 1976W$, and $P_2 = 4778.5W$. The charge voltages are $V_{in1} = 18V$ and $V_{in2} = 20V$. Simulated waveforms are presented in Fig. 4.6.
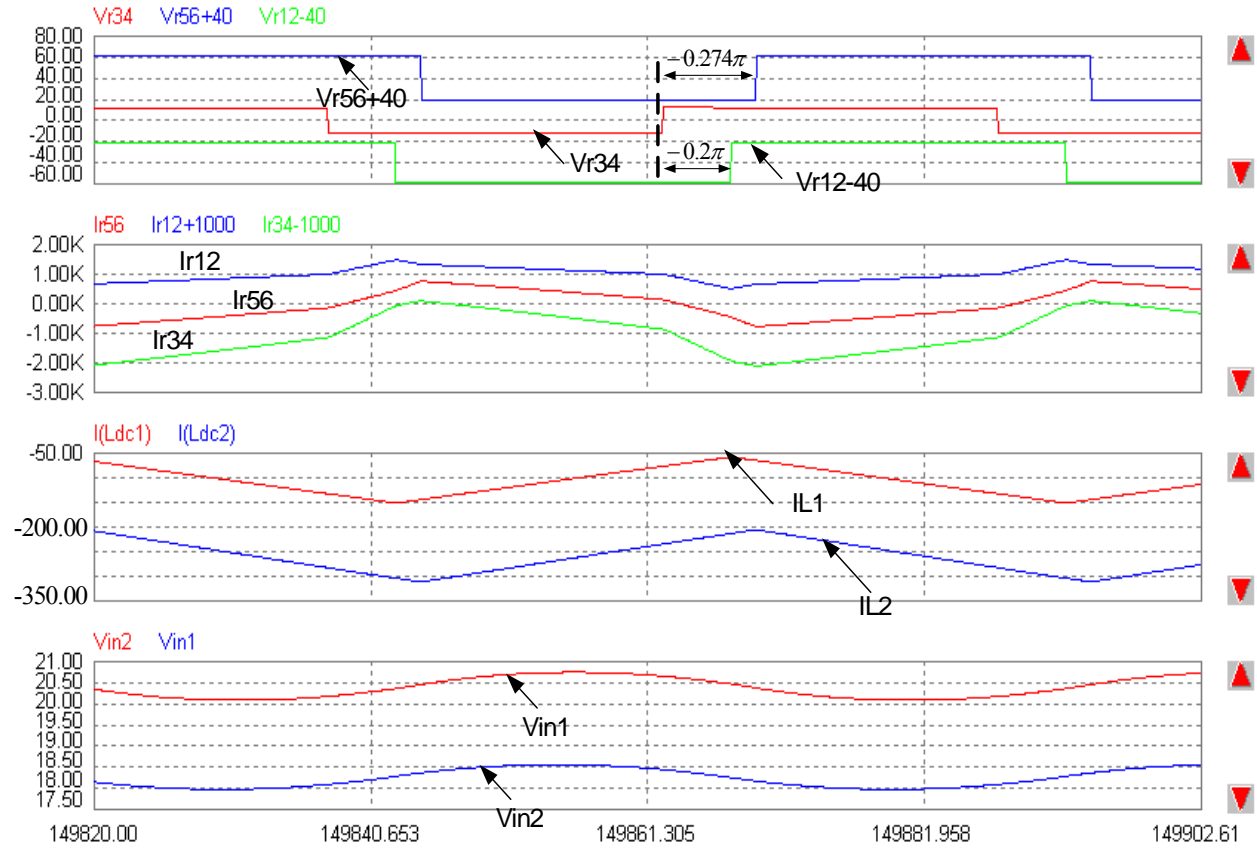
Fig. 4.6. Simulated waveforms for buck mode.

5. DESIGN AND IMPLEMENTATION

The specifications of the proposed dc-dc converter application are reviewed as

- The nominal voltage at the LVS of one input is 12 V and another input is 16 V. These values can vary from 8–16 V and from 12–20V during charging and discharging.
- The nominal high-side voltage is 288 V, with an operating range of 255–425V.
- Nominal discharging power of the two inputs is 2 kW and 3.5 kW, respectively.
- The nominal output power is 5 kW.
- Bus capacitance C_o is less than 2000 μF.

The numerical design guidelines are briefly listed here (see Appendix A for Mathcad Design file). If L_{dc1} and L_{dc2} are designed as 6 μH, L_{r12} is selected as *0.5 μH*, L_{r56} is *0.4 μH*, $\phi_{13} = 0.4\pi$, $\phi_{53} = 0.4\pi$, η = 90%, $V_{out} = 380$ V, and R = 27 Ω; then the discharging power of the two inputs are calculated as $P_1 = 2.2$kW, $P_2 = 3.7$kW, and $P_o = 5.3$kW. The average currents provided by the two inputs can be found to be $I_{d1} = 185A$ and $I_{d2} = 232A$ with current ripple of 50A for L_{dc1} and 67A for L_{dc2}. The root-mean square (rms) and peak current for each device and leakage inductances L_{r12}, L_{r56}, and L_{r34} are derived as indicated in Table 5.1.

Table 5.1. Current rating for each device and leakage inductances

	S1	S2	S3	S4	S5	S6	Lr12	Lr56
RMS current (A)	104	193	33	33	293	369	237	363
Peak current (A)	400	400	59	59	625	618	328	393

5.1 MAGNETIC-COMPONENT DESIGN

5.1.1 Transformer Design

A multi-winding transformer plays an important role in this converter circuit. The leakage inductance of the transformer is utilized as an energy-transfer element between the inputs and the load. The leakage inductance is dependent on the geometry of the windings. Figure 5.1 is the designed physical structure of a three-winding transformer for the proposed converter. Only the right half of the transformer is illustrated because of symmetrical characteristics. Windings P11 and P12 are connected in parallel to allow higher current, the same as S11 and S12, and P21 and P22. Fluxes flowing across the core are Φ_m and Φ_0. Fluxes between windings are represented as $\Phi_{l0} - \Phi_{l6}$.
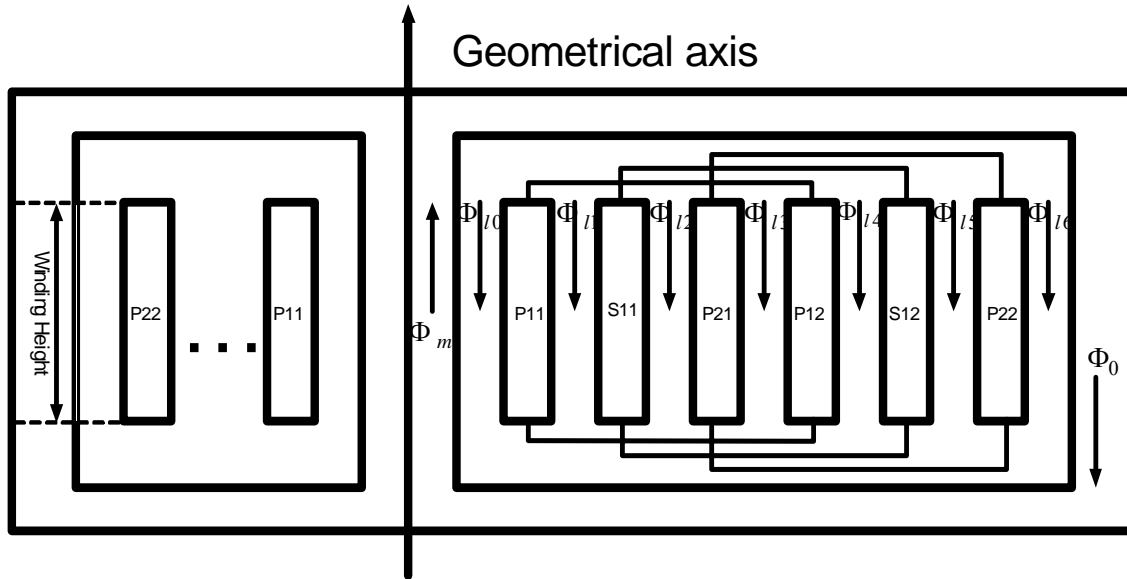
Fig. 5.1. Designed physical structure of a three-winding transformer.

The transformer is very important for the converter design. The ideal transformer should be of high-power density, high efficiency, and high-switching frequency. The issues of core material selection and winding geometry for the minimum core and copper losses at the highest possible switching frequency need to be considered. In addition, the designed-leakage inductance is small and requires the use of special low-leakage transformer design techniques.

5.1.2 Core-Material Selection

The characteristics of a good core material include high-operating frequency, low specific-core loss, and low-power/weight ratio. With the selected switching frequency, $f_s = 20$ kHz, the Ferroxcube E80/38/20-3C81 core was selected.

The designed winding structure and parameters are shown in Fig. 5.2. The sandwich structure is used to decrease the leakage inductance.
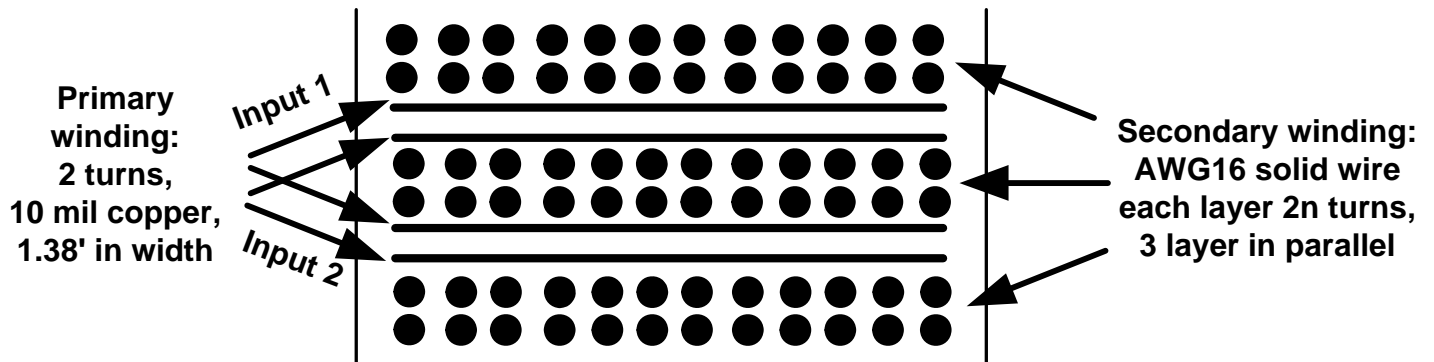
Fig. 5.2. Transformer winding structure.

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5.1.3 Turns-Ratio Selection

The main consideration for turns-ratio selection depends on the output voltage matching capability in the full regions of battery, UC, and load variations. It is required that $255\,V \leq v_o \leq 425\,V$ and n was selected as 12.

5.2 BOOST INDUCTOR L_{dc} DESIGN

The boost inductor is designed according to the peak-input current and the required inductance value. In addition, it should not saturate during maximum power-peak charging. The boost inductance L_{dc} was selected as 6 μH. A Metglas core with high-saturation flux density, AMCC-25 from Allied Signal, was selected for the prototype. An eight-turn copper-foil winding was used with an air gap of 0.07 inches on each side. Figure 5.3 is a photo of two boost inductors.
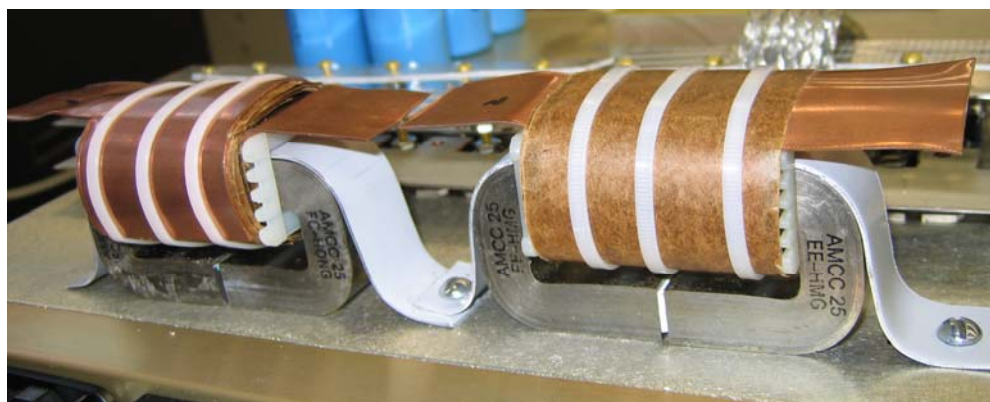
Fig. 5.3. Photo of two boost inductors.

5.3 LEAKAGE-INDUCTANCE DESIGN

The leakage inductance of a transformer can be designed to be a very small value. Therefore, the external inductances are required to provide the controllable power to the output. The external leakage inductance, L_{r12} and L_{r56}, was designed with consideration as to the rms and peak current of transformer. Figure 5.4 is a photo of the fabricated L_{r12} and L_{r56}.
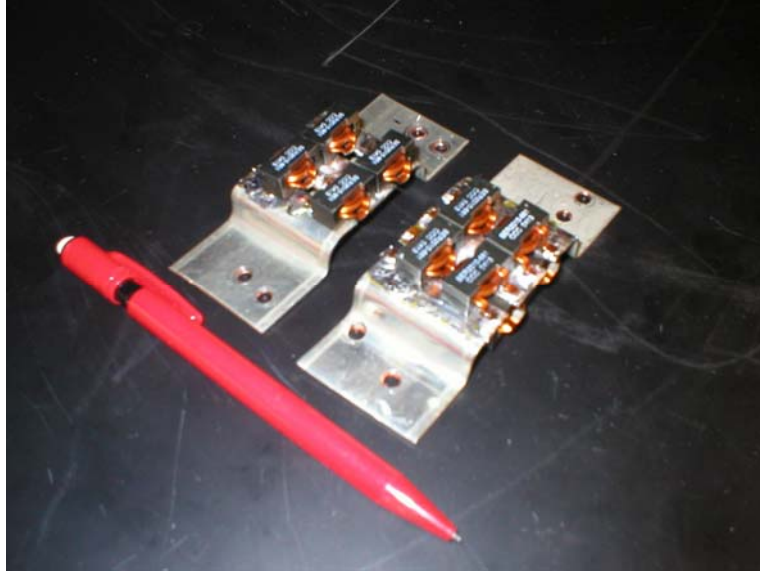
Fig. 5.4. Photo of external leakage inductance L_{r12} and L_{r56}

5.4 CAPACITOR SELECTION

5.4.1 Resonant Capacitor Selection

For the LVS and HVS, the capacitances of the resonant capacitors are designed according to the required *dv/dt* range. A low estimated-series resistance (ESR) and estimated-series inductance (ESL) capacitor is preferred. A polypropylene capacitor was not available with the necessary low-voltage rating, so a ceramic capacitor of 0.1uF @ 50V was selected for each metal oxide semiconductor field-effect transistor (MOSFET).

The resonant capacitor on the HVS was selected as 0.033uF @ 600V. A polypropylene capacitor (orange drop) 716P33396K was utilized.

5.4.2 DC Capacitor Selection

The electrolytic capacitors are *C1, C2, C3,* and *C4*. The main concerns for selecting the capacitors are the ESR value, the ripple-current capability, and the size. To facilitate the circuit layout, higher density was also considered. United Chemi-Con's 747D812M035AA2A, 8100 μF @ 35 VDC, size D×L (inch) 1.375 × 2.125, ESR 5.9 ± 30% mΩ, with a maximum ripple current of 12.8 A(rms) at 20 kHz was selected for C_1 and C_2.

The capacitors for the HVS are Sprague's 80D101P250JA5D, 100 μF @ 250VDC. The high-frequency capacitors, *C1* and *C2*, are Sprague's polypropylene capacitor 10μF @ 100V. The high-frequency capacitors of *C3* and *C4* are 0.47uF @ 400V polypropylene capacitors, part number 716P47494M.

5.5 POWER SWITCHES

5.5.1 LVS Switches

The low voltage and high-current requirements of the LVS switches are optimized with MOSFETs. When D = 50%, the voltage across the switch is two times v_{in} during steady state. Because of the soft-switching characteristics, the overshoot voltage during switching transients is small. Thus, 55V MOSFETs satisfy the requirements. However, a 100 V device was selected to provide an additional safety margin.

Analysis shows that the peak current of S5 and S6 in steady-state operation in the discharging mode will be more than 600A. The rms current of S6 is estimated at 400 A. Paralleling of MOSFETs is required to handle this large current. Fortunately, the positive temperature coefficient nature of their on-resistance makes current sharing among the paralleled devices a minor concern.

Of greater concern is the on-resistance. Because of high current on the LVS, the conduction loss is significant. Therefore, the on-resistance should be as small as possible. In addition, the on-resistance will increase with the temperature above 25ºC.

For the prototype design, the FB180SA10, SOT-227 MOSFETs were selected because of their fast speed, low on-resistance, large current rating, and easy packaging. The related parameters can be found in Table 5.2.

Table 5.2. Datasheet of MOSFETs for LVS switches

Maker	Model	Vds	I_D	Rds@25ºC	Input capacitance
IR	FB180SA10	100V	180A	0.0065W	10700 pF

5.5.2 HVS Switches

Since the output voltage range is 255–425V, the voltage ratings of the high-side switches can be specified at 600V. For the prototype, a 600V/75A device is first selected. The half-bridge insulated gate bipolar transistor (IGBT) modules are favored due to their packaging design.

A Fuji 2MBI, 75N-060, 600V/75A IGBT half-bridge was selected because of its fast speed. Additional data can be found in Table 5.3.

Table 5.3. IGBT half-bridge for HVS switches

Make	Model	V_{CES}	I_C	V_{CE}(sat)	Input cap.	Switching time (µsec)			
						t_{on}	t_r	t_{off}	t_f
Fuji	2MBI75N-060	600 V	75A	3V	4950pF	1.2	0.6	1.0	0.35

5.6 AUXILIARY POWER SUPPLY AND GATE-DRIVE CIRCUITS

In the proposed converter system, the six switches need six isolated power supplies for gate drivers. According to the devices' characteristics, it was decided to use +10 V for the four MOSFET drivers on the LVS and a positive 20 V for the two IGBT drivers on the high side. In the digital-signal processor (DSP) control board, +15V, -15V, and +5V power supplies are needed. The schematic view of the power supplies are shown in Fig. 5.5. All of them need accurate regulation.

primary side

4 × 10 V

+10v   +10v   +20v   +20v

power supplies for the gate drivers

primary side

+15v   -15v   +3.3v   +5v

power supplies for DSP and sensing circuits
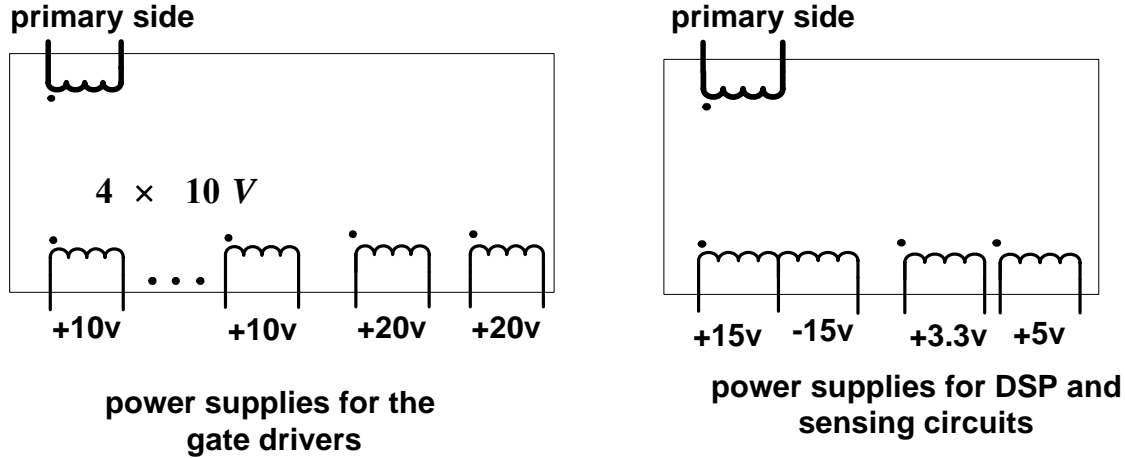
Fig. 5.5. Schematic view of power supplies.

The proper marriage of a MOSFET gate driver and the power MOSFET is essential for good switching performance. Using a gate driver that matches the MOSFET characteristics provides fast rise/fall times and reduces associated losses. The gate drivers selected are MICREL, MIC4451, and MIC4452. With the output of the fly-back power supply for the MOSFET at 10 V, the total maximum gate-driver output current is 8A. MIC4451 is an inverting driver and the MIC4452 is a non-inverting driver. The supply voltage can be as high as 20 V and must be capable of providing 12A peak-current output.

The power MOSFETs used were six IR's FB180SA10 in parallel. The gate-input capacitance is 10700 pF per device and the gate charge Qg is 250 nC per device. For switches on the LVS, six devices in parallel will have a total gate charge of 1500 nC. The device rise and fall times are 351 ns and 350 ns at the switching current of 180A, which is compatible with a switching frequency of 20 kHz.

An HP2212 opto-coupler is used to provide electrical isolation between the control circuit and the power stage mainly for its high speed and high-common mode noise rejection. The HP2212 can work with a supply voltage up to 20 V. The output of the opto-coupler drives the MIC4451 and 4452 chip via a pull-up resistor of 350 ohms.

A gate-drive opto-coupler HCPL-316J is used to drive the IGBT modules. Like the traditional IGBT-driver IC EXB840/850, it can also provide over-current protection and fault-status feedback. In addition, it has a smaller footprint size than older drivers.

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5.7 POWER-STAGE LAYOUT DESIGN

Low-leakage inductance packaging is important to minimize the conduction loss of the switches. The resonant capacitors must be as close as possible to the main devices to reduce the leakage inductance of the loop and avoid any ringing effects. The connection resistance must be as low as possible; otherwise, the large current flowing through it will add extra losses to the system. The layout of the prototype is shown in Fig. 5.6.
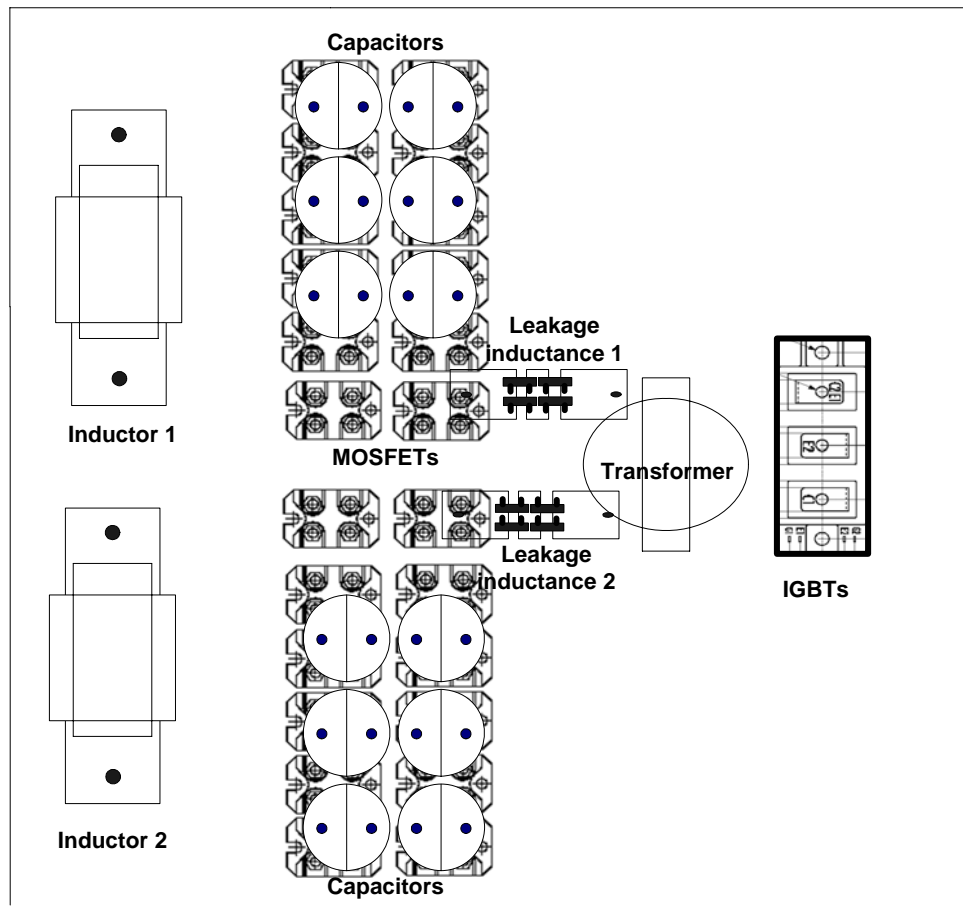
Fig. 5.6. Layout of power circuit.

6. EXPERIMENTAL RESULTS

6.1 EXPERIMENTAL SETUP

In order to validate the analysis and simulation results obtained in the previous chapters, a 5 kW dc-dc converter was built and tested. The prototype is pictured in Fig. 6.1. The power stage is laid on a fan-cooled heat sink and has an overall size of ~16 inches in length and 15 inches in width. The size of the converter is 12 inches by 15 inches by 7 inches. The converter is operated at a switching frequency of 20 kHz. The transformer-turns ratio is 1:12.
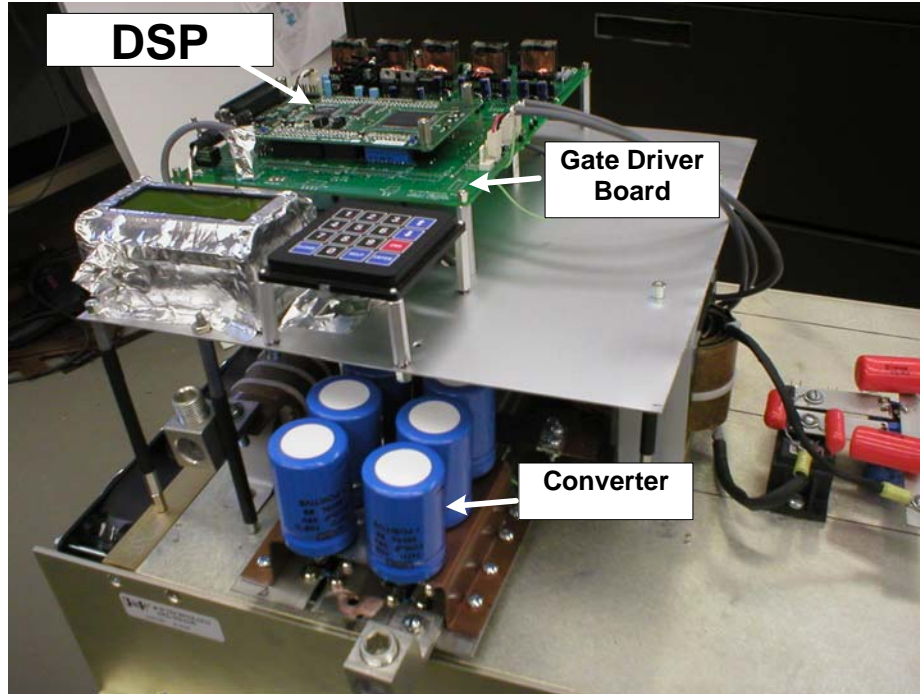
Fig. 6.1. Picture of prototype.

S1, S2, S5, S6:   IR FB180SA10 100V/80A, SOT-227 MOSFET × 6
S3, S4:   FUJI 2MBI75N-060 600V/75A, a half-bridge IGBT module
C1, C2, C5, C6:   747D812M035AA2A, 35 V, 8100 uF electrolytic capacitor × 3
                    (United Chemi-Con)
C3, C4:   80D101P250JA5D, 250V, 100μF electrolytic capacitor (Sprague)
Tr: 2:24:24 turns, E80/38/20-3C81 core (Ferroxcube)
L_{dc}:   6 μH, 8 turns copper foil, AMCC-25 Metglas C-core
L_{r12}:   0.68 μH SER2010-681 × 8 (Coilcraft)
L_{r34}:   0.80 μH SER2010-801 × 8 (Coilcraft)
Cr1-Cr2:   0.1 μF, 50V ceramic capacitor
Cr3-Cr4:   600V, 0.033μF polypropylene capacitor

6.2 EXPERIMENTAL RESULTS

6.2.1 With Phase-Shift Degree

The measured-circuit waveform during discharging operation at a reduced power rating is shown in Fig.6.2. It can be seen that the first input will provide more power than the second because of its larger phase-shift degree referred to the secondary side. The voltage waveforms of V_{r12}, V_{r34}, and V_{r56} do not have high oscillations and large overshoots, which indicate the switches have achieved soft-switching. The soft-switching of each device can be further verified with the derived soft-switching condition as follows

$$\begin{cases} f_1 = I_{r12}(t_4) - I_{L1} > 0 \\ f_2 = I_{r56}(t_5) - I_{L2} > 0 \\ f_3 = -I_{r34}(t_6) > 0 \\ f_4 = I_{L1} - I_{r12}(t_1) > 0 \\ f_5 = I_{L2} - I_{r56}(t_2) > 0 \\ f_6 = I_{r34}(t_3) > 0 \end{cases}$$

We can see that f_1 to f_6 are positive, which means S1–S6 are soft-switching. Figure 6.3 shows the calculated results using Mathcad. The experimental waveform is consistent with the design values.

Fig. 6.2. Measured waveform under boost-mode operation with $V_{in1} = 8V$, $V_{in2} = 5V$, $I_1 = 52A$, $I_2 = 24A$, $\phi_{13} = 0.15\pi$, $\phi_{53} = 0.1\pi$, $L_{r12} = L_{r34} = 0.4 \mu H$, $V_{out} = 123V$, and $P_{out} = 420W$.

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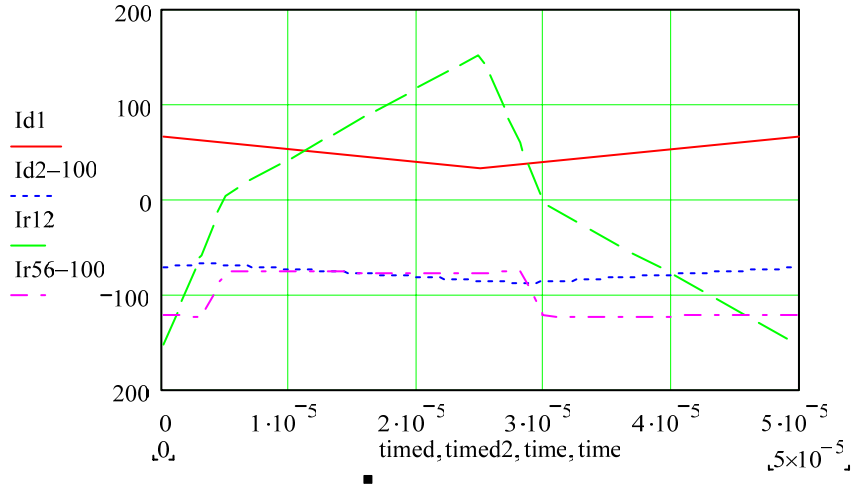
Fig. 6.3. Calculated-current waveform under boost-mode operation with V_{in1} = 8V, V_{in2} = 5V, ϕ_{13} = 0.15π, ϕ_{53} = 0.1π, L_{r12} = L_{r34} = 0.4 μH, and V_{out} = 123V.

6.2.2 No Phase-Shift Degree

The measured circuit waveforms with no phase-shift degrees are shown in Fig. 6.4. Both inputs provide the same power to the output because they share the same phase-shift degree, which can be observed from V_{r12} and Vr_{56}. The input currents I_{dc1} and I_{dc2} have the same magnitude and shape as does I_{r12} and I_{r56}, which are the currents flowing through the primary sides of the transformer. The soft-switching of all six switches provides no high-voltage overshoot or oscillations. The analytical results from Mathcad are compared with the experimental results in Fig. 6.5.

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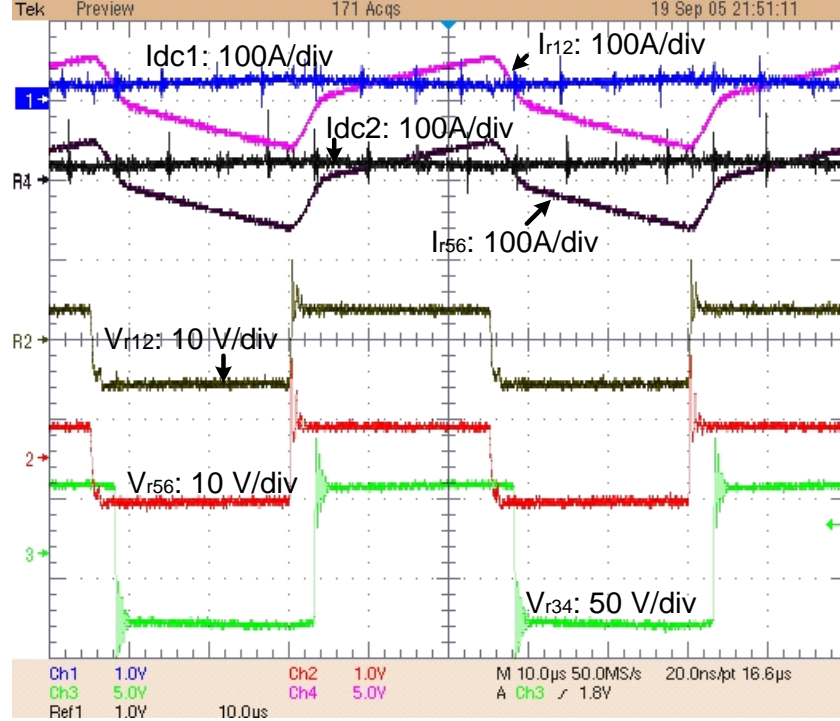
Fig. 6.4. Measured waveform under boost-mode operation with $V_{in1} = 5V$, $V_{in2} = 5V$, $I_1 = 27A$, $I_2 = 27A$, $\phi_{13} = 0.13\pi$, $\phi_{53} = 0.13\pi$, $L_{r12} = L_{r34} = 0.4\ \mu H$, $V_{out} = 90\ V$, and $P_{out} = 225W$.
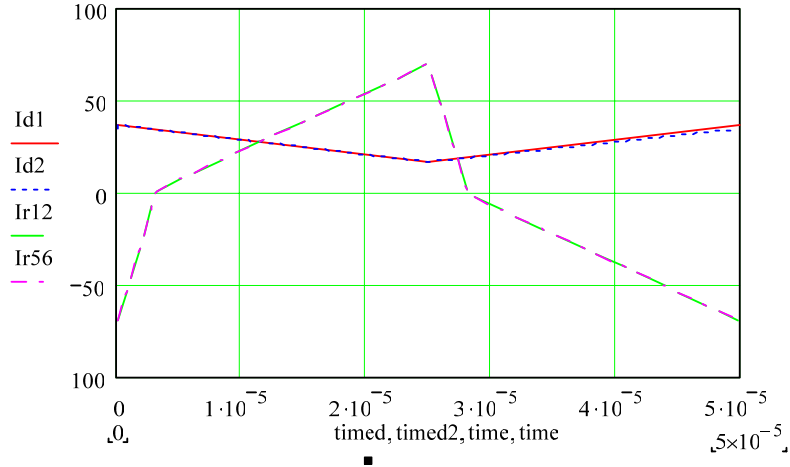
Fig. 6.5. Calculated waveform under boost-mode operation with $V_{in1} = 5V$, $V_{in2} = 5V$, $\phi_{13} = 0.13\pi$, $\phi_{53} = 0.13\pi$, $L_{r12} = L_{r34} = 0.4\ \mu H$, and $V_{out} = 90\ V$.

6.2.3   Additional Experimental Results

After the concept of the proposed topology had been verified, the converter was redesigned and tested at a higher-power rating. Figure 6.6 shows the experimental waveforms measured at an output power of 2.597 kW. There is no phase shift between two inputs, so there is no energy

transferred between the inputs. The analytical result is presented in Fig. 6.7 and shows consistency with the experimental results.
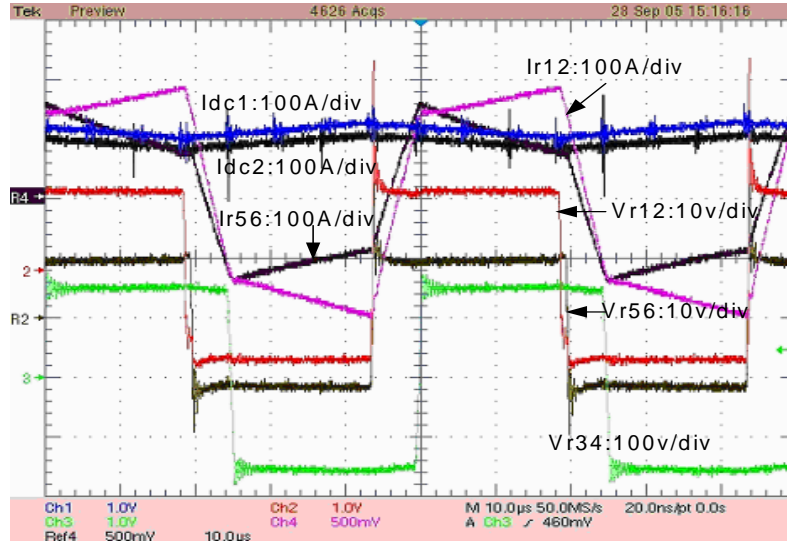
Fig. 6.6. Measured waveform under boost-mode operation with $V_{in1} = 15V$, $V_{in2} = 11V$, $I_1 = 123A$, $I_2 = 92A$, $\phi_{13} = 0.25\pi$, $\phi_{53} = 0.25\pi$, $L_{r12} = 0.5 \mu H$, $L_{r34} = 0.55 \mu H$, $V_{out} = 310 V$, $R = 37Ohm$, and $P_{out} = 2597W$.
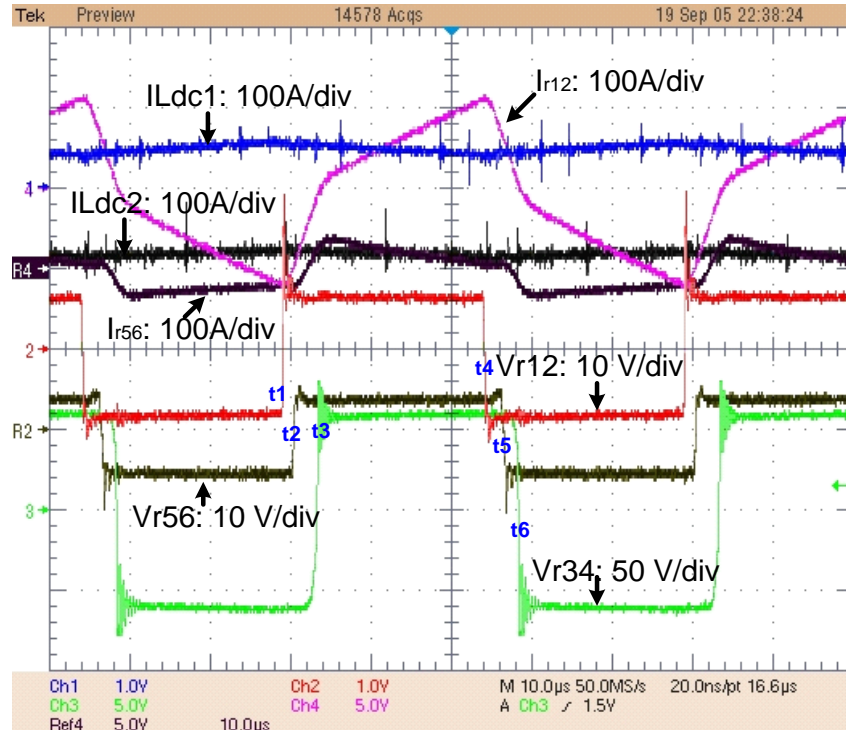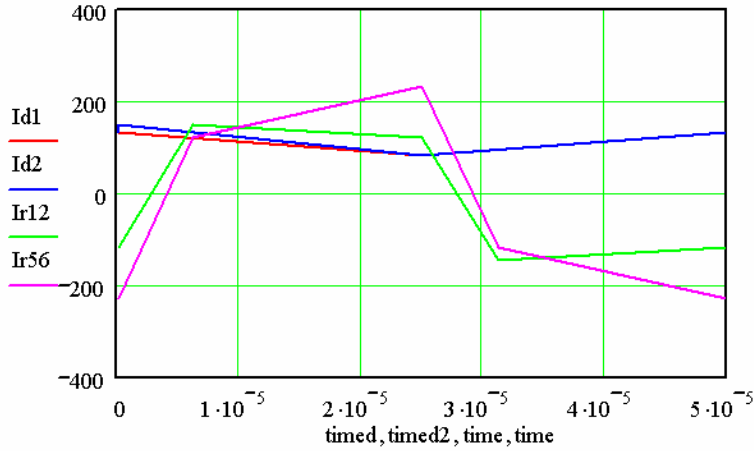

Fig. 6.7. Calculated waveform under boost-mode operation with $V_{in1} = 15V$, $V_{in2} = 11V$, $I_1 = 123A$, $I_2 = 92A$, $\phi_{13} = 0.25\pi$, $\phi_{53} = 0.25 \pi$, $L_{r12} = 0.5 \mu H$, $L_{r34} = 0.55 \mu H$, $V_{out} = 310 V$, $R = 37Ohm$, and $P_{out} = 2597W$.

Figure 6.8 shows the experimental waveforms with a phase shift between the two inputs. The output power is 2.681 kW. The analytical result is presented in Fig. 6.9 and shows the consistency with the experimental results.
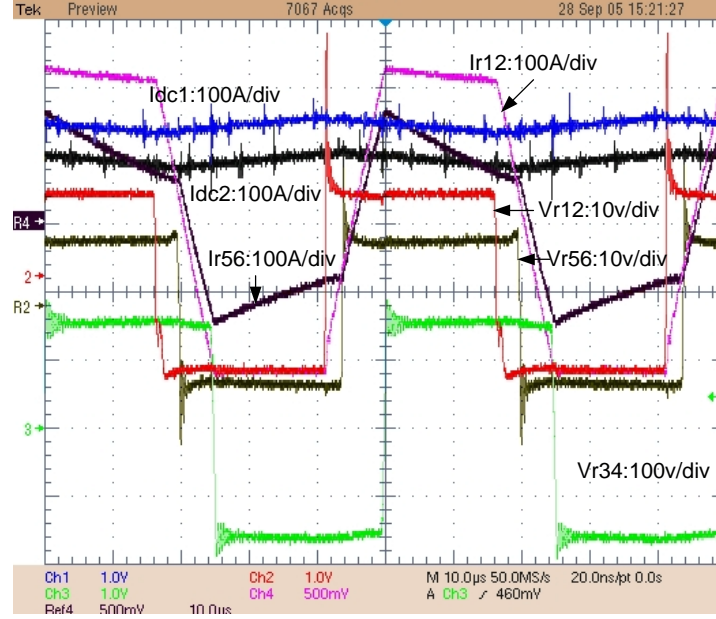
Fig. 6.8. Measured waveform under boost-mode operation with V_{in1} = 12.5V, V_{in2} = 10V, I_1 = 150A, I_2 = 100A, ϕ_{13} = 0.35π, ϕ_{53} = 0.25π, L_{r12} = 0.5 µH, L_{r34} = 0.55 µH, V_{out} = 315 V, R = 37Ohm, and P_{out} = 2681W.
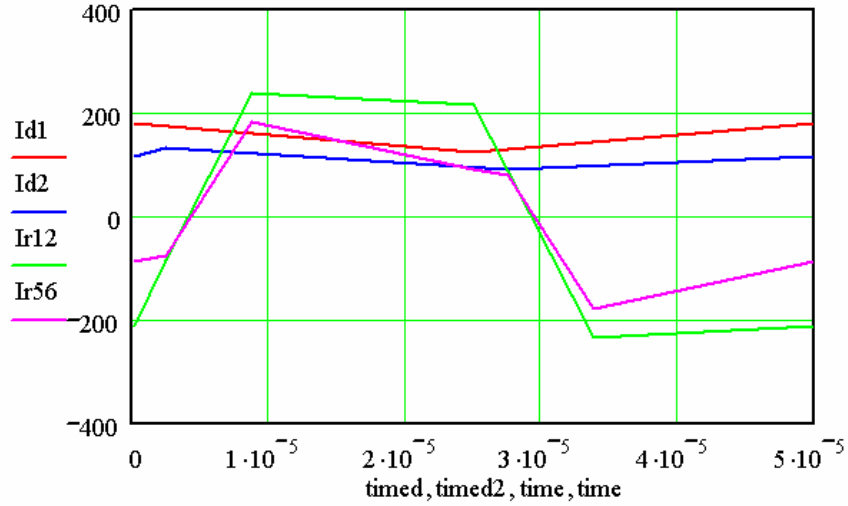
Fig. 6.9. Calculated waveform under boost-mode operation with V_{in1} = 12.5V, V_{in2} = 10V, I_1 = 150A, I_2 = 100A, ϕ_{13} = 0.35π, ϕ_{53} = 0.25π, L_{r12} = 0.5 µH, L_{r34} = 0.55 µH, V_{out} = 315 V, R = 37Ohm, and P_{out} = 2681W.

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DHB Converter Design File

Date : 9/20/06

"Filename: twoinput_experi.mcd

DESIGN INPUT

$Vin1 := 12$ $Vin2 := 16$ $fs := 20 \cdot 10^3$ $\pi = 3.14159265359$

$Ldc1 := 6 \cdot 10^{-6}$ $Ldc2 := 6 \cdot 10^{-6}$ $Vo := 380$ $\eta := 0.9$

$Lr12 := .5 \cdot 10^{-6}$ $Lr56 := .4 \cdot 10^{-6}$ $Lr34 := .005 \cdot 10^{-6}$

$\phi13 := .4 \cdot \pi$ $\phi53 := .4 \cdot \pi$

$D := .5$ $n := 12$

DESIGN PARAMETERS

$V12 := \dfrac{Vin1}{D}$ $V56 := \dfrac{Vin2}{D}$ $V1 := Vin1$ $V2 := V1$ $V5 := \dfrac{V56}{2}$

$V34 := \dfrac{Vo}{n}$ $V3 := \dfrac{V34}{2}$ $V4 := V3$ $V6 := V5$

$\phi15 := \phi13 - \phi53$ $\phi51 := -\phi15$

$Lr13 := \dfrac{Lr12 \cdot Lr34 + Lr34 \cdot Lr56 + Lr56 \cdot Lr12}{Lr56}$

$Lr15 := \dfrac{Lr12 \cdot Lr34 + Lr34 \cdot Lr56 + Lr56 \cdot Lr12}{Lr34}$

$Lr53 := \dfrac{Lr12 \cdot Lr34 + Lr34 \cdot Lr56 + Lr56 \cdot Lr12}{Lr12}$

$Ts := \dfrac{1}{fs}$ $\omega := 2 \cdot \pi \cdot fs$

$con13 := 4\pi \cdot \omega \cdot Lr13$ $con53 := 4\pi \cdot \omega \cdot Lr53$ $con15 := 4\pi \cdot \omega \cdot Lr15$

$V12 = 24$ $V34 = 31.6666$ $V56 = 32$ $Vo = 380$ $V1 = 12$ $V2 = 12$

$\phi15 = 0$ $\phi51 = 0$ $V3 = 15.83$ $V4 = 15.83$ $V5 = 16$ $i3$

$Lr12 = 5 \times 10^{-7}$ $Lr34 = 5 \times 10^{-9}$ $Lr56 = 4 \times 10^{-7}$ $V6 = 16$

$con13 = 0.807733640009$ $con53 = 0.645866912007$ $con15 = 64.586691200729$

DESIGN VARIABLES

Output Power and output resister

$$P1 := \frac{\phi13 \cdot (\pi - |\phi13|)}{con13} \cdot V12 \cdot V34 + \frac{\phi15 \cdot (x - |\phi15|)}{con15} \cdot V12 \cdot V56$$

$$P2 := \frac{\phi53 \cdot (\pi - |\phi53|)}{con53} \cdot V56 \cdot V34 + \frac{\phi51 \cdot (x - |\phi51|)}{con15} \cdot V12 \cdot V56$$

$$Po := (P1 + P2) \cdot \eta \qquad P\_circulate := \frac{\phi15 \cdot (x - |\phi15|)}{con15} \cdot V12 \cdot V56$$

$$R := \frac{Vo^2}{Po} \qquad R\_notrans := \frac{V34^2}{Po}$$

$P1 = 2.229828850856 \times 10^3$ $P2 = 3.716381418093 \times 10^3$ $Po = 5.351588242054 \times 10^3$

$P\_circulate = 0$ $R\_notrans = 0.187379436728$

$R = 26.982638888889$

Inductor Current

$$I\_dc1 := \frac{P1}{Vin1} \qquad \Delta I1 := Vin1 \cdot \frac{Ts}{2 \cdot Ldc1}$$

$$I\_dc1high := I\_dc1 + \frac{\Delta I1}{2} \qquad I\_dc1low := I\_dc1 - \frac{\Delta I1}{2}$$

$$I\_dc2 := \frac{P2}{Vin2} \qquad \Delta I2 := Vin2 \cdot \frac{Ts}{2 \cdot Ldc2}$$

$$I\_dc2high := I\_dc2 + \frac{\Delta I2}{2} \qquad I\_dc2low := I\_dc2 - \frac{\Delta I2}{2}$$

$$I\_dc2high := I\_dc2 + \frac{}{2} \qquad I\_dc2low := I\_dc2 - \frac{}{2}$$

>>>

I_dc1 = 185.819070904646   I_dc2 = 232.273838630807

ΔI1 = 50 ΔI2 = 66.666666666667

I_dc1high = 210.819070904646   I_dc2high = 265.60717196414

I_dc1low = 160.819070904646   I_dc2low = 198.940505297473

Transformer current

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Initial conditions: Ir13

$$Ir13\_t1 := \frac{(V3 - V1)}{2\omega \cdot Lr13} \cdot (\pi - \phi13) - \frac{(V1 + V4)}{2\omega \cdot Lr13} \cdot \phi13$$

$$Ir13\_t3 := \frac{(V3 - V1)}{2\cdot\omega \cdot Lr13} \cdot (\pi - \phi13) + \frac{(V1 + V4)}{2\omega \cdot Lr13} \cdot \phi13$$

$$Ir13\_t4 := -Ir13\_t1$$

$$Ir13\_t6 := -Ir13\_t3$$

Initial conditions: Ir15

$$Ir15\_t1 := \frac{(V5 - V1)}{2\omega \cdot Lr15} \cdot (\pi - \phi15) - \frac{(V1 + V6)}{2\omega \cdot Lr15} \cdot \phi15$$

$$Ir15\_t2 := \frac{(V5 - V1)}{2\cdot\omega \cdot Lr15} \cdot (\pi - \phi15) + \frac{(V1 + V6)}{2\omega \cdot Lr15} \cdot \phi15$$

$$Ir15\_t4 := -Ir15\_t1$$

$$Ir15\_t5 := -Ir15\_t2$$

Initial conditions: Ir53

$$Ir53\_t2 := \frac{(V3 - V5)}{2\omega \cdot Lr53} \cdot (\pi - \phi53) - \frac{(V5 + V4)}{2\omega \cdot Lr53} \cdot \phi53$$

$$Ir53\_t3 := \frac{(V3 - V5)}{2\cdot\omega \cdot Lr53} \cdot (\pi - \phi53) + \frac{(V5 + V4)}{2\omega \cdot Lr53} \cdot \phi53$$

$$Ir53\_t5 := -Ir53\_t2$$

$$Ir53\_t6 := -Ir53\_t3$$

Mode I: t1-t2

$$ir13(x) := \frac{(V1 + V4)}{\omega \cdot Lr13} \cdot x + Ir13\_t1$$

$$ir53(x) := \frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (x - \pi - \phi13) + Ir53\_t6$$

$$ir15(x) := \frac{(V1 + V6)}{\omega \cdot Lr15} \cdot x + Ir15\_t1$$

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$$Ir53\_t1 := \frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (2\pi - x - \phi13) + Ir53\_t6$$

$$Ir53\_t4 := -Ir53\_t1$$

Mode II: t2-t3

$$ir13(x) := \frac{(V1 + V4)}{\omega \cdot Lr13} \cdot x + Ir13\_t1$$

$$ir53(x) := \frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (x - \phi15) + Ir53\_t2$$

$$ir15(x) := \frac{(V1 - V5)}{\omega \cdot Lr15} \cdot (x - \phi15) + Ir15\_t2$$

$$Ir13\_t2 := \frac{(V1 + V4)}{\omega \cdot Lr13} \cdot \phi15 + Ir13\_t1$$

$$Ir13\_t5 := -Ir13\_t2$$

Mode III: t3-t4

$$ir13(x) := \frac{(V1 - V3)}{\omega \cdot Lr13} \cdot (x - \phi13) + Ir13\_t3$$

$$ir53(x) := \frac{(V5 - V3)}{\omega \cdot Lr53} \cdot (x - \phi13) + Ir53\_t3$$

$$ir15(x) := \frac{(V1 - V5)}{\omega \cdot Lr15} \cdot (x - \phi15) + Ir15\_t2$$

$$ir15(x) := \frac{(V1 - V5)}{\omega \cdot Lr15} \cdot (x - \phi15) + Ir15\_t2$$

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$$ir13\_15 := \frac{}{\omega \cdot Lr15} \cdot (\phi13 - \phi25) + ir13\_12$$

$$Ir15\_t6 := -Ir15\_t3$$

Mode IV: t4-t5

$$ir13(x) := \frac{(-V2 - V3)}{\omega \cdot Lr13} \cdot (x - \pi) + Ir13\_t4$$

$$ir53(x) := \frac{(V5 - V3)}{\omega \cdot Lr53} \cdot (x - \phi13) + Ir53\_t3$$

$$ir15(x) := \frac{(-V2 - V5)}{\omega \cdot Lr15} \cdot (x - \pi) + Ir15\_t4$$

Mode V: t5-t6

$$ir13(x) := \frac{(-V2 - V3)}{\omega \cdot Lr13} \cdot (x - \pi) + Ir13\_t4$$

$$ir53(x) := \frac{(-V6 - V3)}{\omega \cdot Lr53} \cdot (x - \phi15 - \pi) + Ir53\_t5$$

$$ir15(x) := \frac{(-V1 + V6)}{\omega \cdot Lr15} \cdot (x - \phi15 - \pi) + Ir15\_t5$$

Mode VI: t6-t7

$$ir13(x) := \frac{(-V2 + V4)}{\omega \cdot Lr13} \cdot (x - \pi - \phi13) + Ir13\_t6$$

$$ir53(x) := \frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (x - \phi13 - \pi) + Ir53\_t6$$

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$$ir15(x) := \frac{(-V1 + V6)}{\omega \cdot Lr15} \cdot \left(x - \phi15 - x\right) + Ir15\_t5$$

>>

$Ir12\_t1 := Ir13\_t1 + Ir15\_t1$ $\quad Ir12\_t2 := Ir13\_t2 + Ir15\_t2$ $\quad Ir12\_t3 := Ir13\_t3 + Ir15\_t3$

$Ir12\_t4 := Ir13\_t4 + Ir15\_t4$ $\quad Ir12\_t5 := Ir13\_t5 + Ir15\_t5$ $\quad Ir12\_t6 := Ir13\_t6 + Ir15\_t6$

$Ir56\_t1 := Ir53\_t1 - Ir15\_t1$ $\quad Ir56\_t2 := Ir53\_t2 - Ir15\_t2$ $\quad Ir56\_t3 := Ir53\_t3 - Ir15\_t3$

$Ir56\_t4 := Ir53\_t4 - Ir15\_t4$ $\quad Ir56\_t5 := Ir53\_t5 - Ir15\_t5$ $\quad Ir56\_t6 := Ir53\_t6 - Ir15\_t6$

$Ir34\_t1 := Ir13\_t1 + Ir53\_t1$ $\quad Ir34\_t2 := Ir13\_t2 + Ir53\_t2$ $\quad Ir34\_t3 := Ir13\_t3 + Ir53\_t3$

$Ir34\_t4 := Ir13\_t4 + Ir53\_t4$ $\quad Ir34\_t5 := Ir13\_t5 + Ir53\_t5$ $\quad Ir34\_t6 := Ir13\_t6 + Ir53\_t6$

$$
\begin{pmatrix}
Ir13\_t1 & Ir13\_t2 & Ir13\_t3 & Ir13\_t4 & Ir13\_t5 & Ir13\_t6 \\
Ir15\_t1 & Ir15\_t2 & Ir15\_t3 & Ir15\_t4 & Ir15\_t5 & Ir15\_t6 \\
Ir53\_t1 & Ir53\_t2 & Ir53\_t3 & Ir53\_t4 & Ir53\_t5 & Ir53\_t6 \\
Ir12\_t1 & Ir12\_t2 & Ir12\_t3 & Ir12\_t4 & Ir12\_t5 & Ir12\_t6 \\
Ir56\_t1 & Ir56\_t2 & Ir56\_t3 & Ir56\_t4 & Ir56\_t5 & Ir56\_t6 \\
Ir34\_t1 & Ir34\_t2 & Ir34\_t3 & Ir34\_t4 & Ir34\_t5 & Ir34\_t6
\end{pmatrix}
=
\begin{pmatrix}
-215.973920130399 & -215.973920130399 & 328.4 \\
1.222493887531 & 1.222493887531 & 0.24 \\
-392.216788916056 & -392.216788916055 & 386.1 \\
-214.751426242869 & -214.751426242869 & 328.6 \\
-393.439282803586 & -393.439282803586 & 385.3 \\
-608.19070946455 & -608.19070946455 & 714.2
\end{pmatrix}
$$

$$t1 := 0 \qquad t2 := \phi15\frac{Ts}{2 \cdot \pi} \qquad t3 := \phi13\frac{Ts}{2 \cdot \pi} \qquad t4 := \frac{Ts}{2}$$

$$t5 := (\pi + \phi15)\frac{Ts}{2 \cdot \pi} \qquad t6 := (\pi + \phi13)\frac{Ts}{2 \cdot \pi} \qquad t7 := Ts$$

$$
time := \begin{pmatrix} t1 \\ t2 \\ t3 \\ t4 \\ t5 \\ t6 \\ t7 \end{pmatrix}
\qquad
Ir13 := \begin{pmatrix} Ir13\_t1 \\ Ir13\_t2 \\ Ir13\_t3 \\ Ir13\_t4 \\ Ir13\_t5 \\ Ir13\_t6 \\ Ir13\_t1 \end{pmatrix}
\qquad
Ir15 := \begin{pmatrix} Ir15\_t1 \\ Ir15\_t2 \\ Ir15\_t3 \\ Ir15\_t4 \\ Ir15\_t5 \\ Ir15\_t6 \\ Ir15\_t1 \end{pmatrix}
\qquad
Ir53 := \begin{pmatrix} Ir53\_t1 \\ Ir53\_t2 \\ Ir53\_t3 \\ Ir53\_t4 \\ Ir53\_t5 \\ Ir53\_t6 \\ Ir53\_t1 \end{pmatrix}
$$

$$\text{Ir12} := \begin{pmatrix} \text{Ir12\_t1} \\ \text{Ir12\_t2} \\ \text{Ir12\_t3} \\ \text{Ir12\_t4} \\ \text{Ir12\_t5} \\ \text{Ir12\_t6} \\ \text{Ir12\_t1} \end{pmatrix} \qquad \text{Ir56} := \begin{pmatrix} \text{Ir56\_t1} \\ \text{Ir56\_t2} \\ \text{Ir56\_t3} \\ \text{Ir56\_t4} \\ \text{Ir56\_t5} \\ \text{Ir56\_t6} \\ \text{Ir56\_t1} \end{pmatrix} \qquad \text{Ir34} := \begin{pmatrix} \text{Ir34\_t1} \\ \text{Ir34\_t2} \\ \text{Ir34\_t3} \\ \text{Ir34\_t4} \\ \text{Ir34\_t5} \\ \text{Ir34\_t6} \\ \text{Ir34\_t1} \end{pmatrix}$$

Soft switching conditions

$$\text{f\_s1} := \text{I\_dc1} - \text{Ir12\_t1} \qquad \text{f\_s2} := \text{Ir12\_t4} - \text{I\_dc1} \qquad \text{f\_s3} := \text{Ir34\_t3}$$

$$\text{f\_s4} := -\text{Ir34\_t6} \qquad \text{f\_s5} := \text{I\_dc2} - \text{Ir56\_t2} \qquad \text{f\_s6} := \text{Ir56\_t5} - \text{I\_dc2}$$

$$\text{device} := \begin{pmatrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{pmatrix} \qquad \text{soft\_switching} := \begin{pmatrix} \text{f\_s1} \\ \text{f\_s2} \\ \text{f\_s3} \\ \text{f\_s4} \\ \text{f\_s5} \\ \text{f\_s6} \end{pmatrix}$$

RMS current for devices

Device S1

$$IS1\_2rms := \frac{1}{2 \cdot \pi} \left[\int_0^{\phi15} \left[\left[\frac{(V1 + V4)}{\omega \cdot Lr13} x + Ir13\_t1 \ldots \right. \right. \right. \\ \left. \left. \left. + \frac{(V1 + V6)}{\omega \cdot Lr15} x + Ir15\_t1 \right] - I\_dc1 \right]^2 dx \ldots \right. \\ \left. + \int_{\phi15}^{\phi13} \left[\left[\frac{(V1 + V4)}{\omega \cdot Lr13} x + Ir13\_t1 \ldots \right. \right. \right. \\ \left. \left. \left. + \frac{(V1 - V5)}{\omega \cdot Lr15} \cdot (x - \phi15) + Ir15\_t2 \right] - I\_dc1 \right]^2 dx \ldots \right. \\ \left. + \int_{\phi13}^{\pi} \left[\left[\frac{(V1 - V3)}{\omega \cdot Lr13} \cdot (x - \phi13) + Ir13\_t3 \ldots \right. \right. \right. \\ \left. \left. \left. + \frac{(V1 - V5)}{\omega \cdot Lr15} \cdot (x - \phi15) + Ir15\_t2 \right] - I\_dc1 \right]^2 dx \right]$$

$IS1\_rms := \sqrt{IS1\_2rms}$ $\qquad$ $IS1\_rms = 103.83074206391$

$IS1\_peak := Ir12\_t3 - I\_dc1$ $\qquad$ $IS1\_peak = 142.868785656072$

$ID1\_peak := Ir12\_t1 - I\_dc1$ $\qquad$ $ID1\_peak = -400.570497147514$

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Device S2

$$IS2\_2rms := \frac{1}{2 \cdot \pi} \left[\int_{\pi}^{\pi+\phi15} \left[I\_do1 - \left[\frac{(-V2-V3)}{\omega \cdot Lr13}(x-\pi) + Ir13\_t4 \right] \dots \right. \right.$$
$$\left. + \frac{-(-V2-V5)}{\omega \cdot Lr15}(x-\pi) + -Ir15\_t4 \right]^2 dx \dots$$

$$+ \int_{\pi+\phi15}^{\pi+\phi13} \left[I\_do1 - \left[\frac{(-V2-V3)}{\omega \cdot Lr13}(x-\pi) + Ir13\_t4 \right] \dots \right.$$
$$\left. + \frac{-(-V1+V6)}{\omega \cdot Lr15}(x-\phi15-\pi) + -Ir15\_t5 \right]^2 dx \dots$$

$$+ \int_{\pi+\phi13}^{2\pi} \left[I\_do1 - \left[\frac{(-V2+V4)}{\omega \cdot Lr13}(x-\pi-\phi13) + Ir13\_t6 \right] \dots \right.$$
$$\left. \left. + \frac{(V1-V6)}{\omega \cdot Lr15}(x-\phi15-\pi) + -Ir15\_t5 \right]^2 dx \right]$$

Device S3

$$IS3\_2rms := \frac{1}{2 \cdot \pi} \left[\int_{\phi13}^{\pi} \left[\frac{(V1-V3)}{\omega \cdot Lr13}(x-\phi13) + Ir13\_t3 \dots \right. \right.$$
$$\left. + \frac{(V5-V3)}{\omega \cdot Lr53}(x-\phi13) + Ir53\_t3 \right]^2 dx \dots$$

$$+ \int_{\pi}^{\pi+\phi15} \left[\frac{(-V2-V3)}{\omega \cdot Lr13}(x-\pi) + Ir13\_t4 \dots \right.$$
$$\left. + \frac{(V5-V3)}{\omega \cdot Lr53}(x-\phi13) + Ir53\_t3 \right]^2 dx \dots$$

$$+ \int_{\pi+\phi15}^{\pi+\phi13} \left[\frac{(-V2-V3)}{\omega \cdot Lr13}(x-\pi) + Ir13\_t4 \dots \right.$$
$$\left. \left. + \frac{(-V6-V3)}{\omega \cdot Lr53}(x-\phi15-\pi) + Ir53\_t5 \right]^2 dx \right]$$

>>

$IS2\_rms := \sqrt{IS2\_2rms}$　　　　$IS2\_rms = 282.556679661397$

$IS2\_peak := I\_dc1 - Ir12\_t1$　　　　$IS2\_peak = 400.570497147514$

$ID2\_peak := I\_dc1 - Ir12\_t3$　　　　$ID2\_peak = -142.868785656072$

$IS3\_rms := \dfrac{\sqrt{IS3\_2rms}}{n}$　　　　$IS3\_rms = 33.461395898072$

$IS3\_peak := \dfrac{Ir34\_t3}{n}$　　　　$IS3\_peak = 59.545639771801$

$ID3\_peak := \dfrac{Ir34\_t1}{n}$　　　　$ID3\_peak = -50.682559087205$

>>

Device S5

$$IS5\_2rms := \frac{1}{2 \cdot \pi}\left[\int_{\phi15}^{\phi13}\left[\left[\frac{(-V6 + V4)}{\omega \cdot Lr53}(x - \phi15) + Ir53\_t2\ ... \atop + \frac{-(V1 - V5)}{\omega \cdot Lr15}(x - \phi15) + -Ir15\_t2\right] - I\_dc2\right]^2 dx\ ...\right.$$

$$+ \int_{\phi13}^{\pi}\left[\left[\frac{(V5 - V3)}{\omega \cdot Lr53}(x - \phi13) + Ir53\_t3\ ... \atop + \frac{-(V1 - V5)}{\omega \cdot Lr15}(x - \phi15) + -Ir15\_t2\right] - I\_dc2\right]^2 dx\ ...$$

$$\left. + \int_{\pi}^{\pi+\phi15}\left[\left[\frac{(V5 - V3)}{\omega \cdot Lr53}(x - \phi13) + Ir53\_t3\ ... \atop + \frac{(-V2 - V5)}{\omega \cdot Lr15}(x - \pi) + -Ir15\_t4\right] - I\_dc2\right]^2 dx\right.$$

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Device S6

$$IS6\_2rms := \frac{1}{2 \cdot \pi} \cdot \left[\int_{\pi+\phi15}^{\pi+\phi13} \left[I\_dc2 - \left[\frac{(-V6 - V3)}{\omega \cdot Lr53} \cdot (x - \phi15 - x) + Ir53\_t5 \right] \dots \atop + \frac{(-V1 + V6)}{\omega \cdot Lr15} \cdot (x - \phi15 - \pi) + Ir15\_t5 \right]^2 dx \dots \right.$$

$$+ \int_{\pi+\phi13}^{2\pi} \left[I\_dc2 - \left[\frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (x - \phi13 - x) + Ir53\_t6 \right] \dots \atop + \frac{(-V1 + V6)}{\omega \cdot Lr15} \cdot (x - \phi15 - \pi) + Ir15\_t5 \right]^2 dx \dots$$

$$\left. + \int_{0}^{\phi15} \left[I\_dc2 - \left[\frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (x - \pi - \phi13) + Ir53\_t6 \right] \dots \atop + \frac{(V1 + V6)}{\omega \cdot Lr15} \cdot x + Ir15\_t1 \right]^2 dx \right]$$

>>

$IS5\_rms := \sqrt{IS5\_2rms}$ $\quad$ $IS5\_rms = 293.467471771213$

$IS5\_peak := Ir56\_t5 - I\_dc2$ $\quad$ $IS5\_peak = 161.165444172779$

$ID5\_peak := Ir56\_t2 - I\_dc2$ $\quad$ $ID5\_peak = -625.713121434393$

$IS6\_rms := \sqrt{IS6\_2rms}$ $\quad$ $IS6\_rms = 369.595494588069$

$IS6\_peak := I\_dc2 - Ir56\_t6$ $\quad$ $IS6\_peak = 618.133659331703$

$ID6\_peak := I\_dc2 - Ir56\_t5$ $\quad$ $ID6\_peak = -161.165444172779$

>>>

$IS4\_rms := IS3\_rms$ $\qquad$ $IS4\_peak := IS3\_peak$ $\qquad$ $ID4\_peak := ID3\_peak$

$$
devices := \begin{pmatrix} 0 \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \end{pmatrix}
\qquad
currentP := \begin{pmatrix} 0 \\ IS1\_peak \\ IS2\_peak \\ IS3\_peak \\ IS4\_peak \\ IS5\_peak \\ IS6\_peak \\ 0 \end{pmatrix}
$$

$$
currentD := \begin{pmatrix} 0 \\ -ID1\_peak \\ -ID2\_peak \\ -ID3\_peak \\ -ID4\_peak \\ -ID5\_peak \\ -ID6\_peak \\ 0 \end{pmatrix}
\qquad
currentR := \begin{pmatrix} 0 \\ IS1\_rms \\ IS2\_rms \\ IS3\_rms \\ IS4\_rms \\ IS5\_rms \\ IS6\_rms \\ 0 \end{pmatrix}
$$

****

SUMMARY OF DESIGN REPORT

****

$Vin1 = 12$ $Vin2 = 16$ $fs := 20 \cdot 10^3$ $D := .5$ $n := 12$

$Ldc1 = 6 \times 10^{-6}$ $Ldc2 = 6 \times 10^{-6}$

$Lr13 = 5.1125 \times 10^{-7}$ $Lr15 = 4.09 \times 10^{-5}$

$Lr53 = 4.09 \times 10^{-7}$

$Lr12 = 5 \times 10^{-7}$ $Lr34 = 5 \times 10^{-9}$ $Lr56 = 4 \times 10^{-7}$

$\phi13 = 1.256637061436$ $\phi53 = 1.256637061436$ $\phi15 = 0$

$V12 = 24$ $V34 = 31.666666$ $V56 = 32$ $Vo = 380$

$V1 = 12$ $V2 = 12$ $V3 = 15.83$ $V4 = 15.8333$ $V5 = 16$ $V6 = 16$

$con13 = 0.807333640009$ $con53 = 0.645866912007$ $con15 = 64.586691200729$

$>>>$

$P1 = 2.229828850856 \times 1$ $P2 = 3.716381418093 \times 10^3$ $Po = 5.351589242054 \times 10^3$

$P\_circulate = 0$ $R = 26.982638888889$

                                  $R\_notrans = 0.187379436728$

$>>>$

$I\_dc1 = 185.819070904646$ $I\_dc2 = 232.273838630807$

$\Delta I1 = 50$ $\Delta I2 = 66.66666666667$

$I\_dc1high = 210.819070904646$ $I\_dc2high = 265.60717196414$

$I\_dc1low = 160.819070904646$ $I\_dc2low = 198.940505297473$

$>>>$

$$
\begin{pmatrix}
\text{Ir13\_t1} & \text{Ir13\_t2} & \text{Ir13\_t3} & \text{Ir13\_t4} & \text{Ir13\_t5} & \text{Ir13\_t6} \\
\text{Ir15\_t1} & \text{Ir15\_t2} & \text{Ir15\_t3} & \text{Ir15\_t4} & \text{Ir15\_t5} & \text{Ir15\_t6} \\
\text{Ir53\_t1} & \text{Ir53\_t2} & \text{Ir53\_t3} & \text{Ir53\_t4} & \text{Ir53\_t5} & \text{Ir53\_t6} \\
\text{Ir12\_t1} & \text{Ir12\_t2} & \text{Ir12\_t3} & \text{Ir12\_t4} & \text{Ir12\_t5} & \text{Ir12\_t6} \\
\text{Ir56\_t1} & \text{Ir56\_t2} & \text{Ir56\_t3} & \text{Ir56\_t4} & \text{Ir56\_t5} & \text{Ir56\_t6} \\
\text{Ir34\_t1} & \text{Ir34\_t2} & \text{Ir34\_t3} & \text{Ir34\_t4} & \text{Ir34\_t5} & \text{Ir34\_t6}
\end{pmatrix}
=
\begin{pmatrix}
-215.973920130399 & -215.973920130399 & 328.4 \\
1.222493887531 & 1.222493887531 & 0.24 \\
-392.216788916056 & -392.216788916055 & 386.1 \\
-214.751426242869 & -214.751426242869 & 328.6 \\
-393.439282803586 & -393.439282803586 & 385.3 \\
-608.19070904655 & -608.19070904655 & 714.5
\end{pmatrix}
$$

$$
\text{currentD} =
\begin{pmatrix}
0 \\
400.57049714751 \\
142.8687856607 \\
50.68255908720 \\
50.68255908720 \\
625.71312143439 \\
161.16544417277 \\
0
\end{pmatrix}
\quad
\text{currentP} =
\begin{pmatrix}
0 \\
142.8687856607 \\
400.57049714751 \\
59.545639771801 \\
59.545639771801 \\
161.16544417277 \\
618.13365933170 \\
0
\end{pmatrix}
\quad
\text{currentR} =
\begin{pmatrix}
0 \\
103.83074206391 \\
282.55667966197 \\
33.461395898072 \\
33.461395898072 \\
293.467471771213 \\
369.595494588069 \\
0
\end{pmatrix}
$$

$$
\text{soft\_switching} =
\begin{pmatrix}
400.570497147514 \\
28.932355338223 \\
714.547677261614 \\
714.547677261614 \\
625.713121434393 \\
161.165444172779
\end{pmatrix}
$$

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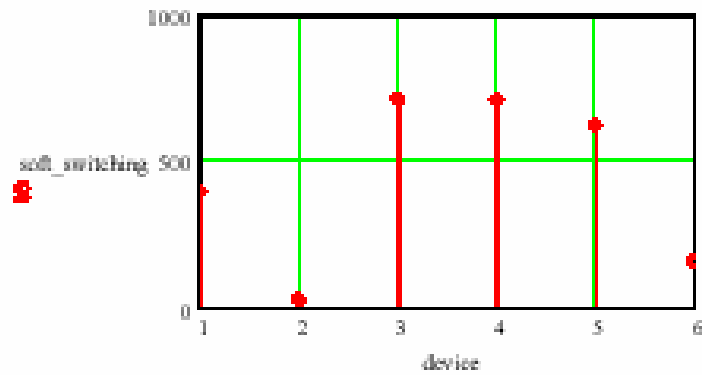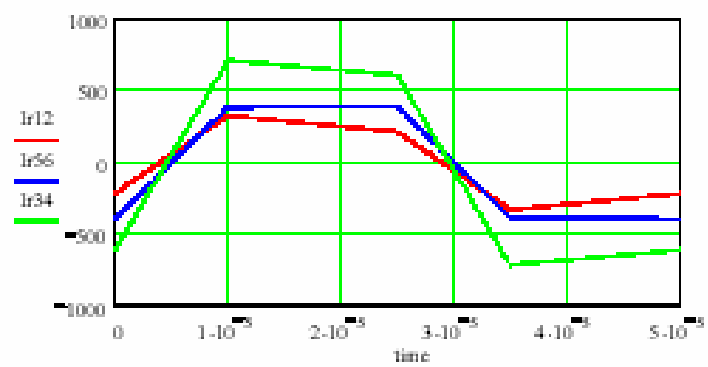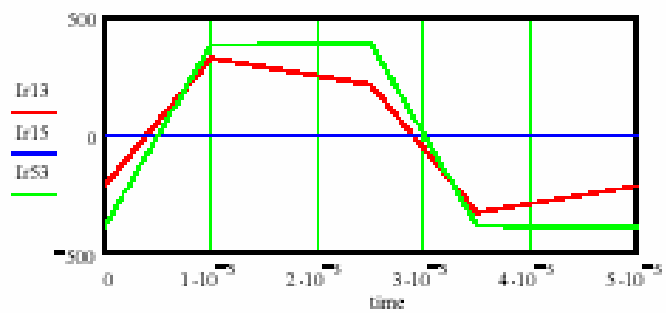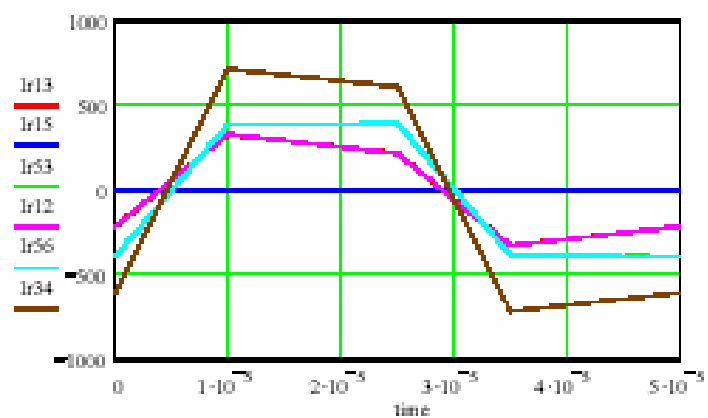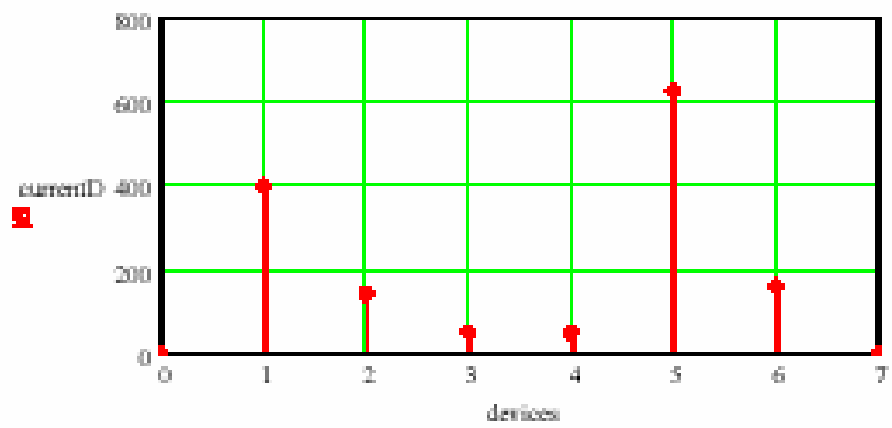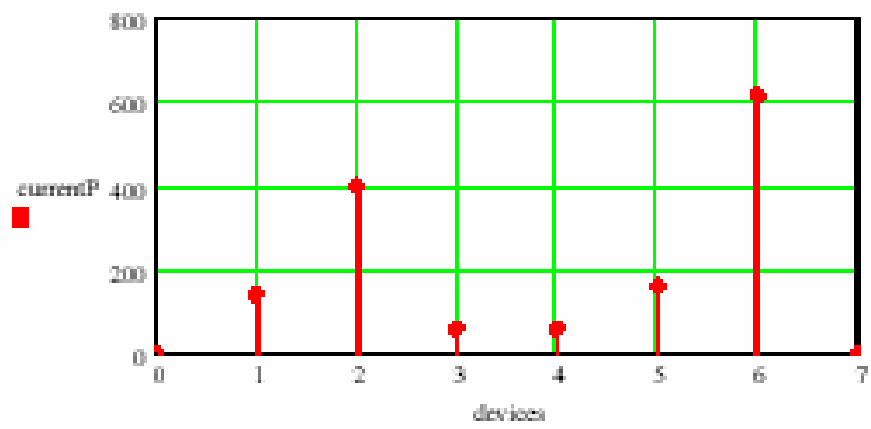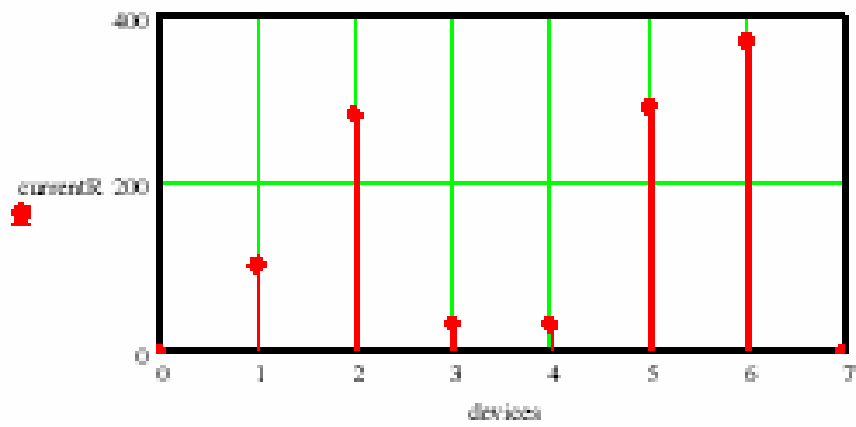
$$\text{Ir12\_2rms\_1} := \frac{1}{2\cdot\pi}\cdot\left[\int_{0}^{\phi15}\left[\left[\frac{(V1+V4)}{\omega\cdot Lr13}\cdot x + Ir13\_t1 \dots \atop +\frac{(V1+V6)}{\omega\cdot Lr15}\cdot x + Ir15\_t1\right]\right]^{2} dx \dots\right.$$

$$+\int_{\phi15}^{\phi13}\left[\left[\frac{(V1+V4)}{\omega\cdot Lr13}\cdot x + Ir13\_t1 \dots \atop +\frac{(V1-V5)}{\omega\cdot Lr15}\cdot(x-\phi15) + Ir15\_t2\right]\right]^{2} dx \dots$$

$$\left.+\int_{\phi13}^{\pi}\left[\left[\frac{(V1-V3)}{\omega\cdot Lr13}\cdot(x-\phi13) + Ir13\_t3 \dots \atop +\frac{(V1-V5)}{\omega\cdot Lr15}\cdot(x-\phi15) + Ir15\_t2\right]\right]^{2} dx\right]$$

$$\text{Ir12\_2rms\_2} := \frac{1}{2\cdot\pi}\cdot\left[\int_{\pi}^{\pi+\phi15}\left[\left[\frac{(-V2-V3)}{\omega\cdot Lr13}\cdot(x-\pi) + Ir13\_t4\right] \dots \atop +\frac{(-V2-V5)}{\omega\cdot Lr15}\cdot(x-\pi) + Ir15\_t4\right]^{2} dx \dots\right.$$

$$+\int_{\pi+\phi15}^{\pi+\phi13}\left[\left[\frac{(-V2-V3)}{\omega\cdot Lr13}\cdot(x-\pi) + Ir13\_t4\right] \dots \atop +\frac{(-V1+V6)}{\omega\cdot Lr15}\cdot(x-\phi15-\pi) + Ir15\_t5\right]^{2} dx \dots$$

$$\left.+\int_{\pi+\phi13}^{2\pi}\left[\left[\frac{(-V2+V4)}{\omega\cdot Lr13}\cdot(x-\pi-\phi13) + Ir13\_t6\right] \dots \atop +\frac{(V6-V1)}{\omega\cdot Lr15}\cdot(x-\phi15-\pi) + Ir15\_t5\right]^{2} dx\right]$$

$$\text{Ir12\_2rms} := \text{Ir12\_2rms\_1} + \text{Ir12\_2rms\_2}$$

$$\text{Ir12\_rms} := \sqrt{\text{Ir12\_2rms}}$$

$$\text{Ir12\_rms} = 236.834062387466$$

$$\text{Ir56\_2rms\_1} := \frac{1}{2 \cdot \pi} \left[\int_{\phi15}^{\phi13} \left[\left[\frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (x - \phi15) + \text{Ir53\_t2} \ldots \atop + \frac{-(V1 - V5)}{\omega \cdot Lr15} \cdot (x - \phi15) + -\text{Ir15\_t2} \right] \right]^2 dx \ldots \right.$$

$$+ \int_{\phi13}^{\pi} \left[\left[\frac{(V5 - V3)}{\omega \cdot Lr53} \cdot (x - \phi13) + \text{Ir53\_t3} \ldots \atop + \frac{-(V1 - V5)}{\omega \cdot Lr15} \cdot (x - \phi15) + -\text{Ir15\_t2} \right] \right]^2 dx \ldots$$

$$\left. + \int_{\pi}^{\pi+\phi15} \left[\left[\frac{(V5 - V3)}{\omega \cdot Lr53} \cdot (x - \phi13) + \text{Ir53\_t3} \ldots \atop + \frac{-(-V2 - V5)}{\omega \cdot Lr15} \cdot (x - x) + -\text{Ir15\_t4} \right] \right]^2 dx \right]$$

Device S6

$$\text{Ir56\_2rms\_2} := \frac{1}{2 \cdot \pi} \left[\int_{\pi+\phi15}^{\pi+\phi13} \left[\frac{(-V6 - V3)}{\omega \cdot Lr53} \cdot (x - \phi15 - \pi) + \text{Ir53\_t5} \ldots \atop + \frac{(V1 - V6)}{\omega \cdot Lr15} \cdot (x - \phi15 - \pi) + -\text{Ir15\_t5} \right]^2 dx \ldots \right.$$

$$+ \int_{\pi+\phi13}^{2\pi} \left[\frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (x - \phi13 - \pi) + \text{Ir53\_t6} \ldots \atop + \frac{(V1 - V6)}{\omega \cdot Lr15} \cdot (x - \phi15 - \pi) + -\text{Ir15\_t5} \right]^2 dx \ldots$$

$$\left. + \int_{0}^{\phi15} \left[\frac{(-V6 + V4)}{\omega \cdot Lr53} \cdot (x - \pi - \phi13) + \text{Ir53\_t6} \ldots \atop + \frac{-(V1 + V6)}{\omega \cdot Lr15} \cdot x + -\text{Ir15\_t1} \right]^2 dx \right]$$
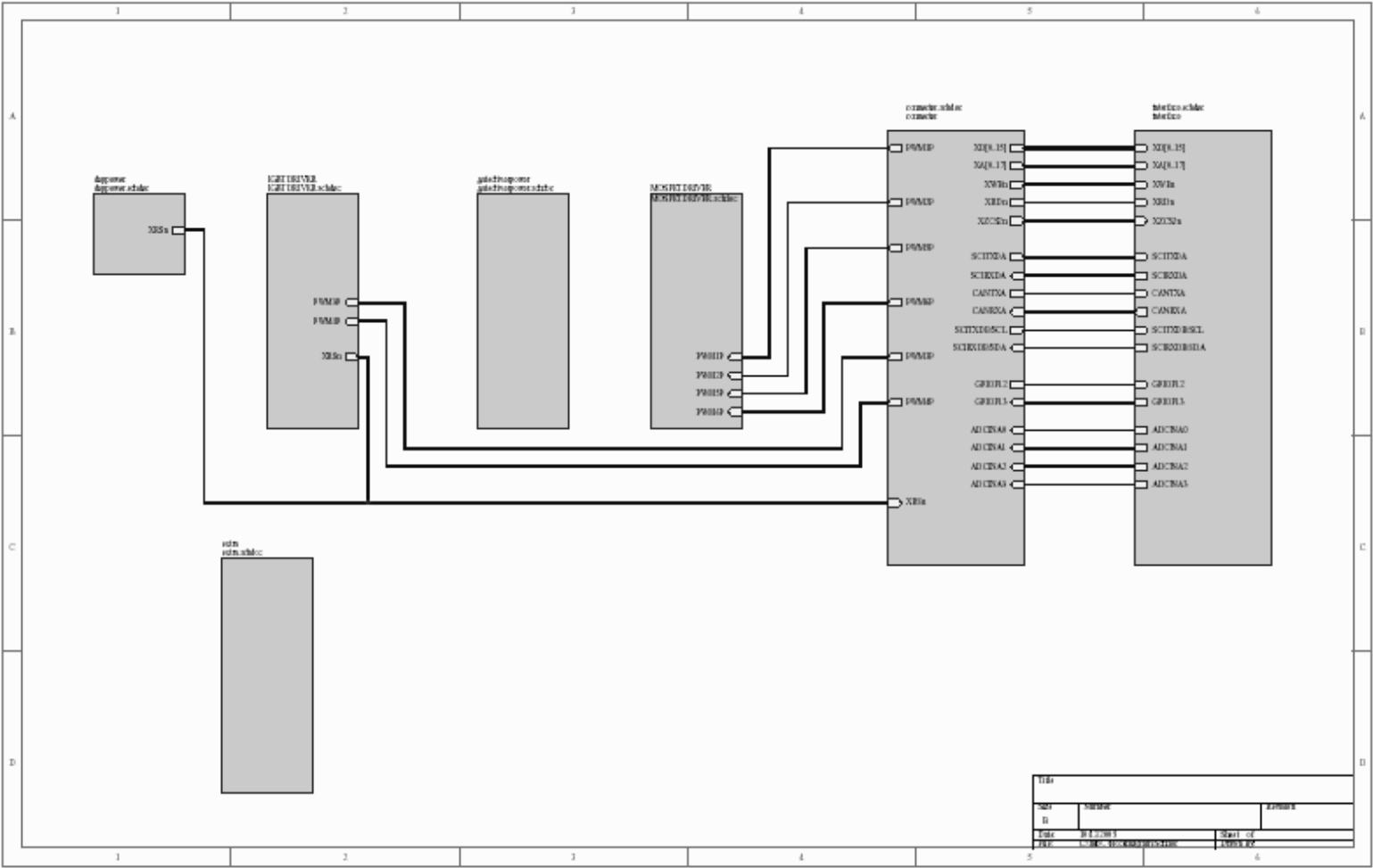
$$\text{Ir56\_2rms} := \text{Ir56\_2rms\_1} + \text{Ir56\_2rms\_2}$$

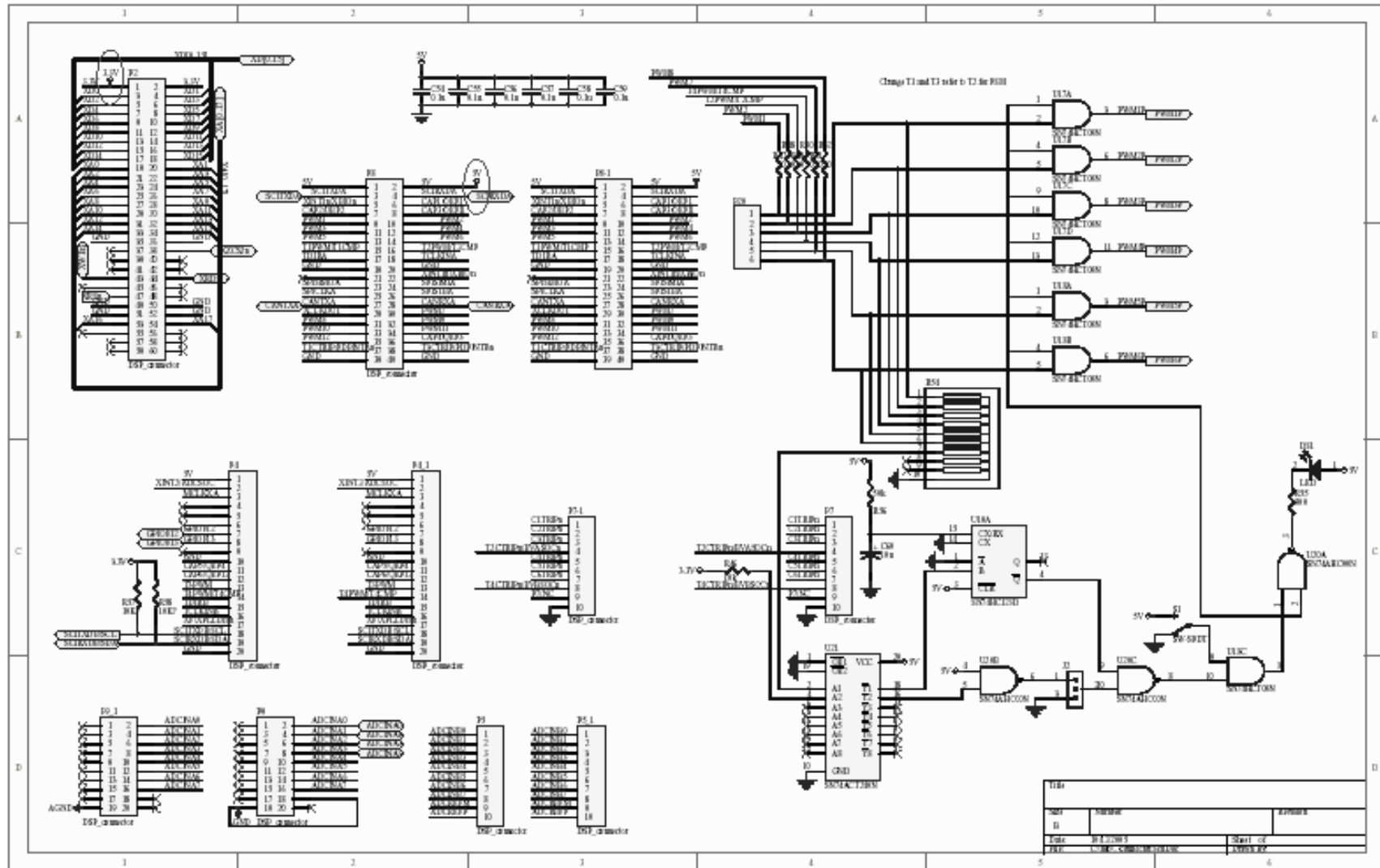$$\text{Ir56\_rms} := \sqrt{\text{Ir56\_2rms}}$$

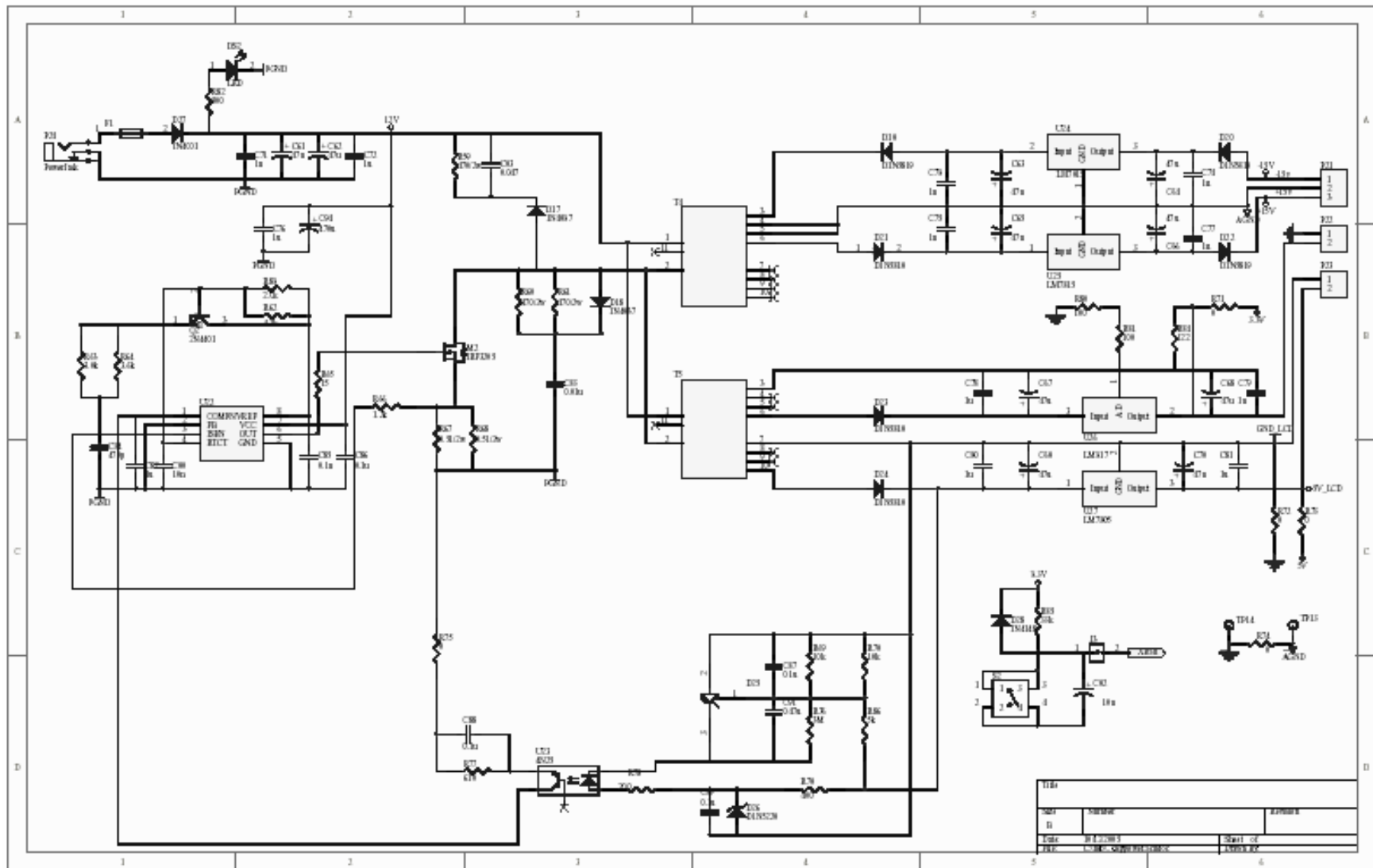$$\text{Ir56\_rms} = 363.904962808273$$

APPENDIX B: CIRCUIT SCHEMATICS

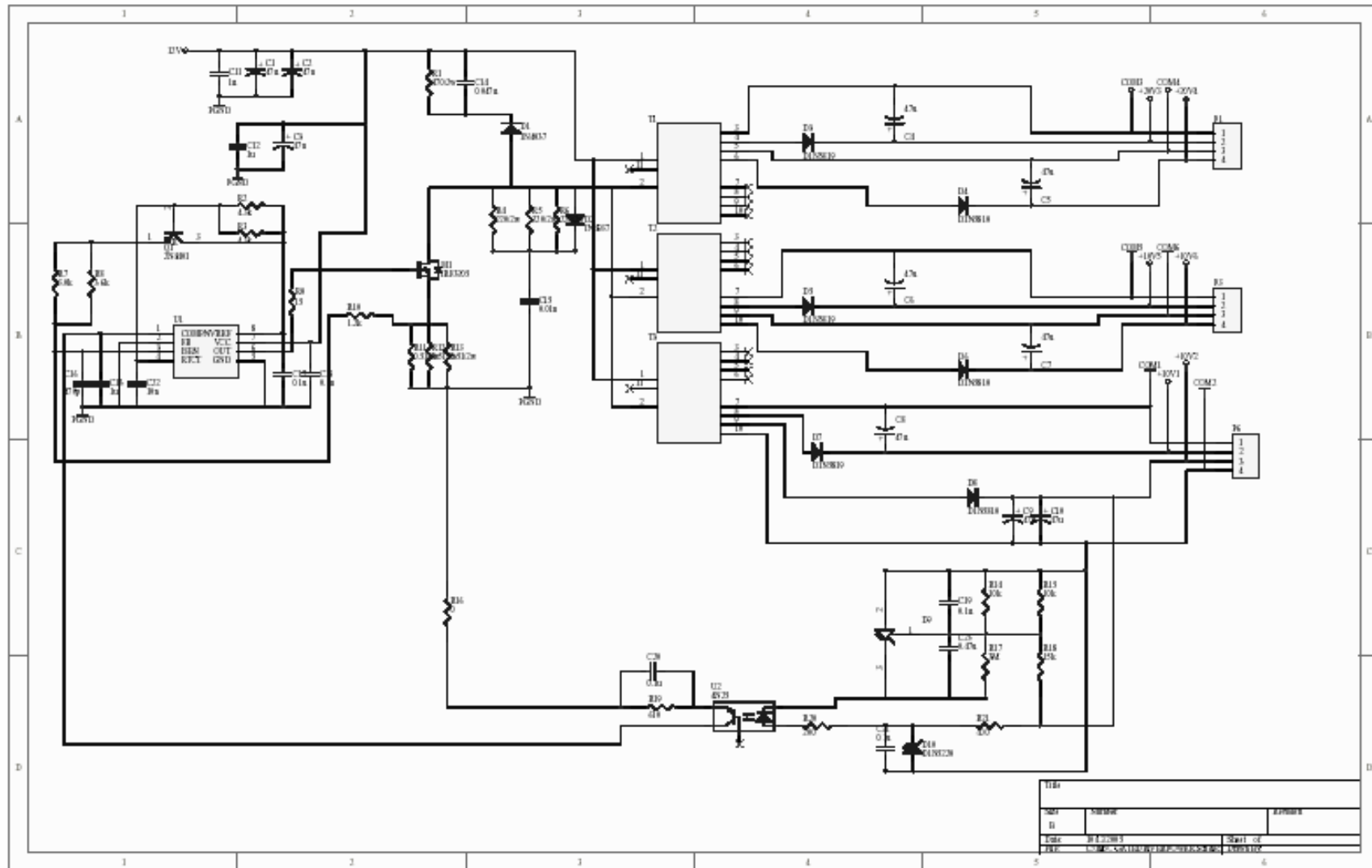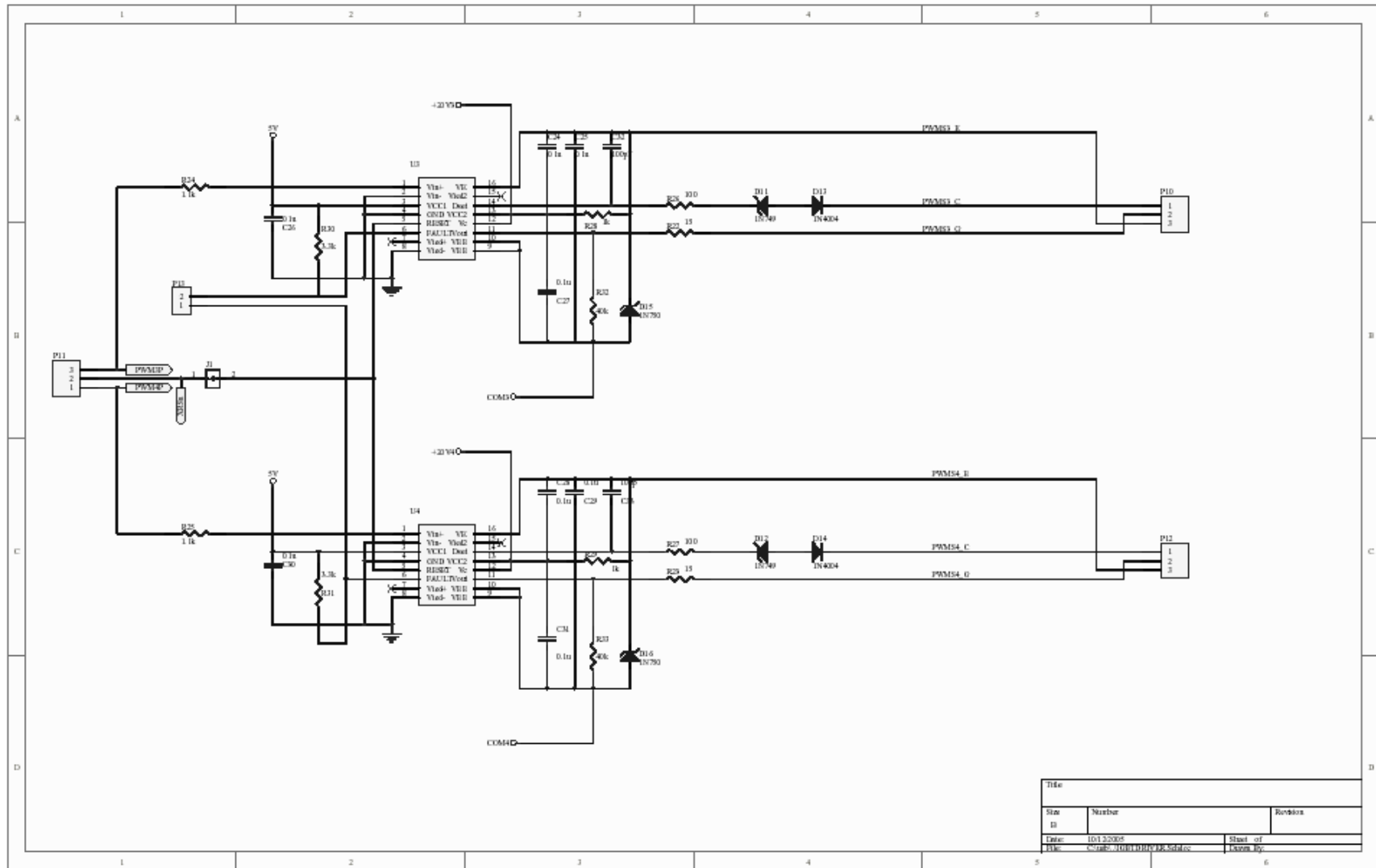## 1. CIRCUIT BLOCK DIAGRAM

2. CONNECTOR CIRCUIT

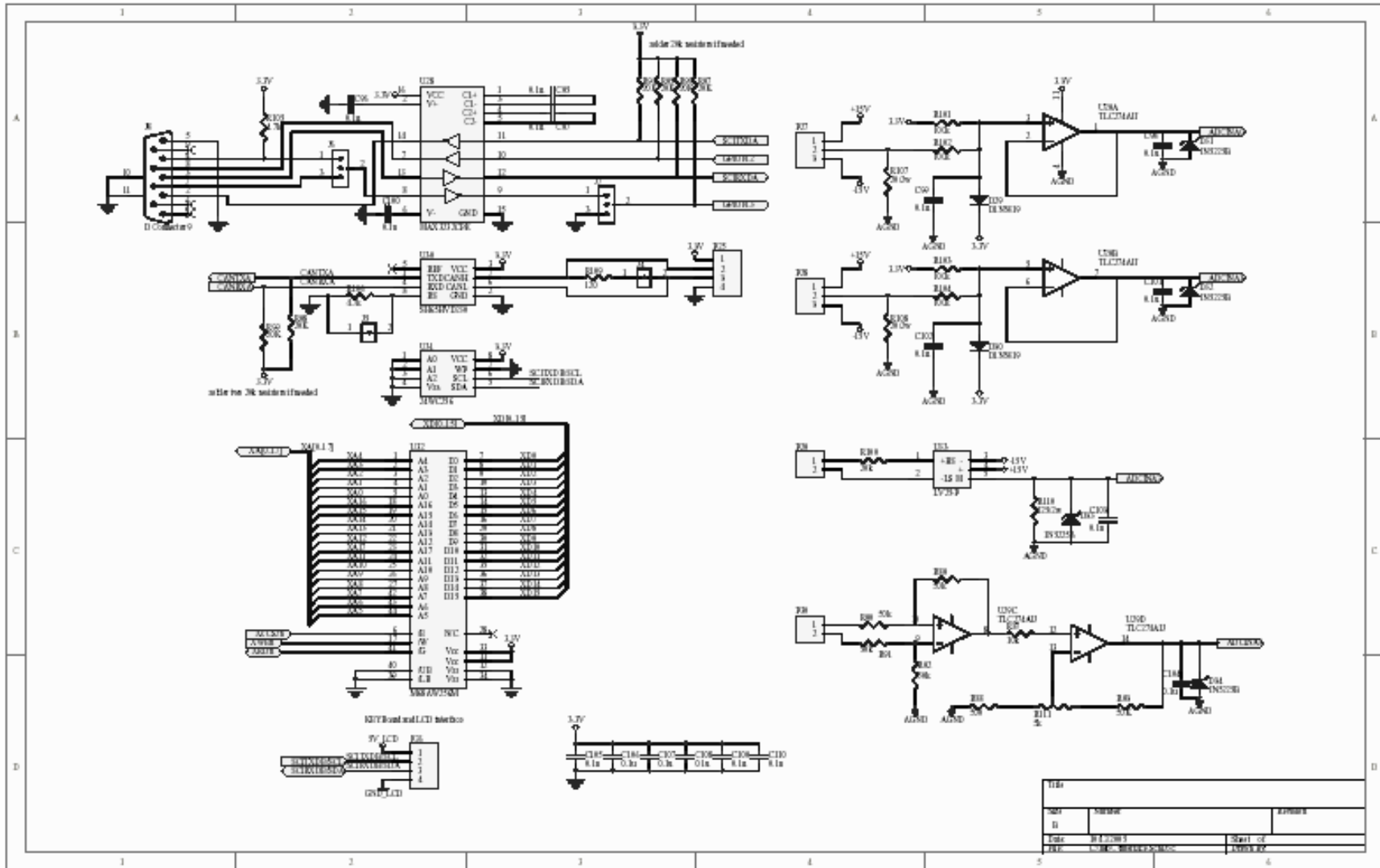# 3. AUXILIARY CONTROL POWER CIRCUIT FOR DSP

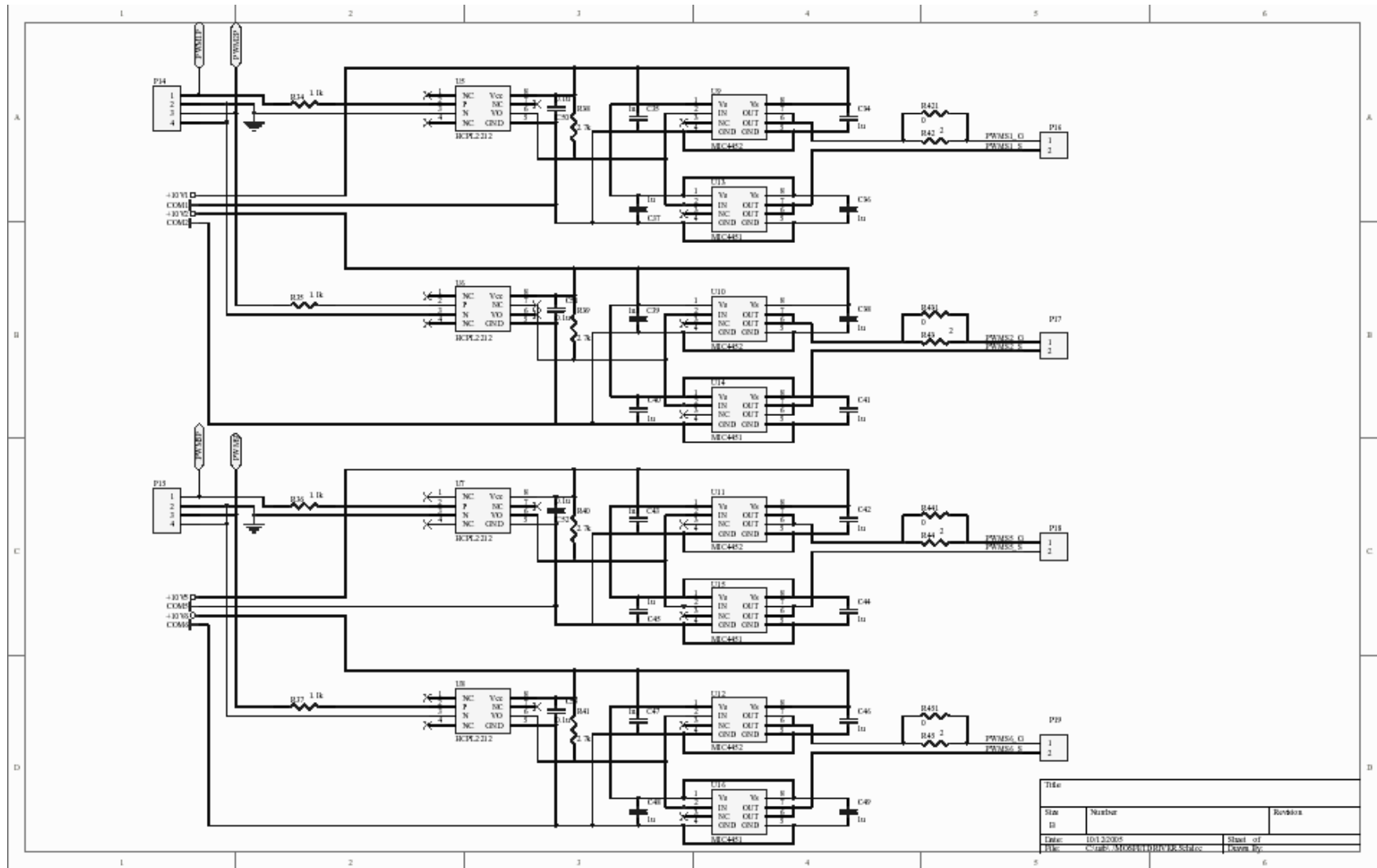## 4. AUXILIARY CONTROL POWER CIRCUIT FOR GATE DRIVERS

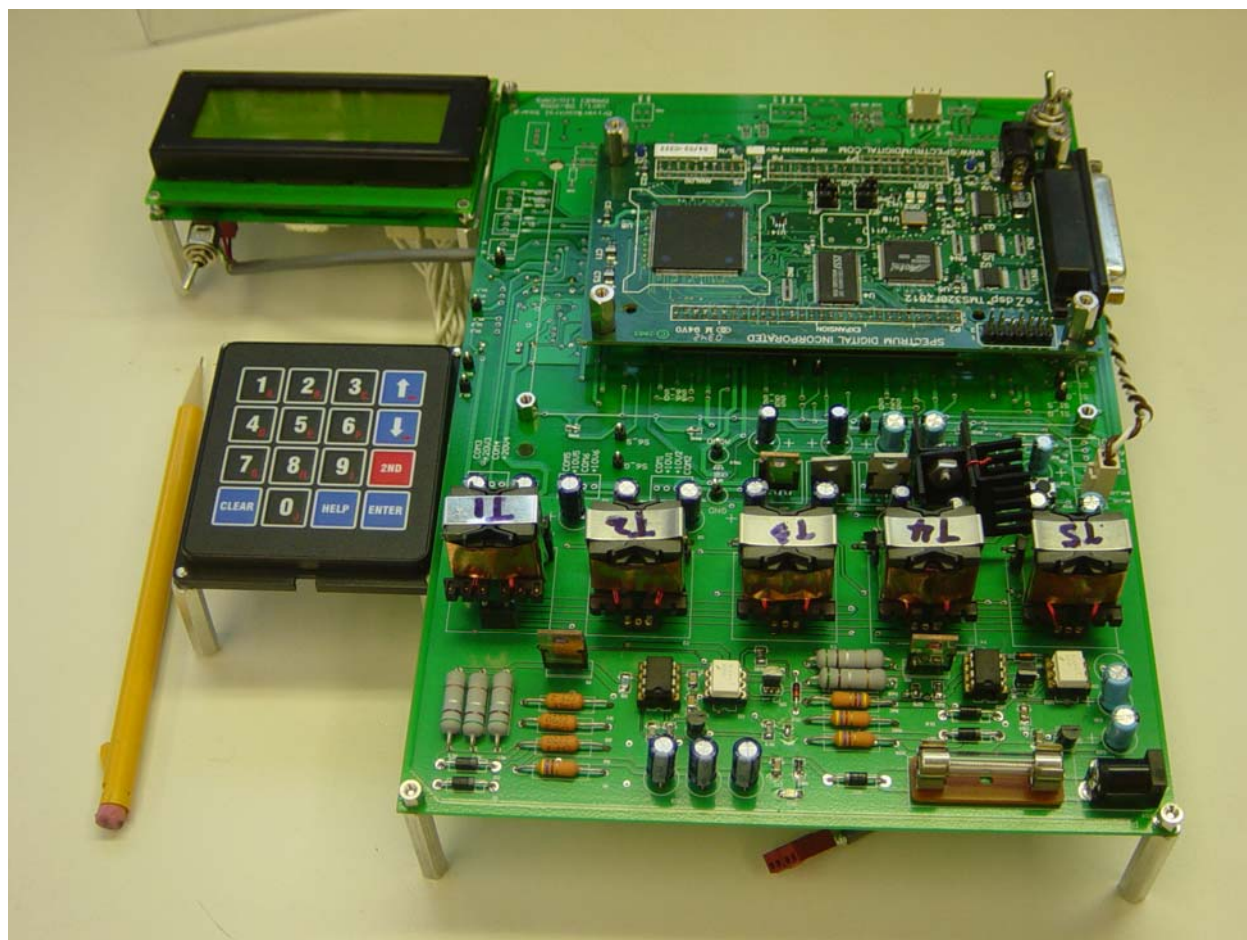## 5. IGBT DRIVER

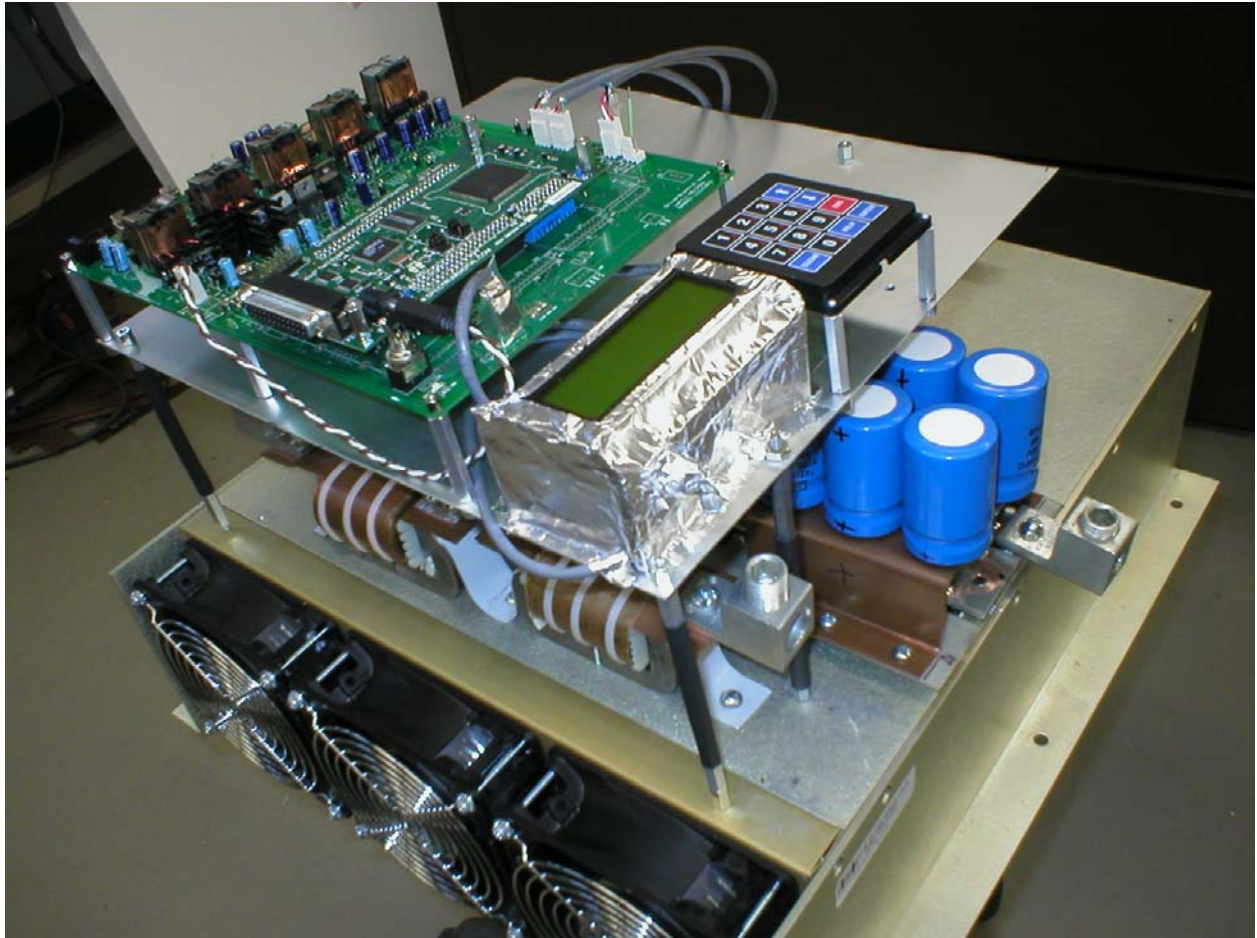# 6. INTERFACE CIRCUIT

7. MOSFET DRIVER
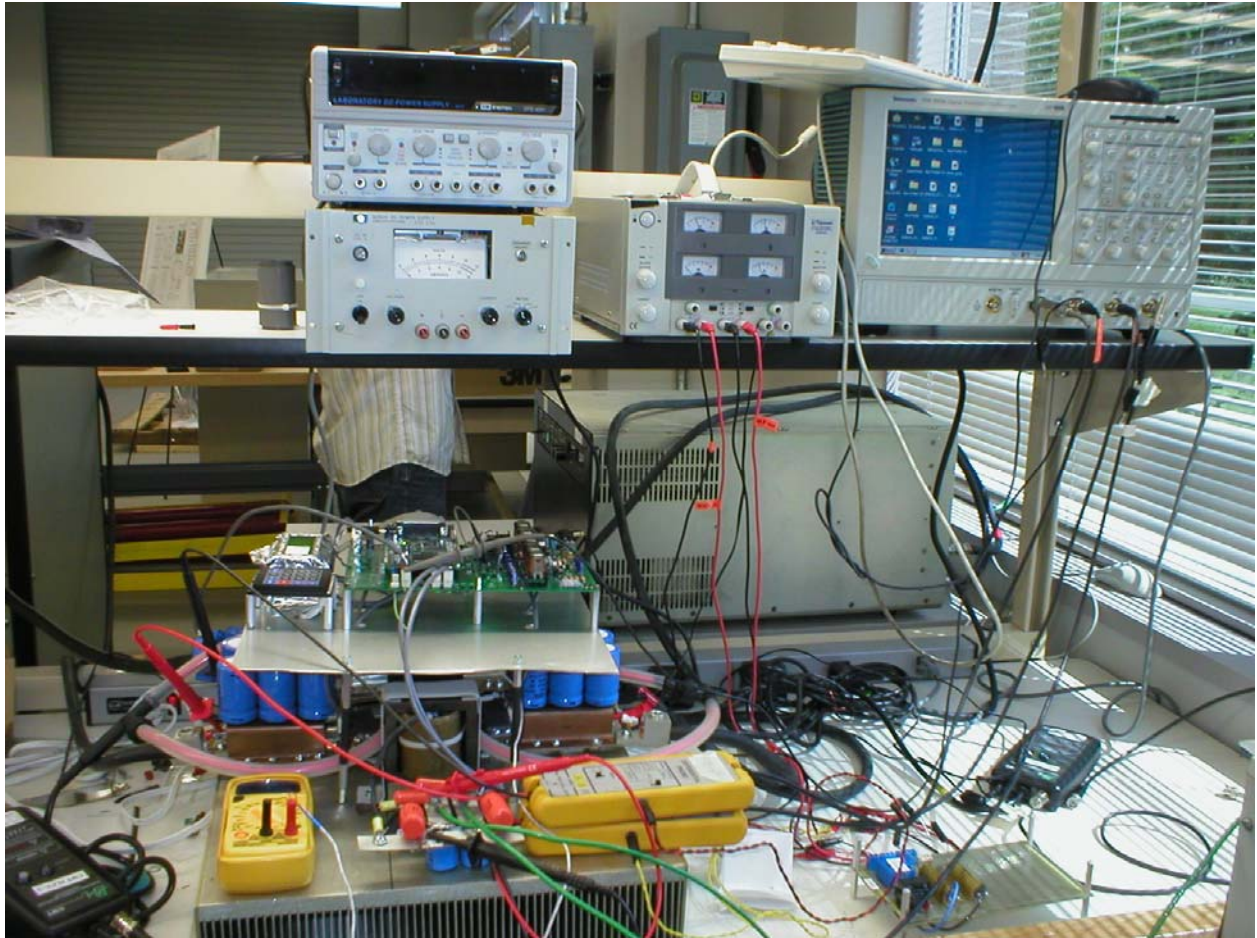
APPENDIX C: PHOTO OF PROTOTYPE

1. PHOTO OF THE DSP AND GATE-DRIVER BOARD

2. PHOTO OF THE PROTOTYPE

3. PHOTO OF THE EXPERIMENTAL SETUP

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