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# EXTENDED CONSTANT POWER SPEED RANGE OF THE BRUSHLESS DC MOTOR THROUGH DUAL MODE INVERTER CONTROL

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# 1. INTRODUCTION

The trapezoidal back electromotive force (emf) brushless direct current (dc) motor (BDCM) with surface-mounted magnets has high-power density and efficiency especially when rare-earth magnet materials are used. Traction applications, such as electric vehicles, could benefit significantly from the use of such motors. Unfortunately, a practical means for driving the motor over a constant power speed ratio (CPSR) of 5:1 or more has not yet been developed. A key feature of these motors is that they have low internal inductance. The phase advance method[1] is effective in controlling the motor power over such a speed range, but the current at high speed may be several times greater than that required at the base speed. The increase in current during high-speed operation is due to the low motor inductance and the action of the bypass diodes of the inverter. The use of such a control would require increased current rating of the inverter semiconductors and additional cooling for the inverter, where the conduction losses increase proportionally with current, and especially for the motor, where the losses increase with the square of the current. The high current problems of phase advance can be mitigated by adding series inductance; however, this reduces power density, requires significant increase in supply voltage, and leaves the CPSR performance of the system highly sensitive to variations in the available voltage. A new inverter topology and control scheme has been developed that can drive low-inductance BDCMs over the CPSR that would be required in electric vehicle applications.[2] This new controller is called the dual-mode inverter control (DMIC). It is shown that the BDCM has an infinite CPSR when it is driven by the DMIC.

The DMIC described in this report has the following features:

- Internal motor inductance can be low and is not a critical parameter. The controller works well with high-strength rare-earth magnets and preserves the power density of such motors. The method also works well with high-inductance motors.
- The motor current remains within the rated root mean square (rms) value over the extended CPSR. Using the DMIC does not increase motor cooling requirements or increase the current handling requirement of inverter switching components.
- Motoring and regeneration are possible. In the regeneration mode, depending on the motor design, it is possible to regenerate at many times the rated power for brief periods. This feature is attractive for electric vehicle applications or other applications requiring rapid regenerative braking.
- In battery-driven applications, the controller functions over a wide range of battery voltage.
- The controller is well suited for use with nonsalient rotor designs. Interior-mounted permanent magnets are not required.
- The controller provides the functional equivalent of field weakening without requiring an auxiliary field winding or rotor saliency.
- Motor back emf can be sinusoidal or trapezoidal.
- The inverter is capable of extinguishing the motor current within one-sixth of a fundamental cycle if a fault develops in the dc supply system.
- A transition control allows smooth operation during speed variations about the base speed. Operation below base speed can be achieved with the usual methods: sinusoidal pulse-width modulation (PWM) for the sinusoidal-back emf motor and hysteresis band current control for the trapezoidal-back emf motor. Operation above base speed involves switching at the

fundamental frequency eliminating the need for high-frequency switching and its associated losses.

- The controller calculations are not elaborate, and the controller can be implemented with a digital signal processor (DSP) or a small microprocessor.

The report is organized into four primary sections. Section 2 describes the motor model and the parameters of an example motor, which is used for demonstration. The example motor has been used in laboratory work to verify the principles of the DMIC. In the third section, we describe the present state-of-the-art in CPSR control for the BDCM, which is the phase advance method. It is shown that when the motor inductance is low, the phase advance method results in motor currents that greatly exceed the ratings required at base speed. Increasing the motor inductance, either through motor design or added external inductance, reduces the power conversion capability of the motor unless additional supply voltage is added to compensate for the additional internal impedance. The required increase in voltage may be substantial. The voltage sensitivity of the phase advance control of a high-inductance motor will not lend itself to applications in which the supply may undergo large changes in potential. In the fourth section, the DMIC is introduced. The inverter topology and firing schemes for motoring and regeneration are described. It is shown that the DMIC can operate over a wide CPSR with low or high motor inductance. The method is shown to be very tolerant of supply voltage variations. A special commutation method, made possible by the DMIC inverter structure, is shown to improve the power conversion efficiency per rms amp. Simulated operation in the motoring and regenerative braking modes is presented and compared to the performance of the phase advance method. In the fifth section the motor equations are solved analytically, and it is shown that the BDCM has an infinite CPSR when driven by the DMIC. Finally, we offer conclusions and our plans for development of the DMIC.

## 2. MOTOR MODEL AND EXAMPLE MOTOR PARAMETERS

Let the parameters of the BDCM be described by the following notation:

$p$ = number of poles
$N_b$ = base speed in rpm
$E_b$ = magnitude of the phase-to-neutral emf at base speed
$P_r$ = rated output power
$L_s$ = self-inductance per phase
$M$ = mutual inductance
$L$ = equivalent inductance per phase = $L_s - M$
$R$ = winding resistance per phase
$v_{an}$ = phase *a* to neutral voltage
$e_{an}$ = phase *a* back emf (to neutral)
$N$ = actual rotor speed in rpm
$n$ = relative rotor speed = $\frac{N}{N_b}$
$E(n)$ = peak phase-to-neutral emf at speed n = $n E_b$
$\Omega_b$ = base speed in electrical rad/s = $\frac{p}{2}\frac{2pN_b}{60}$

With surface-mounted magnets the motor is modeled by the phase equations[3]:

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} L_s & M & M \\ M & L_s & M \\ M & M & L_s \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_{an} \\ e_{bn} \\ e_{cn} \end{bmatrix}. \tag{1}$$

The phase-to-neutral back emfs are trapezoids with 120° of flat top in each half cycle and an amplitude that is linearly proportional to speed. The phase *b* and *c* emfs are delayed from the phase *a* emf by one-third and two-thirds of a cycle, respectively. The shapes of the emfs are shown in Fig. 1.

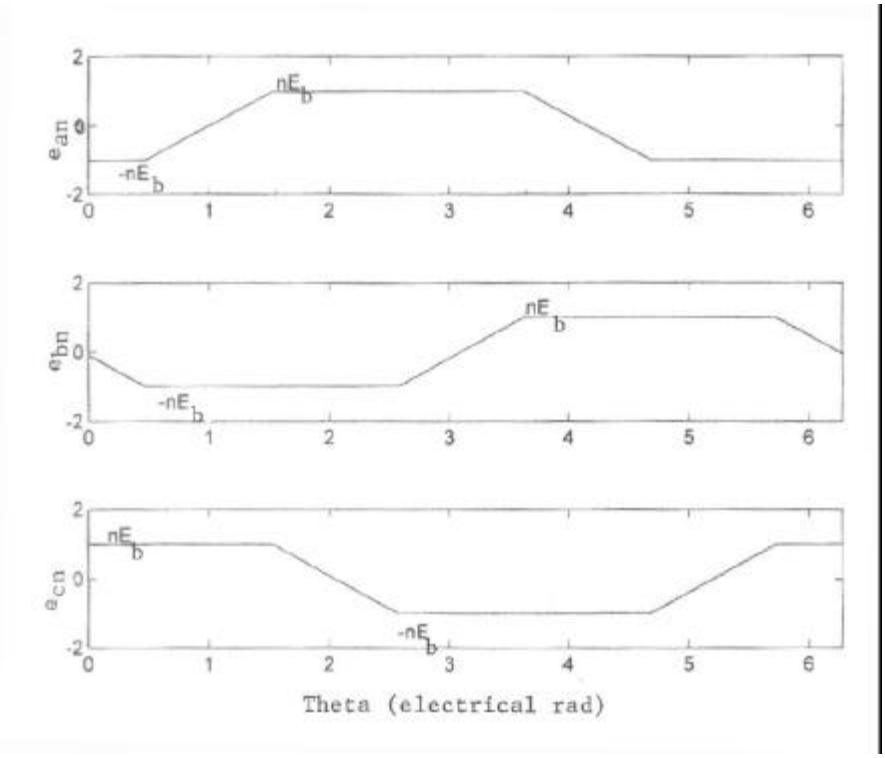


**Fig. 1. Back-emf waveshapes of the BDCM**

Because the phase currents sum to zero, only two of these equations are independent, and a second-order state model can be derived. Preserving phase *a* and *c* currents results in

$$\frac{d}{dt} \begin{bmatrix} i_a \\ i_c \end{bmatrix} = \begin{bmatrix} -R/L & 0 \\ 0 & -R/L \end{bmatrix} \begin{bmatrix} i_a \\ i_c \end{bmatrix} + \frac{1}{3L} \begin{bmatrix} 2 & -1 \\ -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ab} - e_{ab} \\ v_{cb} - e_{cb} \end{bmatrix} . \tag{2}$$

Equation 1 can be further simplified when only two phases are conducting. Assuming that phase *c* is OFF, then the current in phase *b* is the negative of the current in phase *a*, and the model simplifies to

$$\frac{d}{dt} i_a = -\frac{R}{L} i_a + \frac{1}{2L} [v_{ab} - e_{ab}]. \tag{3}$$

Below its base speed, the BDCM runs on two phases at a time. At the instant the switching occurs, there is a finite commutation interval during which the outgoing phase current goes to zero. During this short commutation interval all three phases are conducting, and the appropriate model is expressed by Eq. 2. Once the commutation is complete, only two phases are conducting, and the model in Eq. 3 can be used.

In this study an example motor, designed by the Oak Ridge National Laboratory (ORNL), had the following measured parameters:

$p$ = 12 poles
$N_b$ = base speed = 2600 rpm
$L_s$ = 61.8*m*H per phase
$M$ = 11.8*m*H
$R$ = 0.0118 Ω
$E_b$ = peak phase-to-neutral back emf at base speed = 74.2 V
$P_r$ = rated power = 36.927 kW (49.5 hp)
$V_{dc}$ = 162 V dc supply voltage

The 162-V supply is the voltage required by the motor. Any voltage drop in the inverter would have to be added to this value. In this report, the inverter voltage drops are neglected and the above ideal value is used. A more detailed simulator, which includes inverter voltage drops, is being developed.

Assuming the classical idealized rectangular phase current waveshape of the BDCM (rectangular shape of 120° duration each half cycle), the theoretical peak and rms currents of this motor are

$$\begin{aligned} I_{pk} &= \text{peak current} = \frac{P_r}{2E_b} = 249 \text{ A}; \\ I_{pk} &= \text{rms current} = I_{pk}\sqrt{\frac{2}{3}} = 203.3 \text{ A}. \end{aligned} \tag{4}$$

These values will be used as ratings for the simulated performance presented below.

The example motor was not built for high-speed operation, and the integrity of its rotor at speeds above 3000 rpm is not known. However, in this study the performance of the motor and the two constant power speed control schemes are simulated for speeds of two times base speed (5200 rpm) and higher. Rotor designs for high-speed operation are under development[4], and a full-scale test of the DMIC on a motor capable of high speed will be conducted in the future. In the short term, the example motor has been operated using the DMIC control at reduced dc supply voltage, which effectively reduces the base speed and the power rating of the machine. Successful operation over a 6:1 CPSR has been observed, and experimental results agree well with simulated performance. These experimental results will be reported.[5]

In the next section, simulation results of the CPSR performance of the example motor using the phase advance method are presented.

## 3. CONSTANT POWER OPERATION USING THE PHASE ADVANCE METHOD

The phase advance method[1] for driving the BDCM above base speed uses the common voltage-fed inverter topology shown in Fig. 2. The firing scheme for the phase advance method is shown in Fig. 3. Figure 3 shows the timing of the phase *a* transistor (Q1 and Q4) gate signals relative to the phase *a* line-to-neutral voltage. Phase *b* and *c* transistors would be fired with delays of one-third and two-thirds of a cycle relative to the firing in phase *a*. Transistor Q1 is fired $q_a$ deg ahead of the instant that the phase *a* back emf, $e_{an}$, reaches its positive maximum whose value is n times $E_b$; $q_a$ is the "advance angle." Transistor Q4 is fired $q_a$ deg ahead of the instant that $e_{an}$ reaches its most negative value, which is –n times $E_b$. The gate pulse width of each transistor is 120°. The advance angle may be varied from 0 to 60°. An advance angle of 0° puts the motor in the maximum regeneration mode, while 60° corresponds to maximum motoring operation. An advance angle near 30°, the exact value of which depends on the motor resistance, inductance, and the relative speed, results in zero average motor power.

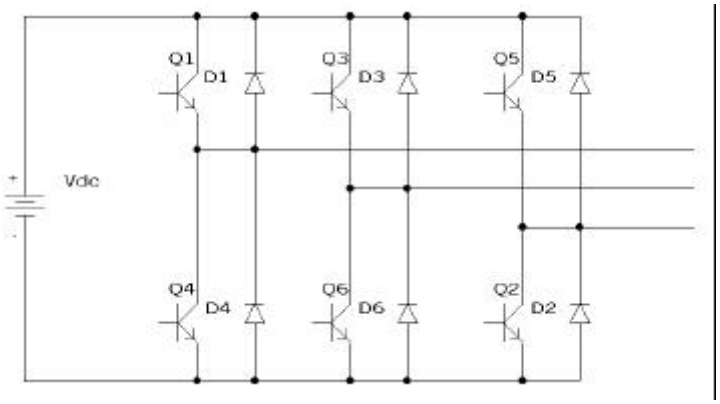


**Fig. 2. Common voltage-fed inverter topology used with phase advance.**

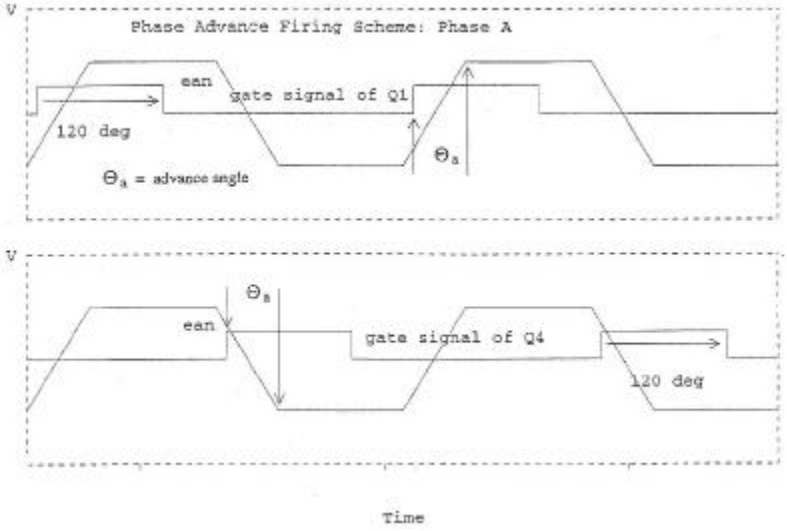


**Fig. 3. Firing scheme used with phase advance, phase *a*.**

The firing scheme of Fig. 3 results in the transistors being fired in the order 1, 2, 3, 4, 5, and 6 with 60° between successive firings and with each transistor remaining on for 120° after it is fired. At any given time, one odd-numbered transistor is "ON," connecting one of the phases to the positive rail of the dc supply; one even-numbered transistor is on, connecting one of the other two phases to the negative rail of the dc supply. Over one electrical cycle, a sequence of six pairs of transistors in the ON state are observed: (Q1, Q6, or a+, b-), (Q1, Q2, or a+, c-), (Q3, Q2, or b+, c-), (Q3, Q4, or b+, a-), (Q5, Q4, or c+, a-) and (Q5,Q6 or c+, b-). This sequence is the same as the conduction envelope used for the BDCM during motoring operation below base speed except that the advance angle is fixed at 0 below base speed and power is controlled by modulating the conduction of the on transistors. Above base speed, the power is controlled by varying the advance angle, and modulation of the on transistors is not used.

Because only two transistors are ON at a time, what is the status of the "idling phase" that is not connected to an ON state transistor? There is a substantial difference in the situation of the idling phase below and above base speed operation. Below base speed the voltage potential at the idling phase is never greater than the positive rail or less than the negative rail of the dc supply. Consequently, not only are the two transistors in the idling phase OFF, but after a brief commutation period, both bypass diodes are back biased and are also OFF. Thus, below base speed the idling phase is isolated from the dc supply, and its current remains zero until one of the transistors is turned on. During high-speed operation, the internal voltage of the idling phase may be greater than the positive rail or less than the negative rail of the dc supply causing one of the bypass diodes to turn on. Consequently all three phases are in conduction simultaneously during high-speed operation with current flowing either through a transistor or a bypass diode in each phase. There really is not an "idling" phase at any time. The conduction of the bypass diodes during high-speed operation results in each motor phase current contributing both motoring and regenerating power. When the motor inductance is low, the current magnitude is large, and both the motoring and regenerating components are much larger than rated average power. The sum of the two components is on the order of the rated power of the motor. The undesirable conduction of the bypass diodes is the critical defect in the phase advance control method. This problem will be solved by the DMIC converter topology.

A PSPICE model of the BDCM was combined with the common voltage-fed inverter topology and the phase advance control method to study the performance of this method in driving the example motor. Speeds of 2, 3.5, and 5 times base speed was simulated for advance angles from 0 to 60° in 5° increments. For each speed and advance angle combination, the simulator was run to determine the peak phase current, rms phase current, average motor power, and the ripple in the motor power. The results of the study are shown in Fig. 4.

The plot of average power vs advance angle in Fig. 4 shows that the phase advance method is effective in controlling the power developed by the motor. For the example motor, the motor power can be varied from minus rated power (maximum regeneration) to plus rated power (maximum motoring), using an advance angle ranging from 20° to 50°. Unfortunately the rms and peak motor currents are substantially larger than their rated values for every operating condition of twice base speed or higher. At 5 times base speed and an advance angle of 50°, the rated motoring power is developed, but the rms and peak currents are 3.04 and 3.57 times their rated values, respectively. In this case the inverter losses would be increased by about 3 times

the losses at base speed, while the copper losses in the motor would be about 9 times larger than at base speed. Note that the rms and peak current magnitudes tend to increase with speed using the phase advance control method. Consequently, speeds higher than 5 times base speed would result in still higher motor current levels. The instantaneous power ripple at relative speed "n" varies at the fundamental frequency, which is 260 Hz for the example motor times 6n. Thus, the peak-to-peak ripple in the instantaneous power shown in Fig. 4 would not likely result in perceptible speed fluctuations in the rotor shaft due to the smoothing resulting from the rotor inertia.

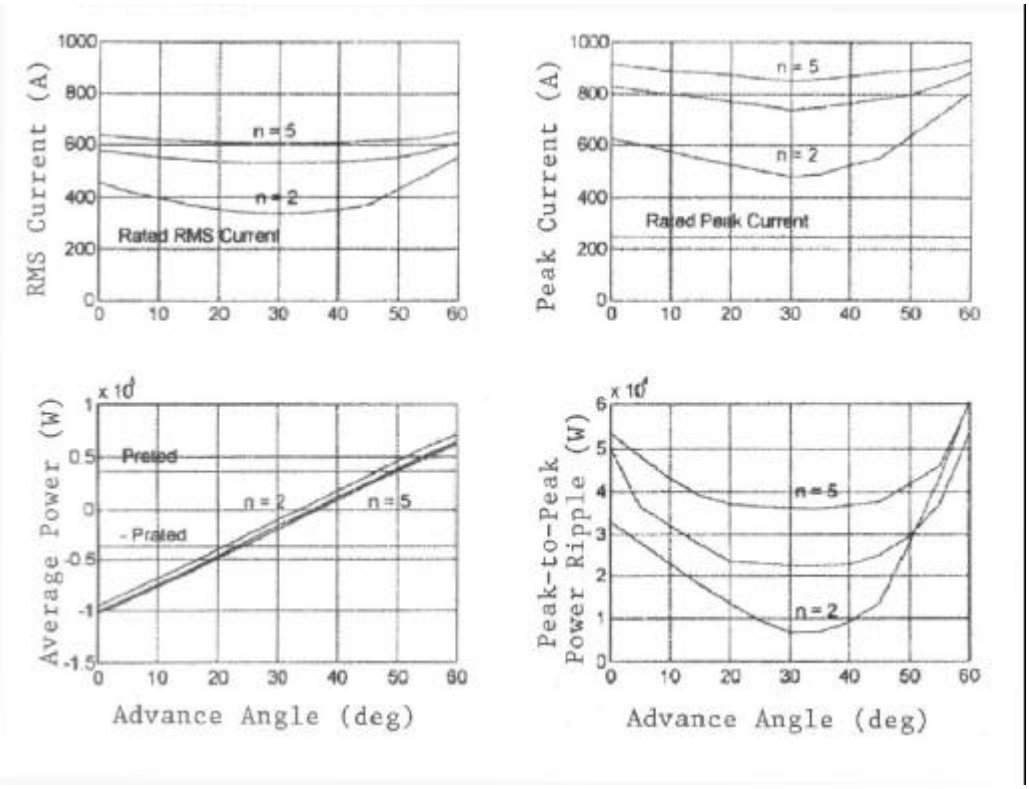


**Fig. 4. High-speed performance of the nominal motor driven by the phase advance method with $V_{dc}$ = 162 V.**

The high magnitude motor current that is observed with the phase advance method, at least when applied to a low-inductance motor, can be traced to the actions of the bypass diodes in the common voltage-fed inverter topology. For a relative speed of 5 and a phase advance of 50° the average power developed by the motor is very close to the rated power of the example motor. Figure 5 shows the instantaneous phase *a* current, $i_a$, and phase *a* back emf, $e_{an}$, for this operating condition. Also shown in the figure are the portion of phase *a* current flowing through the transistors and that portion which flows through the bypass diodes. Note that current conduction is continuous, phase *a* never idles, the amplitude of the current is very large (888.4 A peak, 617.5 A rms), and the phase *a* current peak leads the center of the peak back emf by nearly 90°. With respect to fundamental frequency components of phase voltage and current, the motor is being operated at a very poor power factor. Also, the current component through the bypass diodes is large, and when the bypass diodes conduct, the phase current and back emf have opposite polarity. Thus, the action of the bypass diodes will result in a regeneration component rather than a motoring component.

Figure 6 displays the instantaneous total motor power, the instantaneous power developed in phase *a*, the instantaneous power flowing through the phase *a* transistors, and the instantaneous power flowing through the phase *a* bypass diodes for the same motoring mode operating condition, n = 5, $q_a$ = 50°. The average total power is 36,332 W, which is essentially the rated power of the example motor (36,927 W), and the ripple in the total instantaneous power is a modest 41,860 W. However, in phase *a* alone, the peak-to-peak power oscillation is about 500 kW with an average value of 12,110 W. Note in the plots with the phase *a* power resolved into the portion flowing through the transistors and through the bypass diodes that, on the average, the transistors contribute +71,600 W to motoring while the bypass diodes contribute –59,500 W to regeneration. The sum of the average power through the transistors and the average power through the bypass diodes is the same as the total average power in phase *a*.

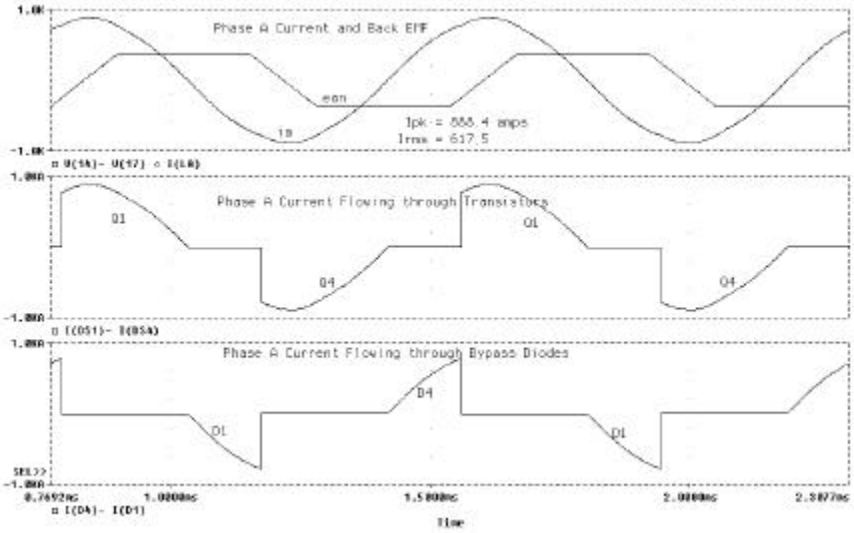


**Fig. 5. Phase *a* current and emf and phase *a* current through transistors and bypass diodes.**

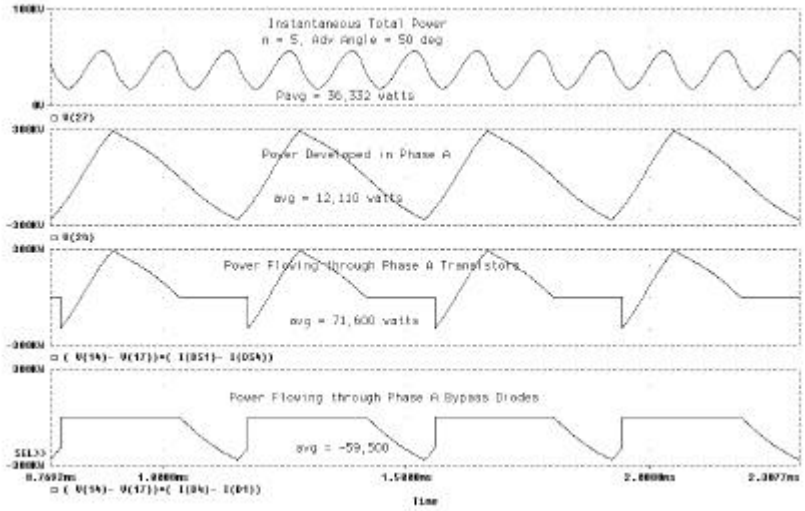


**Fig. 6. Instantaneous total power, phase *a* power, and phase *a* power flowing through transistors and bypass diodes.**

These results indicate that the performance of the phase advance method for operating the example BDCM at speeds of twice base speed or higher is not attractive. The motor current is several times the rated level at base speed; if the phase advance method were used, the inverter components would require increased ratings, and substantial cooling would be required to remove the additional heat in the inverter and motor windings.

The performance of the phase advance method improves if the motor inductance is sufficiently large. The self-inductance and mutual inductances of the example motor were changed from the nominal values, 61.8 $m$ H and 11.8 $m$ H respectively, to values 3.1 times as large. The operating conditions n = 2, 3.5, 5 and $q_a$ = 0, 5°, . . ., 55°, 60° were again simulated with the dc supply remaining at the nominal 162 V. The rms current, peak current, and average power for each operating point is shown in the first column of plots in Fig. 7. Observe that the rms and peak current magnitudes are greatly reduced from the values observed with the nominal motor inductance. However, the motor does not develop full rated motoring or regenerating power over the 60° range of advance angle. At a relative speed of n = 5 and $q_a$ = 60°, the motor develops 25,491 W, which is only 69% of the 36,927 nominal motor rating, and the rms current is 210.9 A, which is slightly over the 203.3 A rating. The problem is that the 162 V supply is not sufficient to overcome the additional internal impedance and maintain rated power. More voltage is required. The supply was increased to 212.6 V, and the simulations were repeated for the study set of operating points. The results of the simulations are shown in the second column of plots in Fig. 7. Note that the 212.6 V supply is able to swing the motor power over the full power range, and the rms and peak currents are within bounds.

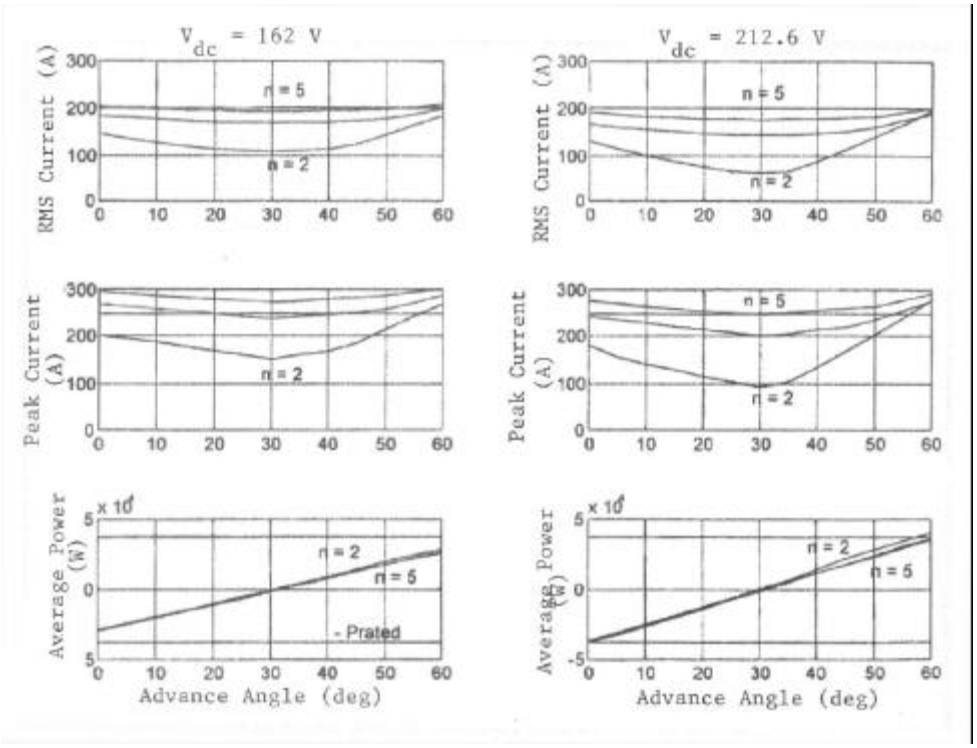


**Fig. 7. High-speed performance of the high-inductance motor driven by the phase advance method with $V_{dc}$ = 162 and 212.6 V.**

Thus, the phase advance method performs well for the high-inductance motor provided the dc supply voltage is increased to an appropriate level. As pointed out in Ref. 6, the added inductance need not be built into the motor. Rather, a higher equivalent motor inductance can be achieved by adding external inductances in series with the motor phase windings. The sensitivity of the phase advance control method to supply voltage does suggest that, in an electric vehicle application, this technique might have some difficulty in maintaining performance as the battery discharges and the available supply voltage decreases.

In the next section, the DMIC method for operating a BDCM above base speed is introduced. The DMIC method is insensitive to motor inductance and is able to drive the BDCM above base speed at rated power and remain within the rated rms current required at base speed.

## 4. CONSTANT POWER OPERATION USING DMIC

The primary problem with the phase advance method for high-speed, constant power operation was shown to be the uncontrolled conduction of the inverter bypass diodes. To review, when operating above base speed, the internal motor phase voltages may exceed the positive or negative rail of the dc supply, which turns on one of the bypass diodes. The DMIC avoids this problem by using a different inverter topology than the common voltage-fed inverter that applies phase advance. In the DMIC, the conventional inverter output is interfaced to the motor through a thyristor-based alternating current (ac) voltage controller as shown in Fig. 8. If in a given phase the two transistors are off, phase current can flow through one of the bypass diodes provided one of the thyristors in that phase is on. This current, however, will not be allowed to reverse. Once the phase current reaches zero, the conducting thyristor shuts off. No matter what the internal potential of that phase, the phase is isolated from the supply until one of the transistors and a companion thyristor are fired. This scheme allows commutation to occur, but once the outgoing phase current reaches zero, there is no further conduction until the next time that the phase is intentionally fired. Thus, each phase of the DMIC inverter has three states; a given phase can be connected to the positive rail of the supply, connected to the negative rail of the supply, or isolated (i.e., floating) when all transistors and thyristors in that phase are off.

Below base speed, the DMIC uses the normal BDCM control scheme and operates on two phases at a time, except for the short commutation intervals when all three phases are conducting. It is appropriate to refer to operation below base speed as a “single-phase” mode of operation because the majority of the time the dc supply current enters one phase winding and returns through another phase winding while the third phase idles. **The ability of the DMIC inverter to isolate one phase from the supply allows the single-phase operation concept (i.e., current through only two phases at a time) to be extended to high-speed operation.** The term, dual-mode, applies to the fact that below base speed, power regulation is achieved for mode one by modulating the conduction of the transistors and involves high-frequency switching. The switching rate depends on the hysteresis band within which phase current is allowed to vary around its desired value. Above base speed mode two switches all of the transistors at the fundamental rate.

While the transistors are modulated for regulation below base speed, which may involve kilohertz switching rates, the thyristors do not participate in the regulation and are always fired at

the fundamental rate as determined by motor speed. Above base speed, all of the devices are fired at the fundamental rate.

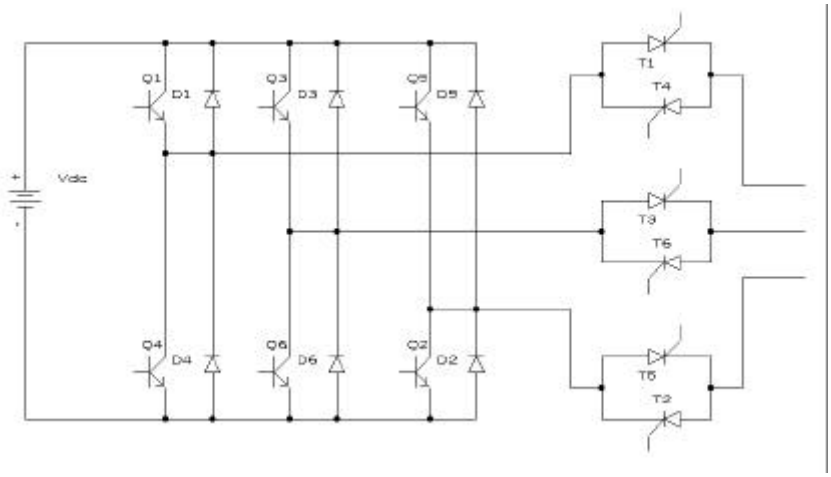


**Fig. 8. Inverter topology used with the DMIC.**

In the phase advance method, with the common voltage-fed inverter topology of Fig. 2, the motor will feed a fault in the dc supply system as long as the motor shaft is turning. The motor current would flow through the bypass diodes into the fault. In the DMIC inverter, once a fault is detected, thyristor firing can be inhibited to prevent the motor from feeding the fault even though the rotor continues to spin. The motor fault current would be extinguished within one-sixth of a fundamental cycle after the fault is detected, and further thyristor firing is disabled.

Using the phase advance method, the output of the common voltage-fed inverter is bipolar under high-speed operation; any given phase is connected to either the positive or negative rail of the dc supply. Therefore, the transistors in the inverter need only be rated to block the dc supply voltage. In the DMIC inverter, with its tristate output, the semiconductors must block the internal emf in the open phase and the supply voltage. The internal emf magnitude to be blocked is the relative speed n times the magnitude of the back emf at base speed. Fortunately, the voltage blocking duties in the DMIC inverter are borne mainly by the thyristors and not the transistors. High-voltage thyristors are readily available and their cost in production may be similar to that of comparably rated transistors. The transistors need only be rated to block the dc supply voltage, which will reduce their cost.

The firing scheme of the DMIC controller for the motoring mode of operation is shown in Fig. 9. As with the phase advance method, the transistors are fired at an advance angle, $q_a$, but the advance angle is defined relative to the intersection of one of the phase-to-phase back emfs with the dc supply voltage. Figure 9 shows the firing scheme for the transistors and thyristors of phase *a* referred to the line-to-line emf, $e_{ab}$. The firing of the semiconductors in phase *b* would be completely analogous to Fig. 9 with the relevant line-to-line emf being $e_{bc}$, and the firing in phase *c* would be referred to the voltage $e_{ca}$. Just as in the phase advance method of the previous section, there are six distinct intervals, which involve one phase being connected to the positive rail of the dc supply and one phase being connected to the negative rail of the supply. Each interval lasts for 60 electrical degrees before one of the conducting phases is exchanged for the

idling phase. Once a phase is energized, it remains energized for two 60° intervals before being rotated out as the idling phase. Firing before the intersection of $e_{ab}$ with $V_{dc}$ allows current to be driven into the phase *a* winding because $V_{dc}$ is greater than $e_{ab}$ when Q1 and T1 are fired. As time advances, $e_{ab}$ becomes greater than $V_{dc}$, which causes the phase *a* current to decrease. The greater the advance angle, the greater the amount of current that can be driven into the winding before the crossover of $e_{ab}$ with $V_{dc}$, and the more power that will be developed by the motor.

Each odd- (even-) numbered thyristor is fired at the same time as the corresponding odd- (even-) numbered transistor and is fired again 60° later. The second firing is necessary at low advance angles, where the incoming phase current rises but falls to zero before the end of the first 60° interval due to the back emf exceeding $V_{dc}$. If the phase current during the first 60° interval falls to zero, then the thyristor must be retriggered at the start of the second interval. When the phase advance is large, the phase current will not be zero at the end of the first 60° interval, and the thyristor will remain on and not need to be retriggered. In such cases the second firing pulse is redundant.

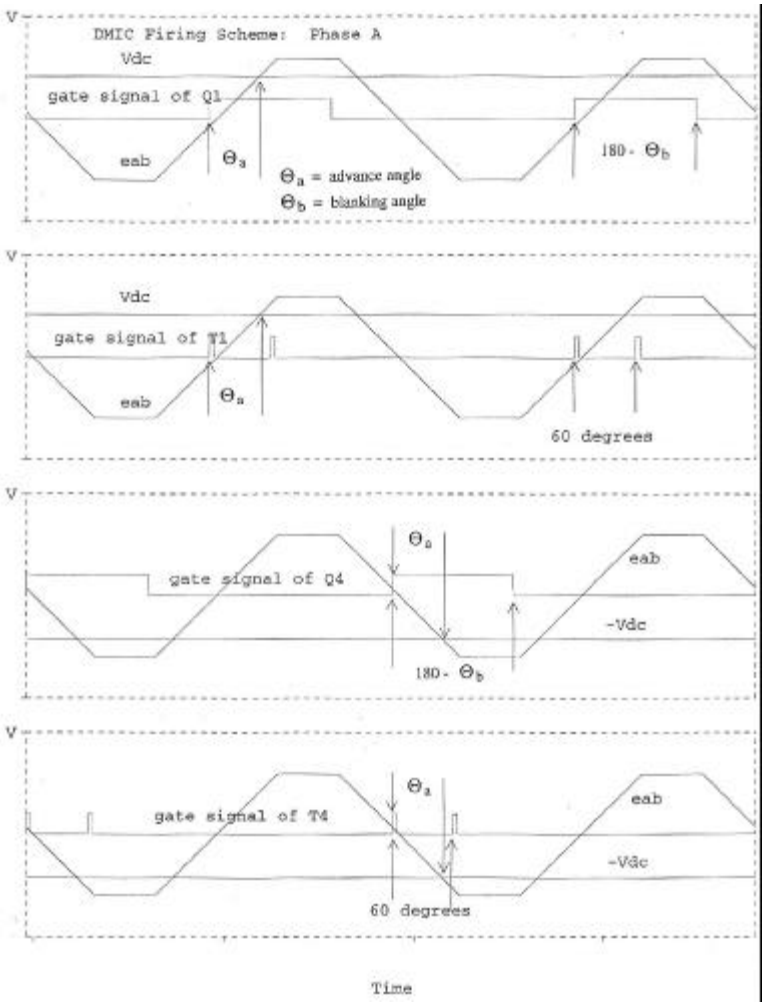


**Fig. 9. Firing scheme of the DMIC in the motoring mode, phase *a*.**

Unlike the phase advance method, where the transistor conduction angles were always 120°, the commanded conduction angle in the DMIC can vary from 120° and approach 180°. In Fig. 9, the transistor conduction angle is denoted as 180° minus the blanking angle, which is $q_b$. In a PWM inverter, some interval is set aside between the time that one transistor in a given phase pole is to be turned off and before the opposite transistor in that pole is to be turned on. This is referred to as the blanking time, and is a safeguard against inadvertent short circuits of the supply due to variations in the OFF and ON times of the transistors. It is analogous to the blanking angle although there is no worry about inadvertent short circuits of the supply in the DMIC.

There is good reason to reduce the blanking angle from 60° to a value closer to 0 degrees. At a commutation time, the phase current in the outgoing phase may be large, but decreasing in magnitude due to the emf crossing $V_{dc}$. That phase is contributing a great deal of power because of simultaneously high current and high voltage. At a blanking angle of 60° the outgoing phase is shut off by turning off its transistor and allowing the phase current to transfer to the bypass diode of the opposite transistor. The thyristor shuts off when the current reaches zero. This sudden reversal of the outgoing phase from one rail of the supply to the opposite rail hastens commutation causing the outgoing phase to go off quickly. However, since the outgoing phase current is already decreasing, allowing the outgoing transistor to stay on longer will slow down the commutation process. Slowing down commutation prolongs the period of simultaneous high current–high voltage in the outgoing phase. As long as the current in the outgoing phase reaches zero within the allowable 60° interval, the amount of power developed will be increased, and substantially so, at the expense of a slight increase in rms current. The increase in power may be as much as 15% at high advance angles, while the increase in rms current is very small. Care must be taken not to run the blanking angle down too far when the motor is operating at speeds that are only slightly greater than base speed. In such cases the back emf is only marginally larger in magnitude than $V_{dc}$, and the outgoing phase may not commutate at all. In fact, should the emf magnitude drop back below the dc supply level, the outgoing phase current may begin to increase. This potential for commutation failures can be avoided by setting the blanking angle to 60° and executing rapid commutation of the outgoing phase. A compromise solution is to set the blanking angle at a value such as 20°, allowing 40° for the phase current to go off naturally and an additional 20° for conventional commutation through a bypass diode if commutation is not already complete.

The transition from below base speed operation to above base speed is a mixture of phase advance, involving adjustment of the advance angle $q_a$ and the blanking angle $q_b$ as well as the set-point of the phase current regulator. Smooth adjustment by the transition control is important in electric vehicle applications so that the operator experiences smooth changes in vehicle speed near the base speed of the motor. The details of the transition control will be reported in subsequent work.

The DMIC inverter topology and the firing control strategy were incorporated into the PSPICE model of the BDCM. For the example motor, the simulator was used to determine the rms and peak motor current, average power, and peak-to-peak power ripple at operating speeds of 2, 3.5 and 5 times base speed for advance angles from 0 to 60°. The study was done twice, first with the blanking angle set to 20°, which is referred to as commutation option 1, and second with the blanking angle set to 60°, which is referred to as commutation option 2. The simulation results are shown in Figs. 10 and 11.

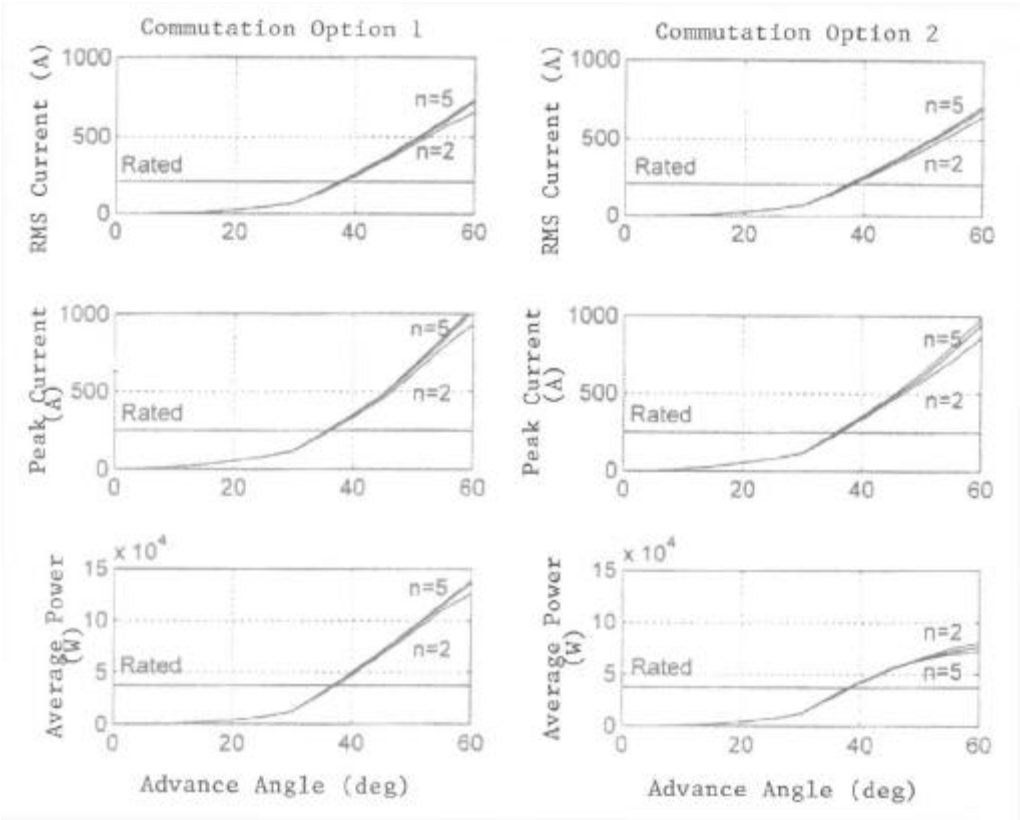


**Fig. 10. High-speed performance of the nominal motor driven by the DMIC in the motoring mode, $V_{dc}$ = 162 V.**

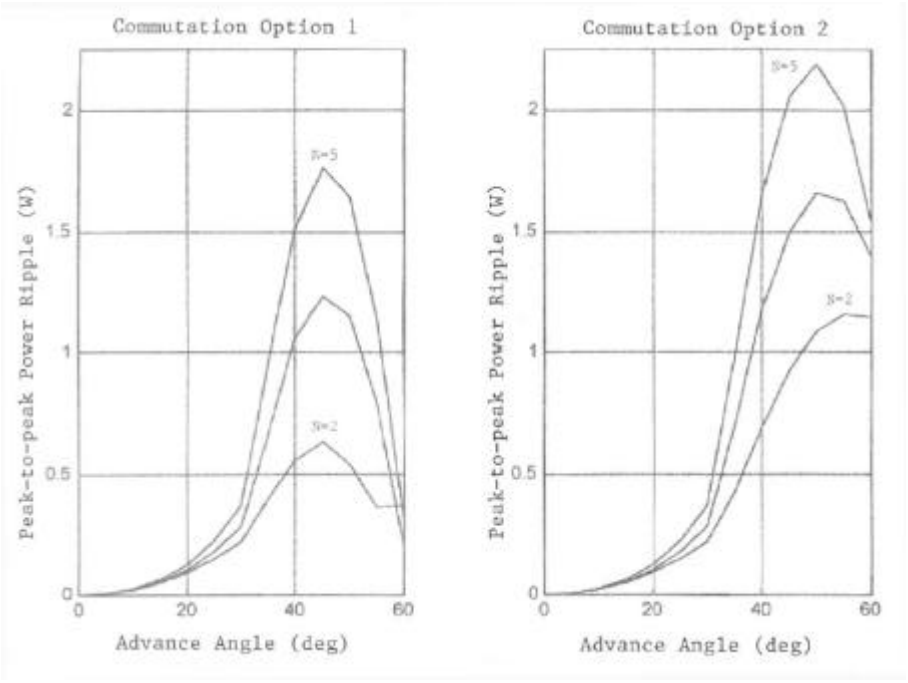


**Fig. 11. Power ripple in the motoring mode with the nominal motor driven by the DMIC.**

Figures 10 and 11 show that both commutation methods are effective in controlling motoring power. Advance angles from 0 to about 38° change the motor power from zero to rated for any speed up to 5 times base speed. For n = 5, the commutation option 2 does not quite reach rated power, 36,927 W, before the rms current exceeds the rated value of 203.3 A. The rated power is reached at an advance angle of 37.6° and an rms current of 210.6 A. With commutation option 1, rated power at n = 5 is reached at an advance of 36.6° with the rms current being 191.6 A. The power efficacy of current at rated power using commutation option 2 is 175.3 W/rms A. For option 1 the corresponding figure is 192.7 W/rms A. Thus, under rated power conditions the power produced per rms amp is 9.9% higher with commutation option 1 than with option 2. Using the rated power of 36,927 W and the ideal rms current below base speed of 203.3 A, the power efficacy of current below base speed is theoretically 181.6 W/rms A. At a relative speed of 5 times base speed, commutation option 1 exceeds this value by 6%. Thus, for the rated rms current the DMIC can produce more power at high speed, at least up to n = 5, than can be produced at base speed. Both commutation options result in phase currents that are higher than the theoretical, 249 A, at base speed. With a 20-A hysteresis band for low-speed regulation, this peak current would be increased to 259 A. At rated power, the peak current is 271 A with commutation option 1 and 295.4 A with commutation option 2. Thus, there is a modest increase in peak current requirement when the DMIC is used with a low-inductance motor.

Figures 10 and 11 also show that a substantial power ripple is associated with the DMIC control. It is well known that single-phase ac motors have a power ripple of twice the average power, and the ripple is at twice the frequency of the motor voltage and current waveforms. Line-fed single-phase motors have a torque ripple at 120 Hz, and yet the shaft runs quite smoothly at high speed due to the smoothing effects of the rotor inertia and its attached load. The BDCM operating in its single-phase mode below base speed produces nearly constant torque, except for torque notches produced as a result of commutation,[6,7,8] because the rectangular phase current wave flows during the constant voltage or "flattop" period of the phase voltage. Under high-speed operation, the phase voltage during the flattop portion of the back emf wave exceeds the dc supply voltage, and current cannot be driven into the winding under this condition. This is why it is necessary to advance the firing to the interval where the emf is undergoing transition and has a value less than the supply voltage. Even though the phase current wave may retain a reasonably rectangular waveshape, the power developed by the DMIC during operation above base speed will contain a ripple because the voltage waveform will not be constant during conduction. In traction applications, the motor will be able to run smooth torque up to base speed, but once the high-speed mode of operation is engaged, there will be a power ripple. At relative speed n, the frequency of the ripple will be at 6n times the electrical frequency at base speed. For the 12-pole, 2600-rpm motor the electrical frequency at base speed is 260 Hz, and the power ripple would be at 1.56 kHz. Oscillations at this frequency, even though they may be of large magnitude, are not likely to result in appreciable shaft speed variations due to the equivalent inertia of the rotor.

Figure 12 shows the phase *a* current waveform, the portion of the current flowing through the phase *a* transistors, and the current through the bypass diodes for commutation option 1 (blanking angle of 20°) at a relative speed of 5 and an advance angle of 36.6°, which is the rated power condition described above. The plots in Figs. 12 and 13 are on the same y-axis scales as the analogous plots of Figs. 5 and 6, which are for the phase advance method. Note that the

bypass diodes never conduct. With the transistor conduction angle extended to 160° commutation is completed during transistor conduction. The phase current hits zero before the transistor is commanded off, but the thyristor cuts off conduction at zero current. Figure 13 shows the instantaneous total power, instantaneous phase *a* power, instantaneous power through phase *a* transistors, and instantaneous power through bypass diodes. Although the instantaneous phase *a* power is positive (motoring) and negative (regenerating), the variation is much smaller than the 500 kW observed with the phase advance method. The regenerating component observed in Fig. 13 is due to the phase advance rather than bypass diode conduction.

The same simulation runs were made for the high-inductance motor. The motoring performance is shown in Fig. 14 for the 162-V supply and the 212.6-V supply, but only for commutation option 1. The high inductance provides a natural increase in commutation time that, combined with a reduced blanking angle, increases the power produced per amp. Using the 162-V supply at relative speed n = 5 and an advance angle of 54.9° results in an rms current of 203 A, a peak current of 285 amps, and an average power of 41,400 W, for an average dc supply current of 268.6 A. Recall that the phase advance method could only produce 25,491 W at a similar condition. For the same speed and advance angle, but with the 212.6-V supply, the rms and peak currents remain 203 and 285 A, respectively; the average dc supply current is still 268.6 A, but the average power produced is 54,776 W, which is almost 150% of the 49.5 hp rating of the motor. The phase advance method resulted in the rated power of 36,927 W at about the same condition.

These results show that the DMIC can accommodate high- or low-inductance motors and can also adjust for variations in supply voltage. This should make this scheme attractive in traction applications.


**Fig. 12. Phase *a* current and back emf, phase *a* transistor current, and bypass diode current.**

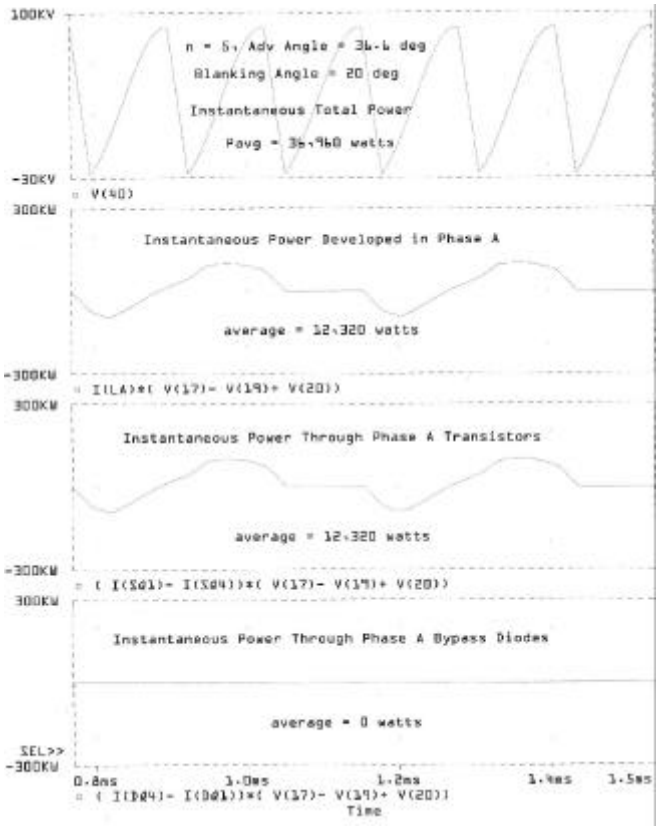


**Fig. 13. Instantaneous total power, phase *a* power, phase *a* power through transistors, and phase *a* power through bypass diodes.**

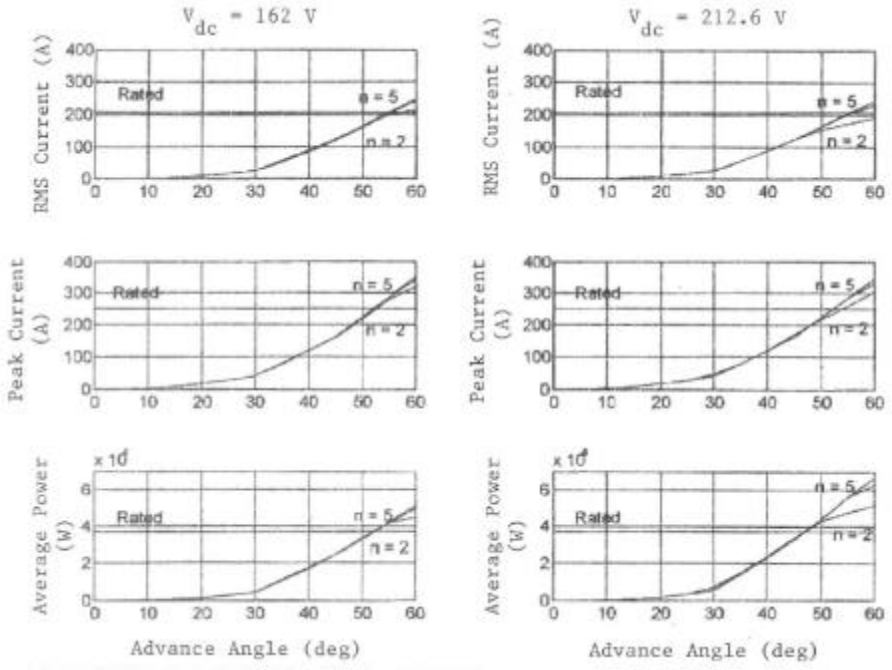


**Fig. 14. High-speed performance of the high-inductance motor driven by the DMIC in motoring mode with $V_{dc}$ = 162 V and 212.6 V.**

The firing scheme for the DMIC in the regeneration mode is shown in Fig. 15. Note that the reference for phase *a* firing is the intersection of the phase-to-phase emf, $e_{ab}$, with $V_{dc}$ at the point where the slope of the emf is negative. This is the companion to the intersection used to initiate firing in the motoring mode. Also note that only the thyristors would be fired at high speed. The figure shows only the firing scheme for the phase *a* thyristors, T1 and T4. The firing of the phase *b* and *c* components would be analogous to Fig. 15. Although the transistors are not required during high-speed regeneration, it may be desirable at low speed to modulate the transistors to boost the motor current. This idea is already used routinely in regeneration at and below base speed for the BDCM.

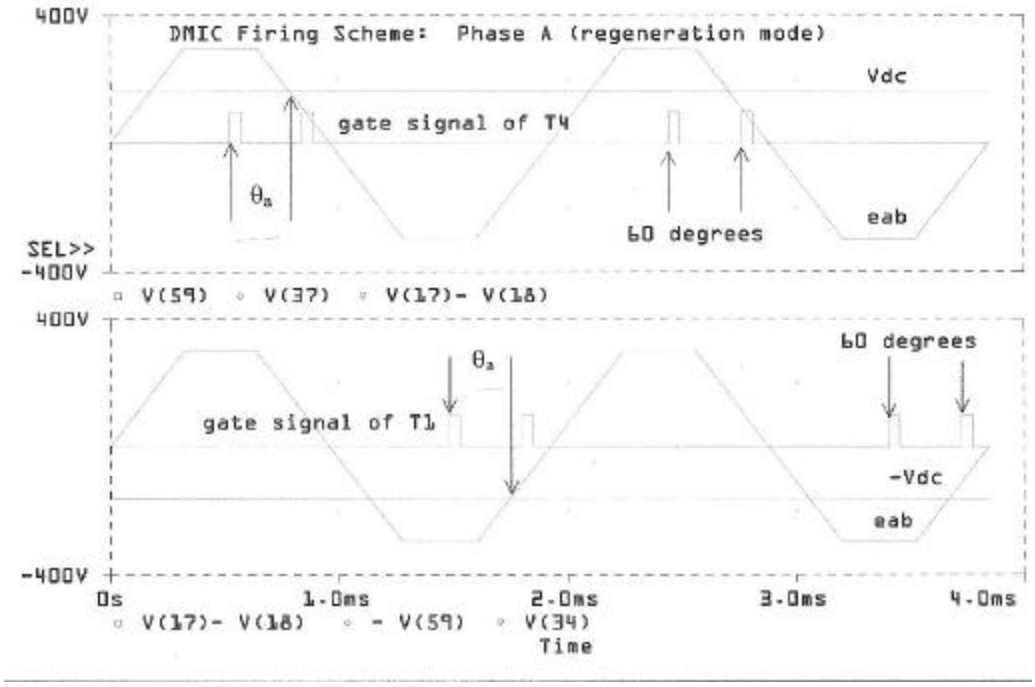


**Fig. 15. DMIC firing scheme in the regeneration mode, phase *a*.**

The performance of the nominal motor in the regeneration mode is shown in Fig. 16. Note that an advance angle of about 40° is adequate to produce rated regenerating power. Beyond 40° of advance the motor current increases rapidly with angle and with speed. However, the regeneration level also increases rapidly, which may make it possible to use short-term regeneration at a level that is several times rated power for brief intervals. This could be useful in electric vehicle applications. Peak and rms currents are within the 249- and 203-A ratings, respectively. A power ripple in the regeneration mode is similar to that observed in the motoring mode.

A closed-loop controller that can drive the BDCM through the full range of speeds is under development.

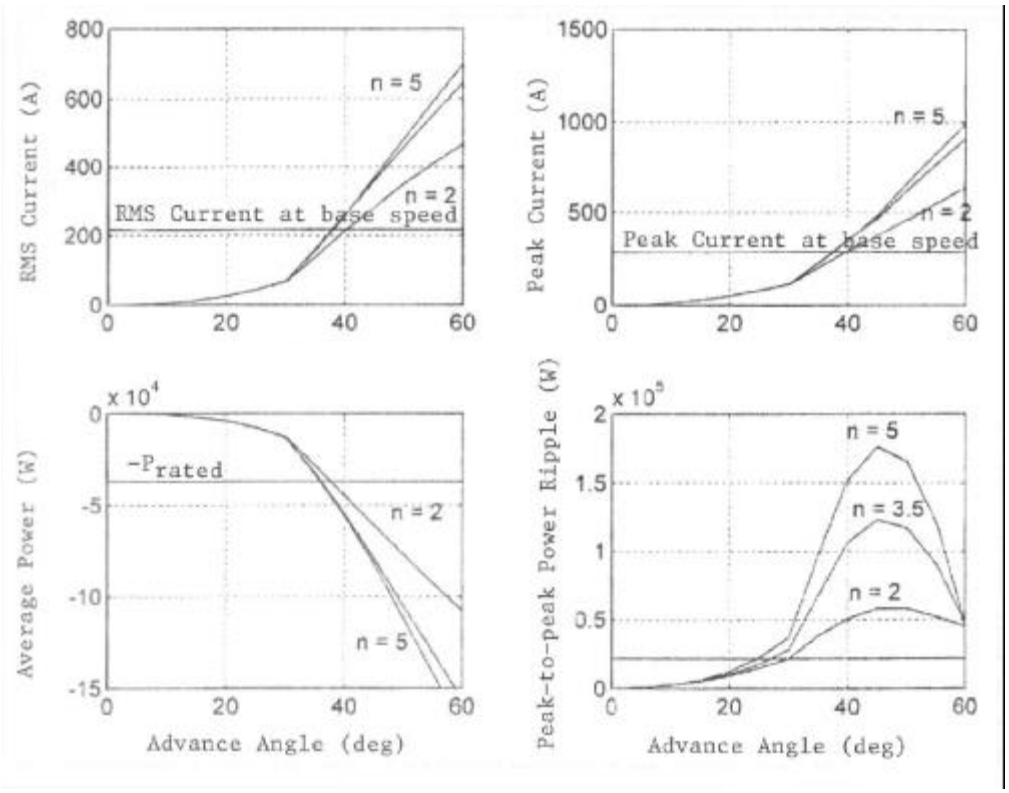


**Fig. 16. High-speed performance of the nominal motor driven by the DMIC in the regeneration mode, $V_{dc}$ = 162 V.**

## 5. THEORETICAL CPSR LIMIT OF A BDCM DRIVEN BY THE DMIC

In this section we show that the theoretical limit to the CPSR using the DMIC is infinite. Factors such as hysteresis and eddy current losses and semiconductor switching losses may place a practical limit on the CPSR, but the control has no inherent limiting consideration that would cause the power to eventually begin decreasing with speed.

With the change of variable,

$$q = n\,\Omega_b\,t\,, \tag{5}$$

the state model Eq. (2) becomes

$$\frac{d}{dq}\begin{bmatrix} i_a \\ i_c \end{bmatrix} = \begin{bmatrix} -R/nW_bL & 0 \\ 0 & -R/nW_bL \end{bmatrix}\begin{bmatrix} i_a \\ i_c \end{bmatrix} + \frac{1}{3nW_bL}\begin{bmatrix} 2 & -1 \\ -1 & 2 \end{bmatrix}\begin{bmatrix} n_{ab} & -e_{ab} \\ n_{cb} & -e_{cb} \end{bmatrix}. \tag{6}$$

Consider the transition from the phase pair (c+,b-) to the phase pair (a+, b-); that is, c is the outgoing phase, and a is the incoming phase. Let the reference ($q = 0$) correspond to the instant that phase *a* is to be connected to the positive terminal of the supply. Assuming that the advance

angle, $q_a$, is larger than 30° ($p/6$ rad), the back emfs can be analytically described during the 60° interval that the operating pair is (a+,b-) by:

$$e_{ab}(q) = \frac{6nE_b}{p}\left(q - q_a + \frac{pV_{dc}}{6nE_b}\right) \qquad 0 \le q \le p/3,$$

$$e_{cb}(q) = \frac{6nE_b}{p}\left(q - q_a + \frac{pV_{dc}}{6nE_b} + \frac{p}{3}\right) \qquad 0 \le q \le q_a - \frac{pV_{dc}}{6nE_b}, \text{ and} \tag{7}$$

$$e_{cb}(q) = 2nE_b \qquad q_a - \frac{pV_{dc}}{6nE_b} \le q \le p/3.$$

These waveforms are shown in Fig. 17. Note that $e_{ab}(q_a) = \mathrm{V_{dc}}$ is consistent with the fact that phase *a* is to be energized $q_a$ rad ahead of the intersection of $e_{ab}$ with $\mathrm{V_{dc}}$. To insert phase *a* positively, we fire transistor Q1 and thyristor T1, engaging the phase *a* terminal to the positive rail of the dc supply. Under commutation option 1, phase *c* is left connected to the positive rail of the dc supply, by extending the gate command for Q5 beyond 120°, and allowing the current in phase *c* to decrease to zero at which time T5 will shut off. Consequently in Eq. (6) set

$$v_{ab} = v_{cb} = +V_{dc}. \tag{8}$$

As a simplification neglect the winding resistance R. It is straightforward to show that the resulting phase currents are:

$$i_a(q) = \frac{E_b}{\Omega_b L}\left\{\left[\frac{2q_a}{p} + \frac{2}{3}\right]q - \frac{1}{p}q^2\right\},$$

$$i_b(q) = \frac{E_b}{\Omega_b L}\left\{\left[\frac{p}{3} - 2q_a\right] + \left[\frac{2}{3} - \frac{4q_a}{p}\right]q + \frac{2}{p}q^2\right\},$$

$$i_c(q) = \frac{E_b}{\Omega_b L}\left\{2q_a - \frac{p}{3} + \left[\frac{2q_a}{p} - \frac{4}{3}\right]q - \frac{1}{p}q^2\right\}, \text{ for} \tag{9}$$

$$0 \le q \le q_c.$$

$q_c$ is the outgoing commutation angle, that is, the angle at which the current in the outgoing phase reaches zero. It can be shown that

$$q_c = 2q_a - \frac{p}{3}. \tag{10}$$

To maximize power conversion efficiency it is desirable that the gate signal for Q5 remains in the ON condition until commutation is complete. The sum of the outgoing commutation angle and the blanking angle must not exceed $\pi/3$ radians; therefore, Eq. 10 yields the minimum blanking angle to make this occur,

$$q_b \le \frac{p}{3} - q_c = \frac{2p}{3} - 2q_a. \tag{11}$$

A microprocessor controller should be able to easily make this type of adjustment continuously during operation so that maximum power conversion efficiency is maintained.

None of the currents in Eq. 9 depend explicitly on the dc supply voltage, $V_{dc}$, or on the motor speed, $nN_b$. The dependence on $V_{dc}$ is implicit in the expressions because of the way that the advance angle is defined. As long as the advance angle remains fixed relative to the intersection of $e_{ab}$ with the actual value of $V_{dc}$, the instantaneous currents would be the same regardless of the dc supply voltage. The dependence on motor speed is implicit in the rotor angle, $q$, given by Eq. (5). Thus, the only impact of speed on the shape of the current waveforms is to compress them in time as the motor speed increases. For a fixed advance angle, $q_a$, the shape of the phase currents over one fundamental cycle remains the same.

After commutation is complete, the motor is running on only phases *a* and *b* and the model of Eq. (3) applies. If the relative speed, n, is 2 or more, the back emf, $e_{ab}$, is described as noted above no matter what the advance angle may be for smaller n, and for a small advance angle it could happen that $e_{ab}$ would reach its maximum inside the 60° interval under discussion, after which the functional form of $e_{ab}$ would be $2nE_b$. With the present assumption it can be shown that the phase currents following commutation are

$$\begin{aligned} &i_a(q) = \frac{E_b}{\Omega_b L}\left\{\left(q_a - \frac{p}{6}\right) + \frac{3q_a}{p}q - \frac{3}{2p}q^2\right\}, \\ &i_b(q) = -i_a(q), \text{ and} \\ &i_c(q) = 0, \text{ for} \\ &q \le q \le \frac{p}{3}. \end{aligned} \tag{12}$$

By interchanging the identities of the phases and recognizing that commutation occurs in both the positive and negative halves of the inverter, the solutions above can be arranged to give the full solution for any of the phase currents over one cycle. For example, to construct the phase *a* current during the positive half cycle, the a phase current above describes the first 60°, the negative of the phase *b* current above describes the second 60°, and the phase *c* current above describes the last 60°. The results of the theoretical model are shown graphically in Fig. 17.

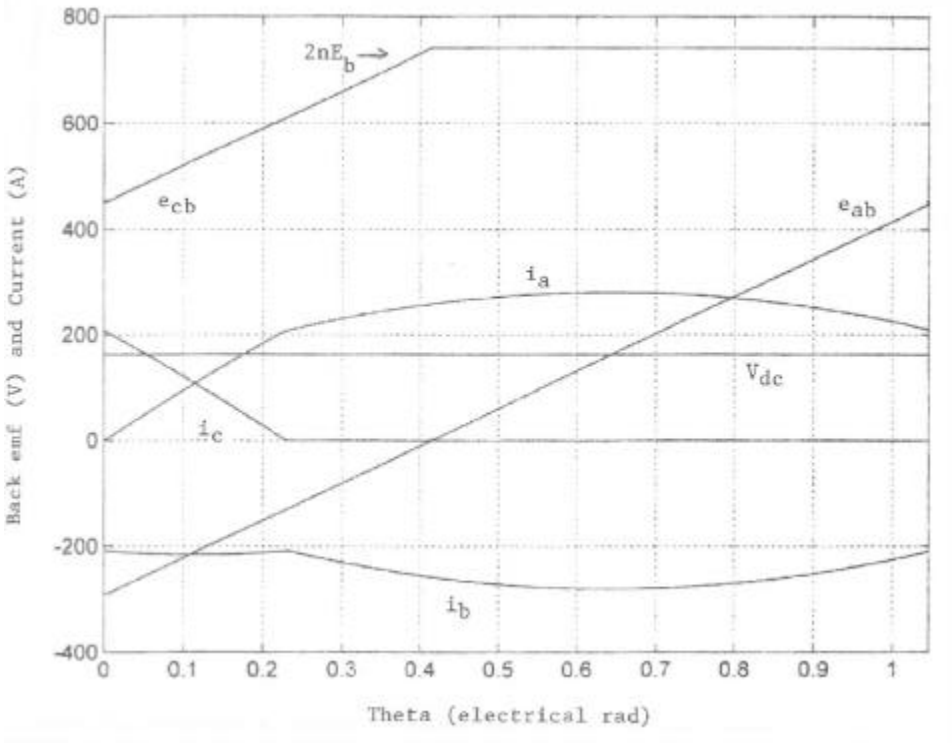


**Fig. 17. Response of the analytical motor model in one 60° interval.**

The implication of Eqs. (9) and (12) is that as long as the advance angle is fixed, the steady state current waveforms will be scaled only in time corresponding to the change in speed, but the shape of the waveforms as well as their peak and rms values will remain unchanged as speed increases. Consequently, if the motor is capable of running within its rated current values and produces rated power at a low speed such as n = 2, it will be able to produce the same performance at any higher speed. The fact that the shape of the current waveform is dependent solely on the advance angle because it simply compresses or expands in time with motor speed means that the maximum CPSR for the BDCM is infinite when driven by the DMIC. The previously mentioned caveats apply along with the fact that winding resistance has been neglected in this analysis, and winding resistance can be a limiting factor.

The phase current solutions in Eqs. (9) and (12) can be used to compute the average power. Because the power has a ripple of six times the fundamental, the average over the 60° interval under study equals the average over a fundamental cycle;

$$P_{avg} = \left\{ \frac{3}{p} \left[ \int_0^{p/3} i_a(q) e_{ab}(q) dq + \int_0^{p/3} i_c(q) e_{cb}(q) dq \right] \right\}$$
$$= \frac{2V_{dc}E_b}{p^2 \Omega_b L} \left\{ q_a^3 + p q_a^2 + \frac{p^2}{3} q_a - \frac{2p^3}{27} \right\}. \quad (13)$$

This expression clearly shows that the output power is linearly dependent on the supply voltage. If the supply voltage is reduced, the desired power may be restored by increasing the advance angle, but increasing the angle will also increase the magnitude of the motor current.

The peak current can also be obtained from the above expressions as an explicit function of the advance angle. The peak may occur in phase *a* or in phase *b*. When the peak in phase *b* is larger than the peak in phase *a*, it means that the maximum current is experienced in the second 60° interval that the phase is energized. The peak current is given by:

$$I_{pk} = \max\{i_a(q), -i_b(q)\}$$
$$= \max\left\{ \frac{E_b}{\Omega_b L} \left[ q_a - \frac{p}{6} + \frac{3q_a^2}{2p} \right], \frac{E_b}{\Omega_b L} \left[ \frac{4q_a}{3} - \frac{5p}{18} + \frac{2q_a^2}{p} \right] \right\} \quad (14)$$

where the expression for $i_a(q)$ is from Eq. 12 and the expression for $-i_b(q)$ is from Eq. 9.

For advance angles less than 0.7666 rad (43.92°), the peak current is determined by the expression for phase *a* current. Above this value, the current peaks in the second 60° interval and is determined by the phase *b* current expression.

The rms current can likewise be computed from the solutions for the phase currents in the single 60° interval analyzed above recognizing that over a half cycle the current in each phase will $i_a$ for $p/3$ radians, $i_b$ for $p/3$ radians, and $i_c$ for $p/3$ radians. Therefore, the average over half of a fundamental cycle equals the average over a fundamental cycle.

$$I_{rms} = \sqrt{\frac{1}{2p} \int_0^{2p} i_a(q)^2 dq}$$
$$= \sqrt{\frac{1}{p} \left\{ \int_0^{p/3} i_a(q)^2 dq + \int_0^{p/3} i_b(q)^2 dq + \int_0^{p/3} i_c(q)^2 dq \right\}} \quad . \quad (15)$$
$$= \frac{E_b}{\Omega_b L} \left\{ \sqrt{\frac{1}{p} \left[ \frac{8}{5p^2} q_a^5 + \frac{8}{3p} q_a^4 + \frac{16}{9} q_a^3 + \frac{4p}{27} q_a^2 - \frac{16p^2}{81} q_a + \frac{23p^3}{1215} \right]} \right\}$$

This theoretical analysis compares favorably to the results obtained with the PSPICE simulator. For the nominal example motor at n = 5, an advance angle of 36.6° and a 162-V supply, the analytical expressions for the average power, peak current, and rms current yield 40,159 W, 281.5 A, and 190.6 A, respectively. When the PSPICE model is modified to have zero winding

resistance to conform with the assumption made in the theoretical analysis, the average power is 39,962 W, while the peak and rms currents are 280.7 and 200.1 A, respectively. With the resistance included the simulated values are 36,927 W, 270.2 A peak, and 191.4 A rms.

Simulation results and the theoretical results confirm that the DMIC offers a very substantial increase in the CPSR performance of the BDCM. Using the example motor we have demonstrated a 6:1 speed ratio in the laboratory. The demonstration was done at reduced supply voltage to keep the rotor speed below 3000 rpm. Additional experiments are ongoing, and detailed results will be reported in the future.

## 6. CONCLUSIONS

The BDCM has been shown to have an infinite CPSR when it is driven by the DMIC. The effect of field weakening is achieved without interior-mounted magnets or supplementary field windings. The rms motor current in the constant power range is no greater than the rms current required to produce full power at base speed. This performance should make the BDCM a viable alternative for traction applications. In addition to extending the constant power range, the inverter that is used can prevent the motor from feeding faults that might develop in the dc supply system. Disabling the thyristor firing pulses after sensing a fault will allow the motor current to be extinguished within one-sixth of a fundamental cycle. This feature will improve safety in electric vehicle applications.

Proof of concept has been achieved in the laboratory with a 49.5-hp/2600-rpm motor running with a reduced power supply. A CPSR of 6:1 was demonstrated with the limiting factor in the demonstration being concern for the integrity of the rotor above 3000 rpm. These results are being prepared for presentation.

It is expected that a demonstration motor designed specifically for high-speed operation will be built within the next year, and full-scale testing of the DMIC is planned.

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