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Oak Ridge National Laboratory Photon-to-Digital Converters for Neutron Imaging Instruments, Final Report

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OAK RIDGE National Laboratory

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PHOTON-TO-DIGITAL CONVERTERS FOR NEUTRON IMAGING INSTRUMENTS, FINAL REPORT

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ABSTRACT

Oak Ridge National Laboratory (ORNL) collaborated with the Université de Sherbrooke (UdeS) to design a modular and scalable tile of innovative digital photodetectors called Photon-to-Digital Converters (PDCs) and the required subsystems to demonstrate the feasibility of large area, single-photon detectors to support high-resolution, depth-of-interaction, fast neutron radiography based on scintillation detectors. The goal is to demonstrate the advantages of using PDCs over conventional Silicon Photomultiplier (SiPM) for neutron imaging systems.

The basic building blocks of analog SiPMs and PDCs are Single-Photon Avalanche Photodiodes (SPADs). The main difference between conventional SiPMs and PDCs is in the fact that analog SiPMs sum the charge produced by individual SPADs passively, while in PDCs, each SPAD is read out individually by an active electronic circuit. Hence, PDCs provide a direct photon-to-bit conversion where a logic "1" means a detection in a given SPAD. Conversely, an analog SiPM requires a sophisticated preamplifier (current amplifiers or transimpedance amplifier) followed by a shaping amplifier and an analog-to-digital converter. Moreover, since the charge from each SPAD varies slightly, the passive sum of the analog SiPM will have signal fluctuations for the same number of photons detected. This is one of many issues that is eliminated by individual one-to-one SPAD read out in PDCs.

The large area required for scintillator readouts for neutron imaging is such that the output capacitance of large area SiPM arrays is very high. This creates a burden on the signal-to-noise optimization with respect to the power budget. For PDCs, the power consumption is dictated by the rate of the incident photon flux, or in photon-starved environments, the dark noise rate of the SPAD array. In other words, the power consumption in the absence of events is extremely low. Hence, the power consumption of a PDC read out system is much lower than its analog counterpart for all practical incoming rates. Further, the large SiPM capacitance may introduce signal distortions on the scintillator fast rise or decay time with undesired effects on timing and pulse shape discrimination. The problem is absent in PDCs, as their readout is independent of device capacitance.

Other advantages of PDC are:

- Excellent timing resolution.
- Digital signal processing embedded within the PDC.
- Ability to control individual SPADs, including selectively turning off faulty or radiation-damaged SPADs.
- Built-in modularity for system level scaling.

UdeS is the world leader in 3D vertical integration of frontside illuminated SPAD arrays over complementary metal-oxide semiconductor transistor (CMOS) readouts. These capabilities allow future production of "3D PDC" with maximum photosensitive fill factor and electronic functionalities tailored to the application. UdeS's vast knowledge of SPADs and CMOS design made the team an ideal collaborator in the development of large area, high-resolution fast neutron radiography.

1. OVERVIEW OF THE PROJECT

In the present Life Cycle Plan, ORNL, in collaboration with UdeS, took on the task of designing and producing a tile of PDCs, including the tile controller, to demonstrate the feasibility of PDC devices for

instrumenting readout of large scintillator panels. The project was organized in tasks over a two-year period. The purpose of this two-year study was to demonstrate that the approach can be extended to arbitrarily large tile sizes (or arbitrary number of tiles). The work was organized in the following tasks.

Task 1 (FY21): Performance measurements extension – Replicate Sherbrooke setup at ORNL and extend the Sherbrooke measurements to plastic scintillators.

Task 2 (FY21): Procurement of extra PDC devices – Fabricate PDC v2, an improved version of the original UdeS PDC design.

Task 3 (FY21): Concept tile design – Design a 55x55 mm^2 concept tile.

Task 4 (FY21 and FY22): Tile controller design – Design and simulate the tile controller for the concept tile. The tile controller performs the logic that collects information from a tile of PDCs and sends it to a computer for processing.

Task 5: (FY22) Integration of concept tile with scintillators – Build and integrate the concept tile with plastic scintillators.

Task 6 (FY22, extended to FY23): Tile controller construction and testing – Build the tile controller, later extended to development of the ASIC that includes Time-to-Digital functions (TDC).

Task 7 (FY22, extended to FY23): System integration and demonstration.

1.1 TASK COMPLETION

1.1.1 Task 1, Performance measurements extension

Status: Complete.

The team designed a test platform for the PDC-V1, the first version of the PDC, for ORNL so that measurements could be replicated and later extended to relevant setups. The test platform is based on a commercial Xilinx Zynq UltraScale field programmable gate array (FPGA) development kit along with custom designed printed circuit boards (PCBs) to interface with the PDC-V1. Figure 1 shows the test platform in detail.

UdeS provided the PDCs-V1 to assemble the 2 × 2 Heads and, with ORNL, managed the PCB design, fabrication, assembly, and fabrication. Figure 1 shows a photodetection module with 1 FPGA board, 2 adapter boards and 2 heads. ORNL completed a set of measurements that, for the first time, showed scintillation photons being detected by the PDCs. Timing measurements were also performed, and all measurements have extended applicability to the final task of this project. Details will be discussed in such task.

Key milestones:

- Head and adapter PCB-V1 assembled in March 2021
- Adaptor powered in March 2021
- First tests with PDC-V1 and the new setup performed in April 2021

- System completed in April 2021
- System shipped to ORNL in May 2021
- Measurements completed and later extended to an 8×8 tile for final project task.

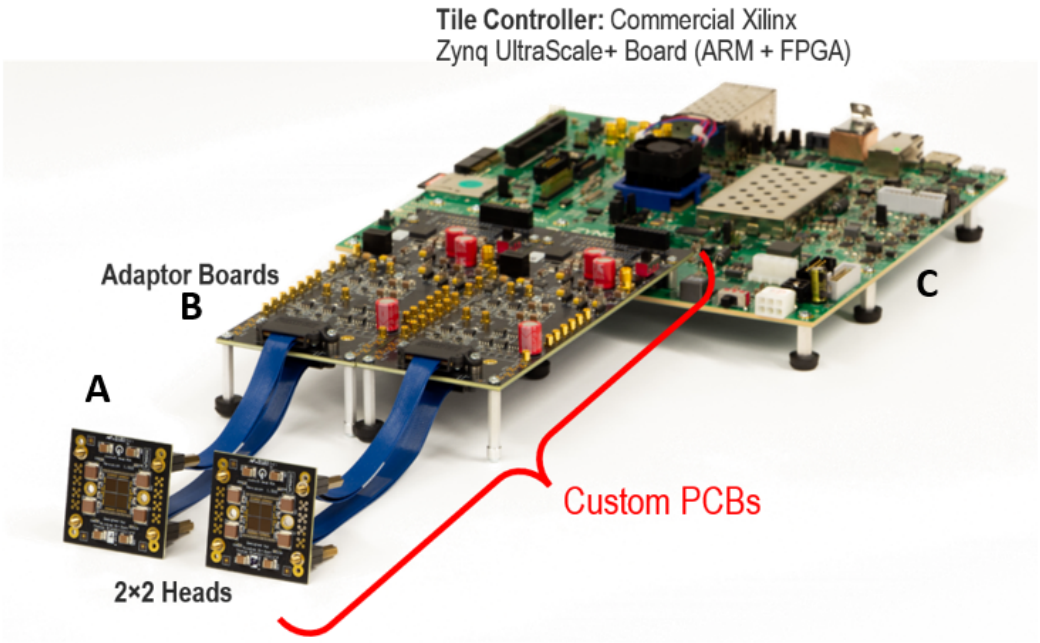

Figure 1: Photograph of the 2x2 test platform based on PDC-V1. PDC-V1 chips are mounted on 2×2 arrays (boards 'A'). Adapter boards (B) interface signals between the FGPA development board (C) and the PDC arrays. They also provide bias to the PDCs.

1.1.2 Task 2, Procurement of extra PDC devices

Status: Complete except for some firmware

Based on experience with the PDC-V1, the team designed and fabricated wafers of the PDC-V2. This revision lowered the number of I/O connections to enable large-scale tile integration of PDCs required by the long-term objective for fast neutron imaging system developed at ORNL. The revision also put efforts on lowering the power consumption of the PDC and correcting minor bugs identified in the PDC-V1.

To test the PDC-V2 and validate the proper operation, the design of the Adaptor PCB and the Head PCB of Task 1 was revised, along with the firmware of the FPGA development kit.

A head with a 2×2 array of PCB-V2, another with an 8×8 array of PDC-V2, and an adapter PCB-V2 were modified from the V1 design at no additional cost to the project.

Key milestones:

- PDC-V2 4×4 CMOS shot sent for fabrication in March 2022.

- PDC-V2 PCBs design completed (2×2 Head & Adaptor, 8×8 Head & Adaptor) in March 2022.
- PDC-V2 PCBs sent for fabrication in April 2022.

In order to share the same architecture and data management as in the tile controller ASIC that the team is working on in a parallel project OR23-3D PDC-PD2Ja funded by the Near Field Detection Portfolio, the digital sum readout remains to be completed. By sharing the same firmware code, maintenance will be more efficient, enhancing the features of the system in this project.

1.1.3 Task 3, Concept tile design

Status: Complete.

This concept tile is the foundation for future large-scale integrations of PDCs into large area, fast neutron imaging instruments. The 8×8 tile was designed along with the required adapter PCB to interface with the Xilinx FPGA Development kit. At this stage of the project, the FPGA on the Xilinx Development kit is used as a tile controller and was chosen based on the following trade-offs. The FPGA used in this project has the largest number of I/Os available commercially in a development kit format (see Figure 1). The number of I/Os limits the number of PDCs the controller can manage. Using a larger FPGA would require the design of a complex and high-risk PCB. It would also bring high power dissipation near the PDC, which is undesirable for SPAD operation.

Tiles of 2×2 and 8×8 PDC-V2 were assembled using PCBs fabricated in Task 2. This system was the subject of a presentation at the 2022 IEEE NSS MIC RTSD: N. Roy et al. “Towards Large-Scale Photosensitive Area with Photon-to-Digital Converter-based Module”, IEEE NSS MIC RTSD, Milan, Italy, 2022.

Key milestones:
- PDC-V2 PCBs: Design of the assembly fixtures: Nov 2021.
- PDC-V2 PCBs 2×2 Head & Adaptors received and assembled in July 2022.
- PDC-V2 PCBs 8×8 Head received and assembled in September 2022.
- Presentation of the system at the NSS MIC RTSD 2022.

A photograph of an 8×8 tile is shown in Figure 2.

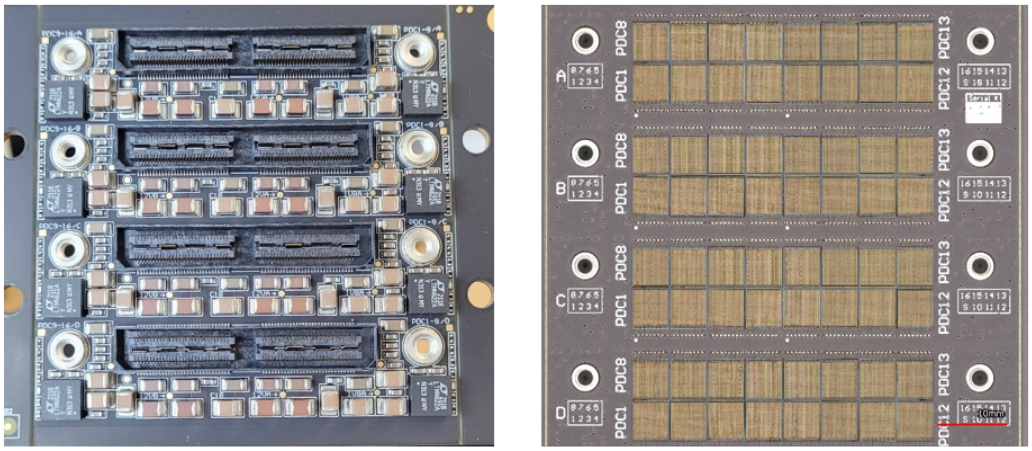

Figure 2: Bottom (left) and top (right) 8x8 PDC-V2 tile fully assembled.

1.1.4 Task 4 and 6, Tile controller design, tile controller construction and test

Status: Complete.

The tile controller functions were all successfully designed for the FPGA-based controller in Task 3. The bulk of the work focused on the time-to-digital converter (TDC) section. A 32-channel TDC with sub-100 ps timing requires substantial resources in the FPGA. This is an important issue, knowing that at least one TDC per PDC is required to timestamp incoming photons with minimal dead time. Such a system was developed and documented in a presentation at the 2022 IEEE NSS MIC RSTD: A. Samson et al. "A sub-100 ps Resolution 32 Channel TDC Platform Based on Xilinx UltraScale+ Architecture", IEEE NSS MIC RTSD, Milan, Italy, 2022.

Upon testing, the TDC achieved a resolution of 72 ps, a precision of 31 ps and a root mean square (RMS) differential nonlinearity (DNL) of 0.015 least significant bit (LSB).

Key milestones:

- SMA-to-FMC PCB design review in April 2021.
- SMA-to-FMC PCB assembly in July 2021.
- FPGA TDC Design completed in July 2021.
- FPGA TDC Design optimized in September 2021.
- FPGA TDC Design – 32 channels in September 2021.
- FPGA TDC Design—Ready to be integrated in June 2022.
- Presentation at the IEEE NSS MIC RTSD 2022 in November 2022.

1.1.4.1 Task 6 extension

Status: Complete.

In the original statement of work, a tile of 8×8 PDCs controlled with a commercial FPGA platform acting as the tile controller was planned. The FPGA platform brings flexibility and reduces design time. On the other hand, the goal is to provide a modular photodetection system that can be expanded to larger tile sizes (~1000 cm^2). This cannot be achieved with an FPGA platform; therefore, a custom tile controller ASIC will need to be designed in the future. A key circuit in such device is a TDC with timing resolution below 100 ps r.m.s. This task was extended to explore the possibility of implementing such design.

UdeS is an expert at this type of designs, with a proven track record. Their unique TDC architecture previously showed a resolution of 50 ps with a timing jitter of 22 ps RMS, a DNL of 0.09 LSB and an integral non-linearity of 0.17 LSB.

Under this task, the team designed the TDC architecture specifically for our PDCs. Completion of the task was achieved by having a complete design that could later be sent out for manufacturing under the project supported by Obj. J.

1.1.5 Task 5, Integration of concept tile with scintillators

Status: Complete.

Integration of plastic scintillators with tiles was studied in detail during the execution of Task 1. The

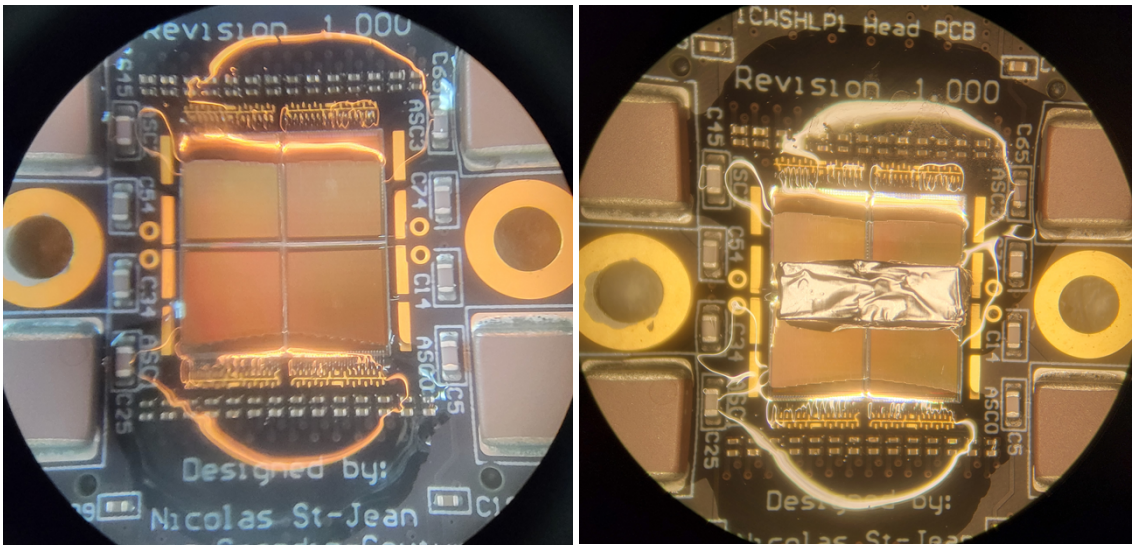

Figure 4: Microscope photograph of an array of PDC with the protecting compund applied (left) and with a small scintillator coupled via optical pads (right).

results apply directly to this integration task because there is virtually no change in geometry and constraints when integrating scintillators to PDC systems. The PDC chips are bare dies bonded to a

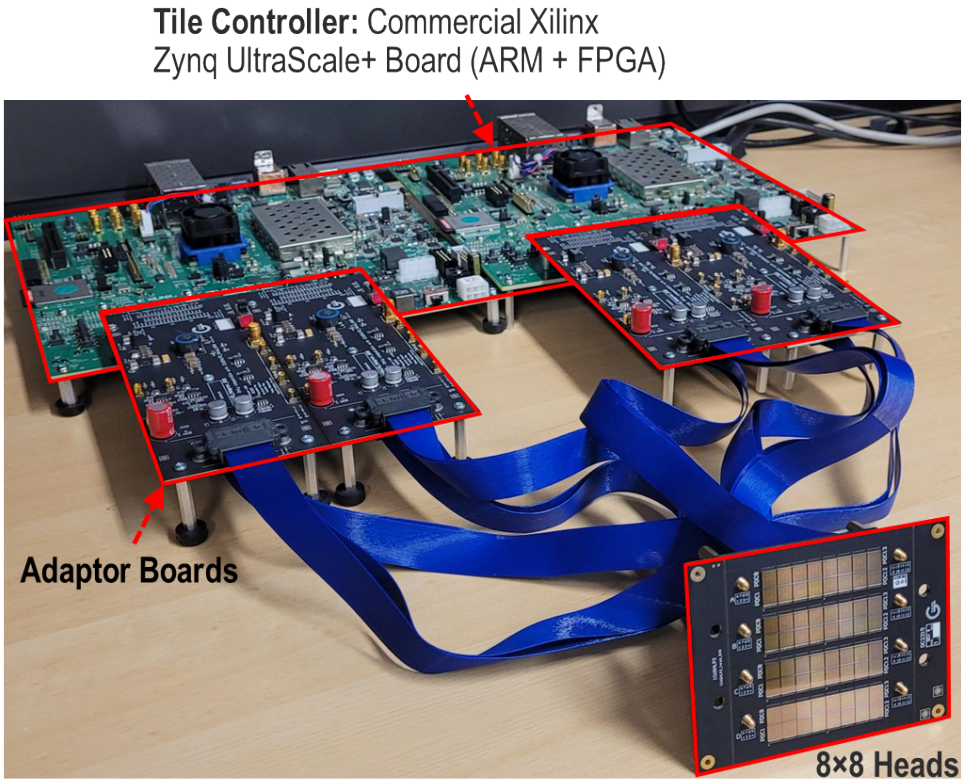

Figure 3: 8×8 Test Platform based on PDC-V2. The function of each board is similar to that described in Figure 1. The size of the 8×8 board is 94 mm × 74 mm.

printed circuit board, thus some protection must be offered so that the scintillator does not destroy bonds.

Further, the dies are coated in silicon oxide, therefore, a method of efficiently optically coupling PDC chips to the scintillator must be found.

In order to protect dies and bonds, we used MASTERBOND's UV22DC80-1, which is a UV and/or heat-curable compound with low viscosity (to penetrate under the wire bonds) and high transparency (to avoid blocking photons). Figure 4 left shows such compound applied to a PDC array.

With the compound applied, optical coupling is safely achieved using optical pads such as Eljen's EJ-560 or similar. Figure 4 right shows a small plastic scintillator coupled with such an optical pad on top of the SPAD arrays.

1.1.6 Task 7, System integration and demonstration

Status: complete, extended effort in project within Obj J

The 8×8 PDC tiles were integrated with two Xilinx FPGA Boards with the Adaptor board designed in Task 2. A picture of the complete system is shown in Figure 3.

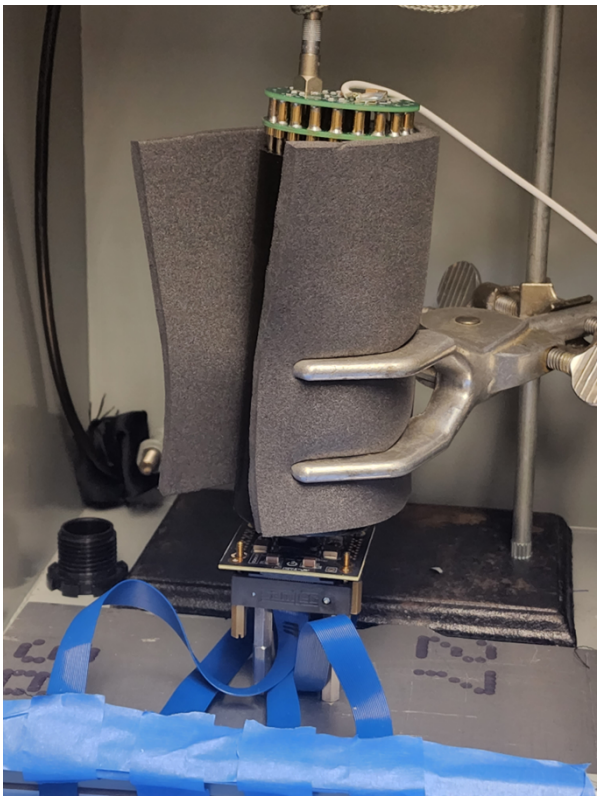

Figure 5: Coincidence set up in dark box.

On a fully wire bonded 8×8 tile, 2 banks were found faulty, meaning that it was not possible to configure all the PDCs in those banks. A bank consists of 8 PDCs with a daisy-chained configuration bus. If a PDC in the chain is faulty, the subsequent PDC cannot be configured. An investigation was started in early 2023 to identify if the problem is present at the wafer level or if it is caused by dicing, placement, wire bonding, manipulation, or misuse.

The investigation is still in progress within the scope of OR23-3D PDC-PD2Ja. However, defective PDCs seem to be limited to a small number of dies inside the 4×4 shot. Over 200 PDCs were manually probed on a probing station with 4 SMUs to power the PDCs. From those measurements, PDCs were tagged as faulty by criteria based on current draw or short-circuit behavior. UdeS designed a probe card to accelerate wafer probing in order to have a large statistical population. The probe card was received in April 2023. More results on this investigation will be done in the future under Obj. J. This effort hindered the final measurements to some extent because while partially working tiles are available, effort had to be diverted to the tests just discussed. However, as mentioned earlier, the geometrical differences between 2×2 and 8×8 tiles are irrelevant when it comes to testing the coupling with a scintillator and results would otherwise be redundant. Thus, the results obtained with 2×2 tiles coupled to the FPGA-based tile controller are discussed next.

For these measurements, the 2×2 PDC tile with scintillator prepared in Task 5 was coupled to a photomultiplier tube (PMT) for the purpose of providing a coincidence measurement (i.e., only the photons simultaneously seen by the PDC and the scintillator were recorded) in a dark box (Figure 5). This setup allowed clear identification of source interactions for the very first time using a PDC. Despite having only a handful of SPADs in each PDC (61), the output clearly showed multiple individual photoelectrons being produced by the PDC in coincidence with source detection (Figure 6).

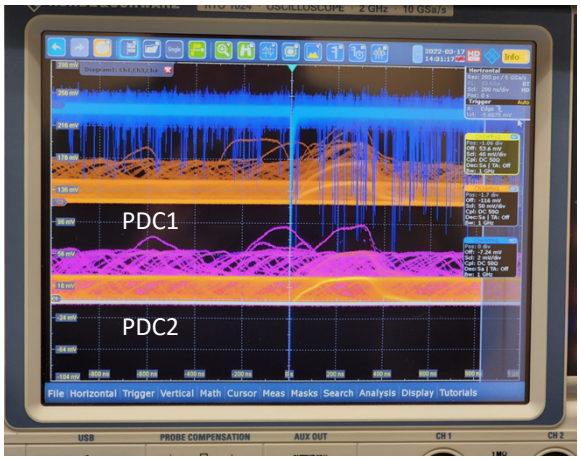

Figure 6: PMT/PDC coincidence detections as seen on an oscilloscope. PDC: orange and purple traces, PMT: blue trace.

Further, all readout functions were tested and found to be working. The measurements focused on acquiring the single photoelectron presence signal and time stamp on the PDC side, and light detection time stamp from the PMT side. The correlation between the time stamps was plotted for two different PDC chips. From the result shown in Figure 7, it is evident that the PDC devices provide excellent timing. The tail on the right side of the coincidence peak is attributed primarily to the intrinsic time dependence of the scintillation process. This may be stretched slightly by the relatively unoptimized optical coupling where photons arrive later due to additional path length from reflecting a few times in the optical interface before being detected. It should also be noted that the PMT

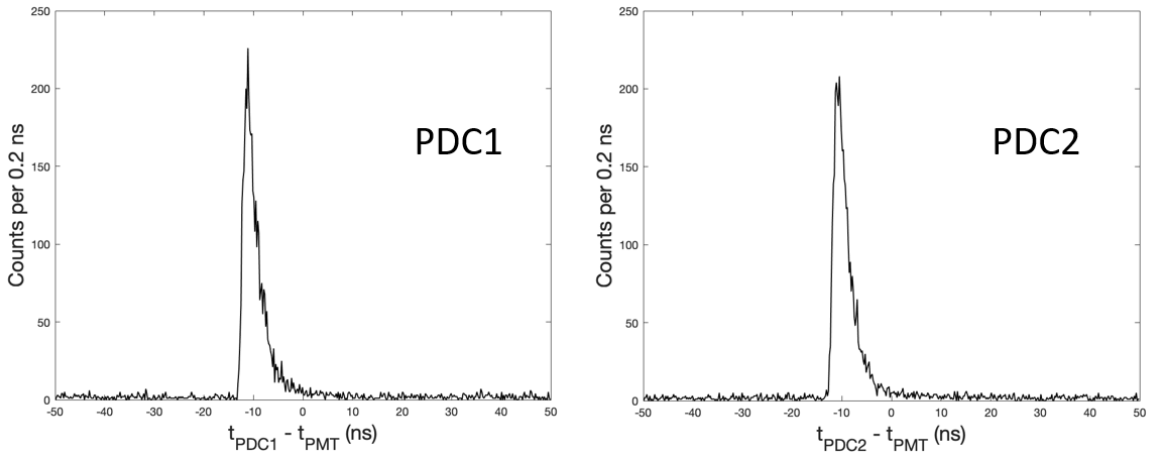

Figure 7: Timing coincidence plots of two PDCs in the array tested.

coincidence signal was taken as reference (0 s). With this choice, the timing peak occurs at a negative time value. This can be explained by considering that the PMT signal contains the transit time of the charge generated in the anode across all dynodes. While such time is typically of the order of a few 10's ns in PMTs, in PDCs the transit region is extremely small (<μm), thus there is no appreciable transit time. It is important to note that, while interesting and relevant to the specific PMT coincidence measurement, these effects do not bear appreciable consequences when a full PDC array, not just a unidimensional line, is available from future developments. Another important observation is that the timing obtained, while remarkable, is still limited by how well the prompt PMT signal can be detected by the coincidence

electronics. This means that the intrinsic PDC timing may even surpass the performance shown in Figure 7.

CONCLUSIONS

ORNL established a collaboration with the Université de Sherbrooke to demonstrate the feasibility of photon-to-digital converters in fast neutron radiography. The devices offer unprecedented advantages over conventional photon detectors thanks to their intrinsic digital nature. The effort, initially planned over the course of two years, was extended for an additional six months as more opportunities for additional developments arose. Over the course of the period of performance, all goals were achieved. This placed the team in a favorable position to pursue the next step towards the adoption of this new technology by the community, which is to advance the design to true three-dimensional (3D) devices where the SPAD array is placed on top of the electronics readout. This arrangement allows for a high fill factor and complete modularity. Thanks to a task extension by the sponsor, the tile controller has been designed into an application-specific integrated circuit. This is another step towards large arrays of PDCs. The success of this project was such that it stimulated interest within the Near Field Detection Portfolio, resulting in a new, five years project to pursue 3D integration of the devices in the OR23-3D PDC-PD2Ja project. Efforts on the new project will heavily leverage the progress made in this work, resulting in fully integrated 3D PDC tiles with ASIC tile controller, ready to be the building block of large arrays of photodetectors.