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Development of a Radiation-Tolerant Front End Digitizer

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OAK RIDGE National Laboratory

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ABBREVIATIONS

ADC	analog-to-digital converter
AFE	analog front end
ASM	astable multi-vibrator
COTS	commercial-off-the-shelf
EMI	electromagnetic interference
FREND	Front End Digitizer
GaN	gallium nitride
GPIO	general-purpose input/output
I&C	instrumentation and control
JFET	junction-gate field-effect transistor
LED	light-emitting diode
MCU	microcontroller unit
MOSFET	metal–oxide–semiconductor field-effect transistor
NPP	nuclear power plant
PCB	printed circuit board
PWM	pulse-width modulation
rad-hard	radiation-hardened
RC	resistor-capacitor
RTD	resistance temperature detector
SEB	single-event burnout
SEE	single-event effect
SiC	silicon carbide
SPGD	self-powered γ detector
SPND	self-powered neutron detector
TDM	time-division multiplexing
TEG	thermo-electric generator
TID	total ionizing dose
TTL	transistor-transistor logic
UART	universal asynchronous receiver-transmitter
WBG	wide bandgap

ABSTRACT

High-radiation and high-temperature environments represent notoriously detrimental conditions for electronics. Yet sensors and instrumentation are critically important for the safe operation of nuclear reactors and for the validity of the scientific experiments conducted within them. Traditionally, sensors in such extreme environments operate with few active components, resulting in small signals (mV–V, nA–μA range) that must be transmitted through long cable runs before digitization by sensitive data acquisition systems located in clean, less-harsh environments. Long cables are prone to picking up noise through electromagnetic interference and distortion caused by their parasitic impedances, resulting in signal degradation. The Front End Digitizer (FREND) system described and demonstrated herein seeks to address these issues by enabling the placement of a radiation-resistant analog front end within reactor containment, or other high-radiation environments. FREND will enable early signal pre-amplification, digitization, and optical encoding within the high-radiation field to transmit sensor signals over an optical fiber to the non-nuclear environment of an instrument room. Early signal pre-amplification and digitization maintain signal integrity, whereas optical transmission renders the system blind to induced electromagnetic noise over the long cable runs. This report describes the FREND initial prototype, which can multiplex and optically encode data from up to four sensor inputs, though, in principle, this can be extended to any number of sensor inputs. The end result is an extremely flexible, high-fidelity system.

1. INTRODUCTION

Instrumentation in nuclear reactors is critical both to their safe operation and to the validity of the scientific experiments performed therein. A suite of flow meters, temperature sensors, pressure sensors, strain sensors, neutron and γ detectors, and other sensors comprise the instrumentation and control (I&C) used to monitor operation and heat removal from a reactor core. Due to the high levels of γ and neutron radiation (10^{10}–10^{11} n/cm^2/s) and temperatures above 350 °C, these sensors must also be sufficiently robust to withstand these conditions [1, 2]. To aid in their robustness, sensors are generally passive, and data acquisition performed by instruments is located far from the actual sensor, behind shielding. Consequently, the electrical signals these sensors produce are generally low amplitude—often on the order of mV–V or mA–μA—may be transmitted through penetrations in the reactor containment, and must be transmitted over hundreds of meters of electrical cables before digitization using a data acquisition system in a non-nuclear environment, which contains sensitive electrical components. The reactor and facility penetrations required for these complex cable runs introduce points of failure and increased inspection and maintenance costs. Additionally, long cable runs allow for electromagnetic interference (EMI) injection, signal distortion, and transmission line losses, which degrade the transmitted signal.

In non-nuclear applications, sensor signal pre-amplification and digitization occur as close as possible to the physical sensor mechanism to maintain signal fidelity. However, the high-temperature and high-radiation environment present in and around nuclear reactors has been shown to quickly damage electronics [3]. Solid-state semiconductor transistors are the most common point of failure of electronic circuits in high-radiation environments. Field effect transistors are sensitive to the charges produced by ionizing radiation. These charges often become trapped in the forbidden gap in insulators, leading to errant operation of the transistors, such as threshold voltage and transconductance variations [3, 4]. In large ionizing radiation fluxes, the sudden surge of charges produced and trapped by the incident particles leads to erroneous bit-flip errors in digital logic devices, which are known as *single-event effects*, *single-event upsets*, and *single-event latchups* [4]. Ionizing radiation also induces stray currents in semiconductors and

insulators, which influence operation of bipolar junction transistors. Passivation layers in commercial-off-the-shelf (COTS) transistors intended for non-nuclear environments are not optimized or specified for radiation-intensive applications. Gate oxides, shallow trench isolation islands, and spacing oxides are susceptible to charge trapping [5]. These regions trap charges on the semiconductor surface, leading to erroneous device performance through biasing the semiconductor material and creating parasitic surface paths for leakage currents [4]. Additionally, neutron irradiation introduces displacement damages that create vacancies in the semiconductor lattice structure and transmutation effects, thus changing the device's dopant profile. Neutron activation also leads to the production of secondary ionization trails, which often lead to single-event burnout and single-event gate rupture. Both of these failure modes are fatal to the device. Neutron irradiation studies of silicon carbide (SiC) transistors have been the subject of recent research interest, especially in relation to commercial power devices. Of SiC devices, SiC metal–oxide–semiconductor field-effect transistor (MOSFET) power devices have been studied the most extensively [6, 7]. Failures occurring at neutron fluences of 10^5–10^9 n/cm^2 are common for these devices, though the specific mechanisms leading to these failure modes are still active research fields [8–12]. In contrast, junction-gate field-effect transistors (JFETs) are extremely insensitive to ionizing radiation due to the absence of an insulating gate and limited interfering surface effects typically created by insulating overlays [3, 4, 13]. Though they are niche in modern electronics, JFETs have been shown to be resistant to $>$ 1 MGy (Si) irradiation [13–16]. This rad-hard behavior is attributed to their simple design and lack of a gate insulator; they function based on the generation of an electric field to limit current flow through the device. SiC JFET-based electronics have been utilized in aerospace for their radiation tolerance to improve the survival of avionics instrumentation, which are designed to survive $>$ 60 kGy total ionizing dose (TID) and $>$ 400 °C [17–19]. The robust field performance of these critical avionics systems suggests that JFET-based electronics could also improve signal transmission in I&C systems in reactor facilities.

To realize the benefits of JFETs toward developing a means of preserving small signal fidelity in nuclear power plant (NPP) facilities, a system has been developed to convert signals from an array of sensors into optical signals. The Front End Digitizer (FREND) (block diagram shown in Figure 2) seeks to improve the fidelity of sensor signals originating within high-radiation environments and minimize the containment penetration count by enabling the placement of a radiation-tolerant analog front end (AFE) within containment. This is achieved through pre-amplifying and digitizing the sensor signal as close as possible to the sensor mechanisms, limiting the exposure to EMI. The amplified signals then transmit these data over optical fibers, which are EMI immune, to an instrument room. The FREND system, can multiplex and encode an array of sensors—up to four different sensors in the present implementation—for transmission over a an optical fiber. The FREND system is targeted to include multiple types of sensors, including thermocouples, thermistors, and particle detectors (e.g., self-powered neutron detectors (SPNDs), self-powered γ detectors (SPGDs), and fission chambers operating in current mode). The end result is an extremely flexible, high-fidelity system that requires fewer containment penetrations than conventional systems.

FREND is targeted to be radiation-hardened (rad-hard) to TIDs on the order of 1 MGy. The analog multiplexer and optical transmission circuitry are designed using components demonstrated by Reed et al. to be radiation tolerant [16, 20]. The AFE of FREND was designed using low-cost, discrete JFETs for the proof-of-principle prototype design described here. However, the silicon-based JFETs chosen are unverified under neutron irradiation and are not expected to exceed the state-of-the-art neutron fluence limit of 10^{14}–10^{15} n/cm^2 [3]. It is feasible to increase this limit by switching to a wide bandgap semiconductor material and increasing the dopant levels [3, 21] or positioning the FREND system further from the

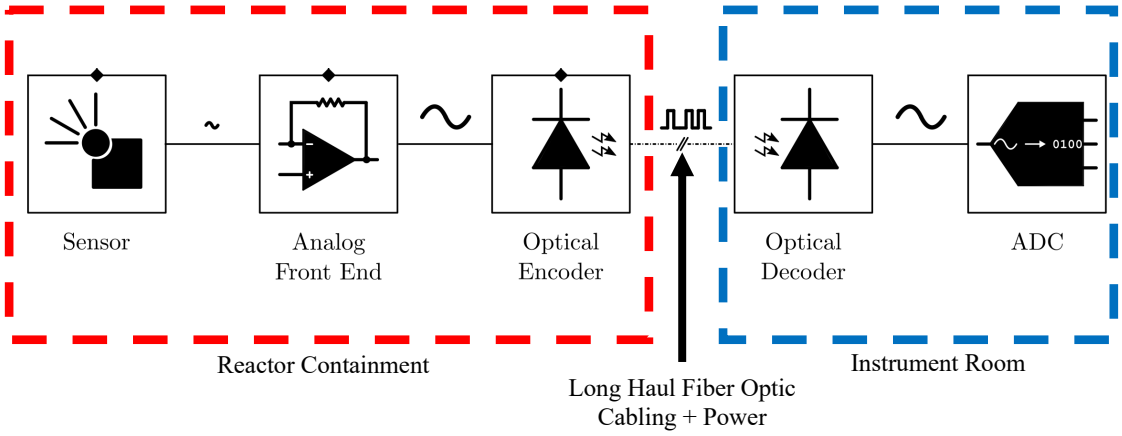


Figure 1. Flow diagram of the FREND system. The red dashed box indicates the portion of FREND inside of radiation containment. The blue dashed box represents the portion located in a control or instrument room.

radiation source to extend it's operational lifetime. However, while the neutron fluxes outside the reactor vessel where the FREND system is intended to be installed are several orders of magnitude lower than the flux in the core, the system must still survive non-trivial neutron fluxes in order to minimize cable length.

Optical telecommunication fibers have been developed specifically to address the concerns related to EMI-induced noise and signal losses that pose challenges in conventional metallic cabling. Light optical fibers provide low signal dispersion, are EMI-immune, have a small footprint, and have been demonstrated to be robust in temperature extremes, high strain, and under irradiation [22–24]. However, many optical fibers darken when exposed to high doses of ionizing radiation. To realize the benefits of fiber optic signal transmission, FREND encodes optical signals in time, rather than optical intensity, using pulse-width modulation (PWM). PWM pulse trains can then be demodulated by remotely located instruments using a low-cost timer-based system such as a microcontroller, enabling the reconstruction of the original signal.

Using a PWM-based scheme to transmit data also serves to convert the time-encoded analog signal to a digital signal interpretable by modern electronics. Digitizing a PWM signal is possible even with low-end microcontrollers using an interrupt capture timing peripheral, rather than requiring high-end analog-to-digital converters, which are found in conventional nuclear instrumentation. Because PWM encodes the relative amplitude of an input signal with a higher frequency carrier signal, the data are, by definition, split into discrete packets, separated by rising- and falling-edge pulses, proportional to the amplitude of the input signal over that time period. This is especially useful in high-radiation and other extreme environments that alter the transmissivity of optical fibers. Instead, using PWM requires only that the transition between high and low logic levels be reliably resolved. In addition to time encoding, the FREND system is capable of transmitting signals from up to four individual sensors simultaneously using time-division multiplexing (TDM). TDM, in combination with PWM encoding, involves encoding one or more measurements from each input sensor in discrete temporal windows, which are transmitted sequentially before being repeated. The time domain windows used in a TDM scheme must reflect the sensors' response time, but it can be easily implemented to provide updates from an array of sensors on the order of < 10 ms (> 100 Hz). In this manner, TDM followed by PWM enables an array of sensors to be multiplexed for transmission over a single optical fiber.

To realize a system that mitigates the complications of long cabling runs and minimizes cable penetrations, a JFET-based FREND concept instrument has been designed, fabricated, and bench-top tested. The FREND system is designed around discrete JFET devices that convert the analog signals from an array of sensors to the PWM-encoded signal and drive a light-emitting diode (LED) to convert the encoded electrical signals into optical signals, which are then transmitted to a data acquisition system over a fiber optic cable. The system-level implementation of the signal multiplexing, analog-to-optical conversion, and digital data acquisition are described and analyzed. Design equations, circuit simulations, and data acquired from bench-top testing of a prototype system are reported and discussed in the context of the present use case and future development targets. The circuitry required to multiplex these signals using TDM and encoding them using PWM for transmission has been simulated and fabricated on printed circuit boards (PCBs) to demonstrate the end-to-end feasibility of this approach as part of the fiscal year 2022 statement of work. The FREND system described here is, to the authors' knowledge, a first-in-class device designed to be readily integrated into existing instrumentation suites in radiation environments, where it can improve sensor signal integrity and data acquisition.

2. THEORY OF OPERATION

2.1 INSIDE OR NEAR REACTOR CONTAINMENT

2.1.1 Analog Multiplexer

The FREND system was designed around a JFET-based analog multiplexer subsystem to enable data acquisition from an array of sensors (Figure 2). The proposed system can accommodate up to four sensors in its present embodiment, but the system can be extended for use with 2^N total sensors through TDM, where N is the bitwidth of a counter. This is performed by generating a square wave used as a clock signal (CLK_A) from one leg of a JFET-based astable multi-vibrator (ASM) and then dividing its frequency down 2^M times to the desired modulation frequency. These circuits comprise the clock signal generator subsystem. In the present case, the clock signal is divided down four-fold ($M = 2$) to 2 kHz. Meanwhile, an N-bit counter is used to sequentially switch through the sensors using an analog multiplexer.

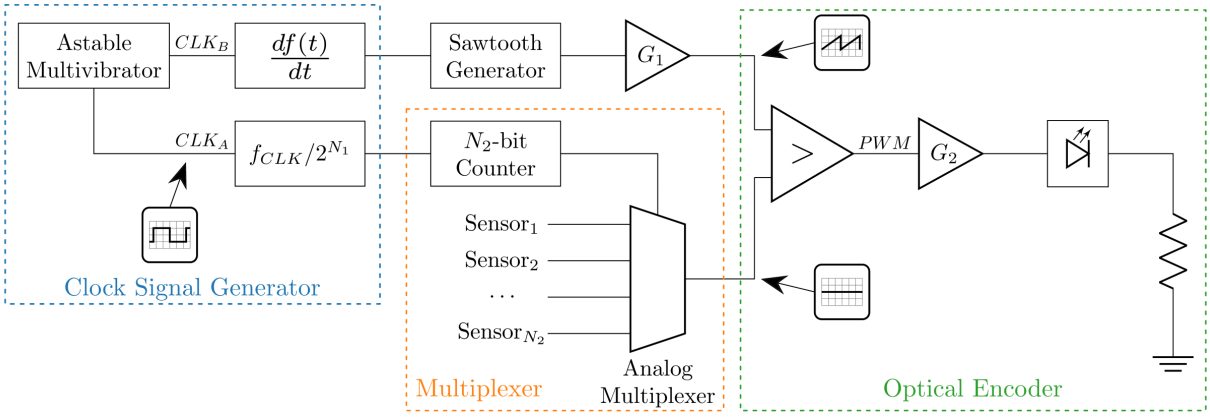


Figure 2. Circuit diagram of the FREND system.

More formally, let $X_n(t)$ be defined as the output voltage from sensor n, which exists within an array of N

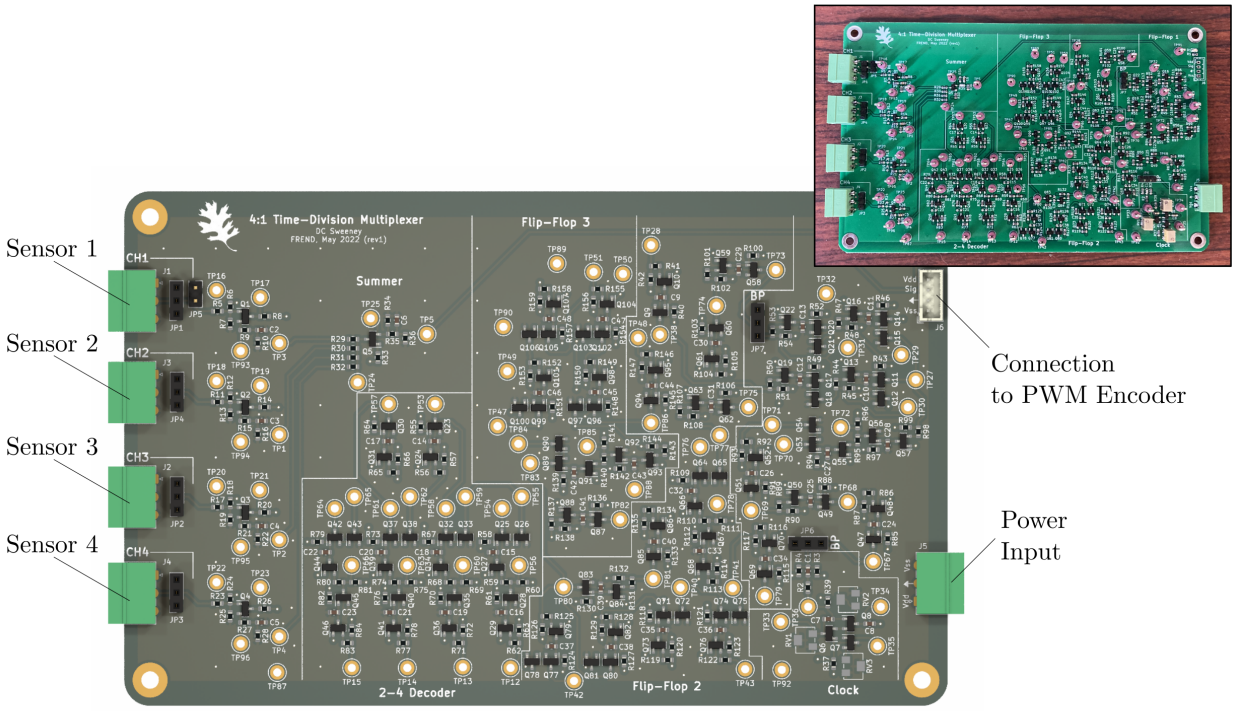


Figure 3. Four-channel analog multiplexer circuit board design with inset photo of the assembled prototype.

sensors. Let $G(t)$ be a AC-coupled pulse wave

$$G(t,\theta) = \frac{2A_g}{\pi} \sum_{i=1}^{\infty} \frac{1}{i} \sin(\pi i \tau) \cos(2\pi f_g i t - \theta), \tag{1}$$

where $\tau = t_{on}/(2^{N_1}T)$ is the duty cycle with on-time t_{on} and period T, amplitude A_g, frequency f_g, and phase shift θ. For TDM, $G(t,\theta)$ can be used as a modulating function if $A_g = 1$ and θ is varied according to the modulating scheme, which is $\theta_n \in \{2\pi n/N \mid \forall n \in N\}$ in the present case. For a TDM signal acquired from an array of N sensors, the output voltage from the analog multiplexer $M(t)$ is given by

$$M(t) = \sum_{n=1}^{N} G(t,\theta_n) X_n(t), \tag{2}$$

where the signal at θ_N is reserved as sequence flag to indicate the ending of one sequence of measurements and the beginning of the next.

2.1.2 Optical Encoder

The analog multiplexer output $M(t)$ is compared to a rising-edge sawtooth waveform generated from the second leg of the same ASM (CLK_B). The CLK_B is differentiated to produce an impulse that rapidly charges a capacitor. This capacitor then slowly discharges across a parallel resistive load. If the time

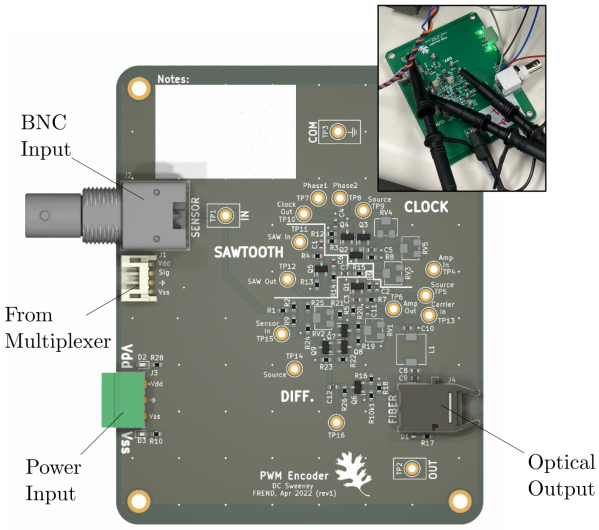


Figure 4. Optical encoder circuit board with inset photo of the assembled prototype.

constant of the resistor-capacitor (RC)-network is sufficiently large, then the voltage drop across the capacitor will appear linear. Let the rising-edge sawtooth modulating signal $C(t)$ be represented as

$$C(t) = -\frac{2A_c}{\pi} \arctan\left(\cot\left(\frac{\pi t}{T}\right)\right), \tag{3}$$

where T is the period of $C(t)$. To optically encode $M(t)$, a PWM scheme was adopted, as shown in the optical encoder subsystem (Figure 2). In PWM, a zero-offset bipolar signal of interest is compared against a triangle wave of a slightly larger peak-to-peak amplitude. The output is a binary signal with the ratio of the on-time to total period providing an approximation for the signal of interest over the PWM period. The idealized output of the PWM encoder ($V_{pwm}(t)$) can be represented as

$$V_{pwm}(t) = H(C(t) - M(t)), \tag{4}$$

where $H(\cdot)$ is the Heaviside step function, and V_{pwm} is the output of the comparator signal. V_{pwm} is ideally encoded in the binary set $\{V_0, V_1\}$, where V_0 and V_1 are analog voltages corresponding to a logical low (V_0) and high (V_1). After encoding, this PWM voltage is amplified and buffered to drive an LED to produce an optical signal I_{pwm} with intensities corresponding to V_0 and V_1 that can be coupled to and transmitted along an optical fiber.

2.2 OUTSIDE CONTAINMENT

2.2.1 Acquisition Circuitry

The PWM signal through the optical fiber–coupled LED (I_{pwm}), transmitted from the FREND AFE received and demodulated by data acquisition hardware in a benign environment. Several methods exist for demodulating the original signal $X_n(t)$ from an encoded PWM signal, such as low-pass filtering (integration) to remove carrier wave frequency. Low-pass filtering of a PWM signal requires a filter stage with a cut-off frequency between the maximum frequency content of the input signal $X_n(t)$ and half the

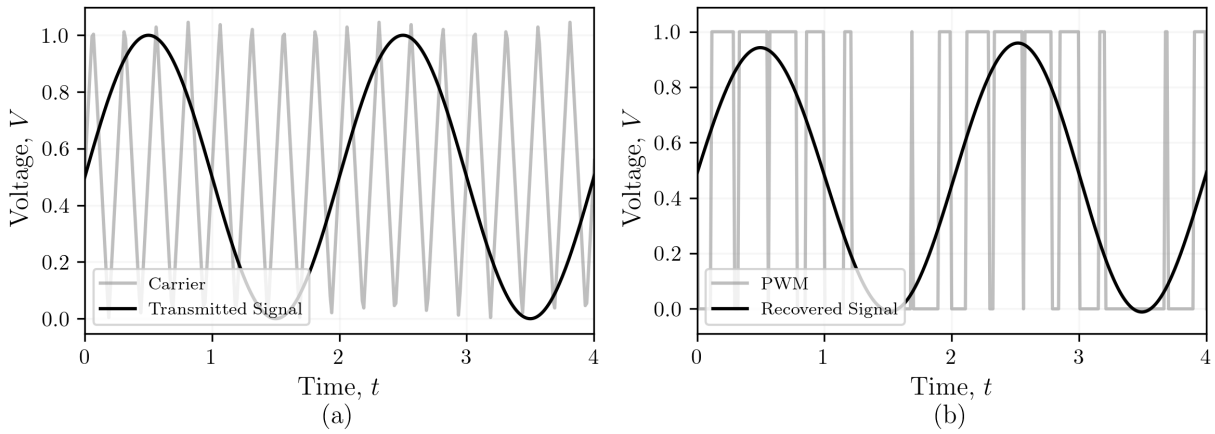


Figure 5. Example PWM waveform with a symmetric triangle carrier wave encoding a sinusoidal wave with a slightly lower peak-to-peak amplitude.

(higher) frequency of the triangle wave to which it is compared. This filtered signal can then be digitized using an analog-to-digital converter (ADC). Though effective, this process ultimately incurs the additional cost of an ADC and may reduce the operational bandwidth overhead as a result of the digital communication between the ADC and microcontroller or microprocessor.

To ameliorate bandwidth challenges, the FREND data acquisition system has been designed to take advantage of the binary nature of the optical intensity of the received PWM-encoded signal. An input capture interrupt on a microcontroller unit (MCU) counter with a clock speed of 80 MHz was configured to utilize a free-running increasing timer which was itself configured to trigger on both the rising and falling edges of the input signal. A photodiode driving a transimpedance amplifier was used to convert I_{pwm} to a transistor-transistor logic (TTL) signal compatible with the input capture peripheral. Let the PWM signal $V_{pwm}(t)'$ be the voltage signal incident on the general-purpose input/output (GPIO) pin configured as the input capture interrupt. On the falling edge of $V_{pwm}(t)'$, the state of a digital counter at count c is stored ($c_{init} = c$), and an overflow counter is initialized to $k = 0$. Until a rising edge triggers a second interrupt, the MCU timer periodically counts until it reaches its maximum and resets to $c = 0$, at which point k is incremented. When a rising edge triggers $c = c_{\uparrow}$ and $k = k_{\uparrow}$ and a second interrupt, the total number of counts c_{low} while $V_{pwm}(t)'$ was in the logical low state can be written as

$$c_{low} = c_{\uparrow} + k_{\uparrow}(2^B) - c_{init}, \tag{5}$$

where B is the bit-depth of the timer. the timer c and overflow counter k continue incrementing following the rising-edge interrupt until a second falling-edge interrupt is triggered at $c = c_{\uparrow}$ and $k = k_{\uparrow}$. The total number of counts acquired during one period of the PWM signal c_{tot} can then be calculated in the same manner as Eq. (5), namely

$$c_{tot} = c_{\downarrow} + k_{\downarrow}(2^B) - c_{init}. \tag{6}$$

After c_{tot} is calculated, the overflow counter is re-initialized to $k = 0$, and the cycle restarts. However, in the present embodiment of the FREND system, $c_{tot} \leq 65535$, enabling each duty cycle measurement to be represented as the tuple (c_{low}, c_{tot}). The duty cycle $D(t)$ is proportional to the analog input voltage of the sensors normalized over the voltage range of the FREND AFE and transmission circuitry $\bar{G}(t, \theta)$ and is then

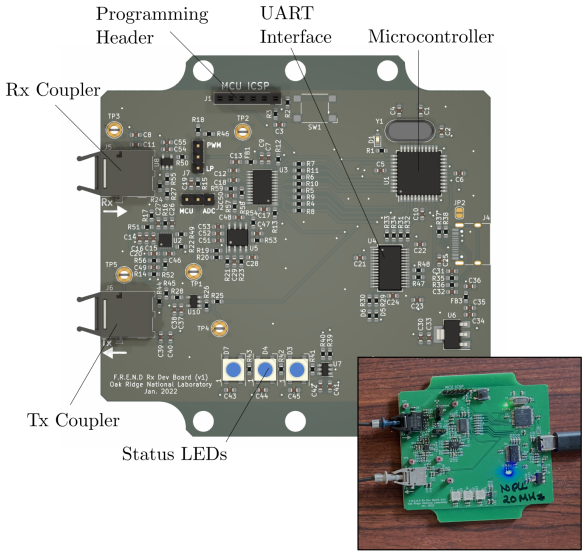


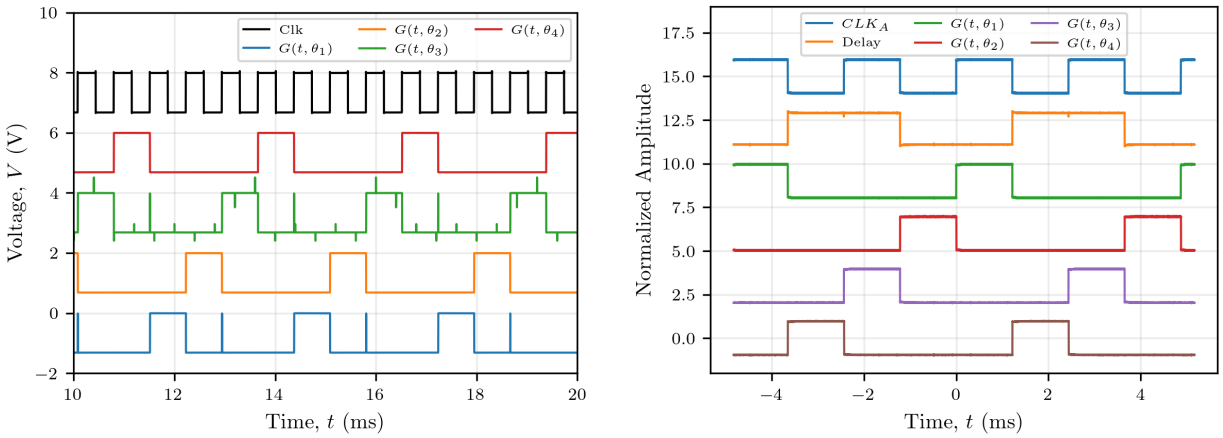
Figure 6. Optical receiver circuit board with inset photo of the assembled prototype.

calculated as

$$D(t) = 1 - \frac{c_{low}}{c_{tot}} \approx \bar{G}(t, \theta). \tag{7}$$

2.3 MATERIALS & METHODS

An analog multiplexer was constructed in LTspice (v17.0.35.0; Analog Devices, Inc., Wilmington, MA, USA) using the 2SK2394-6 model available from the manufacturer (ON Semiconductor Corporation, Phoenix, AZ, USA). Transient simulations were initialized at a DC state and run for 20 ms from startup to capture the 2 kHz ASM output and the PWM signal driving the fiber-coupled LED. KiCad EDA (v6.0.5) was used to design the PCBs. An AE3648A benchtop power supply (Agilent, Santa Clara, CA, USA) was used to supply ±3.3 V to PCBs during testing, and measurements were recorded using an MSO46 mixed signal oscilloscope (Tektronix, Beaverton, OR, USA). Sensor inputs were simulated using an 33500B waveform generator (Keysight, Santa Rosa, CA, USA). The optical demodulation and data recording was performed using a dsPIC33FJ128GP804 MCU equipped with a 20 MHz external oscillator and operated with a four-fold phase-locked loop multiplier (80 MHz). MCU firmware was written in embedded C in the MPLAB X IDE (v6.00; Microchip Technology, Inc., Chandler, AZ, USA) using the XC16 compiler (v1.70). The duty cycle was transmitted as two 16-bit integers c_{low} and c_{tot}, enabling a single tuple to be transmitted as four bytes. This transmission was facilitated over a 2.5 Mbaud universal asynchronous receiver-transmitter (UART) interface. A programming interface was developed in Python (v3.8.13) to facilitate data acquisition and easy integration with other systems. Thermal testing was performed on a hotplate (400 Hotplate/Stirrer; VWR Scientific Products, Radnor, PA, USA), and thermal imaging was performed using an infrared camera (FLIR-T62101; Teledyne FLIR, LLC., Wilsonville, OR, USA).



(a) Simulation **(b) Circuit**

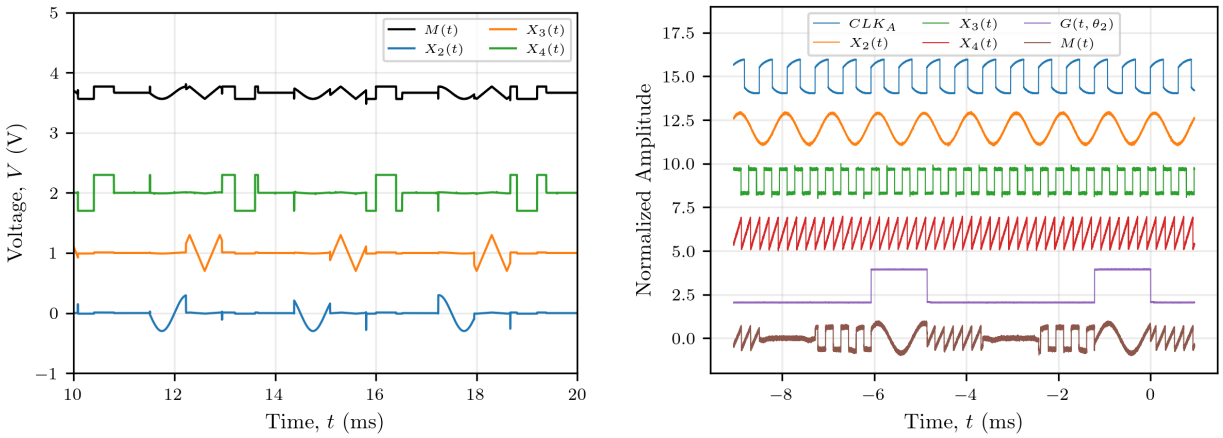
Figure 7. Comparison of the simulated output of the circuity used to sequentially enable each input channel (a) with its physical implementation (b). Note that an artificial offset was added to each of the traces to improve their visibility and comparison.

3. RESULTS

3.1 SIMULATION–IMPLEMENTATION AGREEMENT

SPICE circuit simulations were performed on the transistor level to inform the real-world analog design. An ASM at approximately 2 kHz, followed by two cascaded D flip-flops, each halving the clock frequency, were used to generate a 500 Hz enable signal for each channel of the analog multiplexer for the TDM (Figure 7). This signal was then used, in combination with a 2×4 decoder, to generate four sequential pulses. This signal was used to modulate the gate of a JFET positioned with its drain and source between the analog input channel and common voltage summer to enable each signal to be sequentially cycled at a rate of 2 kHz. The simulation of the decoder circuitry contained several errant signal peaks, particularly on the rising and falling edges of each of the phase-shifted enable signals (Figure 7(a)). These were attributed to a misrepresentation in the JFET model that did not accurately account for parasitic capacitances, as they were not present in the physical implementation of the circuitry (Figure 7(b)). The output signal from the decoder circuitry showed good agreement between the simulated and experimentally measured results. The resultant signal combines four input channels (including one null channel used for indexing and synchronization) into a single signal.

After the four decoder signals are generated, they are used to sequentially enable each of the four input channels to pass a signal through to the output of the analog multiplexer. To ensure that the analog multiplexer was designed correctly, each of the four input channels was set to produce different signals during the transient SPICE simulations: a sine wave for sensor 2, a triangle wave for sensor 3, a square wave for sensor 4, and a null (zero amplitude) signal on sensor 1. Figure 8(a) shows each input and the simulated output of the analog multiplexer; good agreement is demonstrated between each input channel and its multiplexed output wave shape. However, like the errant peaks in the enable signals (Figure 7(a)), several sharp peaks were observed during testing, especially at the transition between passing two input signals. This was attributed to the voltage summer circuit. These artifacts did not appear in the physical



(a) Simulation **(b) Circuit**

Figure 8. Comparison of the simulated output of the analog multiplexer circuitry (a) with its physical implementation (b). Note that an artificial offset was added to each of the traces to improve their visibility and comparison.

implementation of the analog multiplexer circuitry (Figure 8(b)), which accurately reproduced the signals passed through each of the four input channels.

After the signals entering the input channels are multiplexed, the multiplexed signal enters the optical encoder, where it is compared with a positively sloped sawtooth waveform with a slightly greater amplitude. The analog comparator is designed to output a logical high voltage when the input voltage from one of the sensors is greater than the sawtooth waveform and to output a logical low voltage otherwise—thus generating a PWM waveform with a duty cycle proportional to the input voltage (Figure 9). The PWM waveform is then used by an LED driver circuit to couple optical impulses from an LED into an optical fiber for transmission. The simulated PWM waveform contains artifacts on the rising edges of each of its constituent pulses, though these are most likely artifacts introduced during simulation.

In comparison with the simulated PWM-encoded data, the physical implementation of the PWM encoder did not produce the same rising-edge artifacts (Figure 10). However, similar lower-amplitude artifacts were present on the enable signal ($EN2$), though they do not appear to propagate through to the multiplexed signal (Figure 10(a)). Following encoding via a comparator, PWM-encoded signals transmitted along the optical fiber $V_{pwm}(t)$ and the signal received by the microcontroller $V_{pwm}(t)'$ exhibited clean, sharp edges that remove ambiguity in determining the location of each edge (Figure 10(b)). The PWM signal transmitted along and received after the fiber appeared substantially similar, suggesting that the optical fiber transmission did not significantly affect signal integrity.

Beyond comparing transmitting a PWM signal through an optical fiber, the digitization of the signal is critically important to demonstrate. In the present case, three different waveforms representing three different nuclear sensors, shown in Figure 11, were digitized using the scheme outlined in Section 2.2.1. Using this method, the input capture interrupt peripheral on the microcontroller was configured to use a 16-bit, 40 MHz free-running timer. The interrupt service routine produced an interrupt on both the rising and falling edges of the PWM signal received through the optical fiber, and these counts (c_{low} and c_{tot})

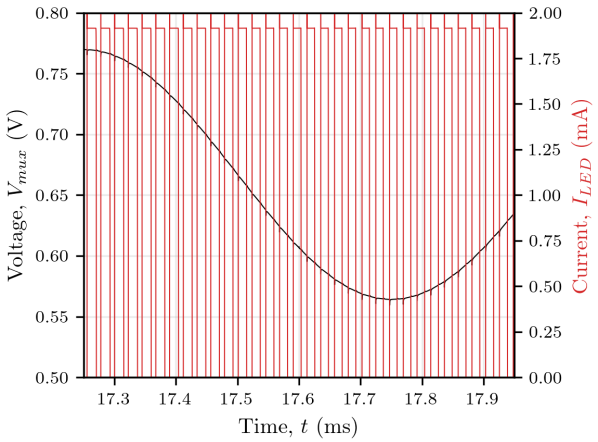


Figure 9. Simulation of the PWM current driving the LED used to transmit signals from the FREND system to the data acquisition system.

were transmitted to the host computer as two sets of two 8-bit integers comprising the most significant bits and least significant bits of the 16-bit counter-derived integers. These values were then converted to a floating-point duty cycle value before using Eq. (7); they were added to a queue to be written to a binary file. The resultant digitized data are shown in Figure 11.

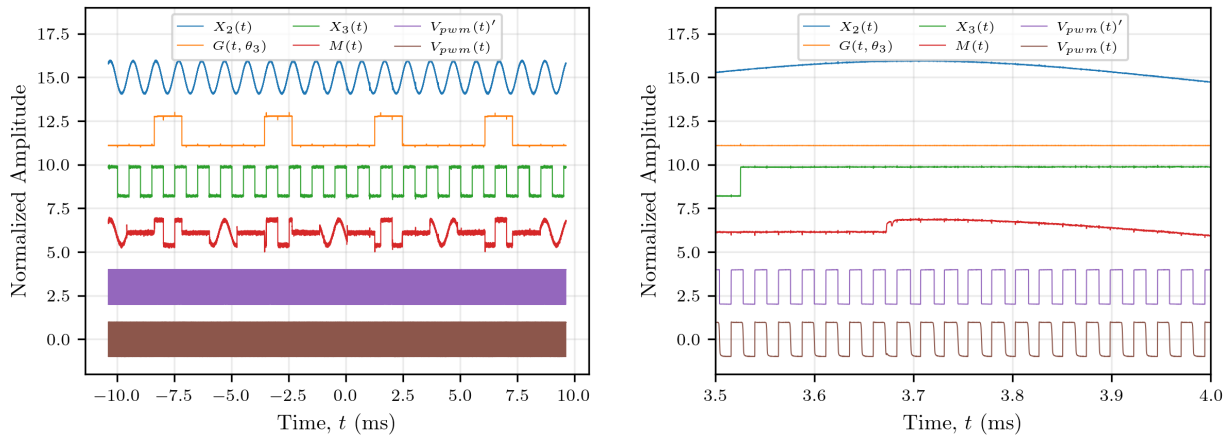
3.2 MEASUREMENT ACCURACY

The accuracy of the digitized measurements are innately subject to quantization error because digital values are represented as integer values. In the present case, the clock speed of the receiver and the PWM dictate the number of discrete integer values a digitized signal can receive. For an MCU with a clock speed of f_{MCU} and a PWM period of T_{PWM}, the ideal resolution χ_{res} of the input signal can be expressed by the reciprocal product $(f_{MCU}T_{PWM})^{-1}$. As such, an effective bit-depth can be expressed as

$$B = \log_2 \left\{ f_{MCU} T_{PWM} (D_{max} - D_{min}) \right\}. \tag{8}$$

In the present case, $f_{MCU} = 40$ MIPS, the $T_{PWM} \approx 25$ μs, and the duty cycle is specified on the interval $D \in [20\%, 80\%]$, giving an effective bit depth of 9.2 bits (0.1%). Under these conditions, the data acquisition rate for all four sensors channels is 20 kHz, enabling relatively fast measurements to be acquired. The maximum data acquisition rate for a single channels is bounded above by the Nyquist–Shannon criterion, such that within a single channel sampling period in the TDM scheme, a signal with a maximum frequency of approximately 20 kHz can be resolved when the carrier frequency of the PWM waveform has a frequency of approximately 40 kHz (Figure 10). However, in a perhaps more likely scenario, if the data within a single window of the TDM scheme are considered together using a statistical mean estimator, then the data acquisition rate is decreased to approximately 250 Hz, as the cycle time for the TDM is approximately 4.0 ms (Figure 10).

In addition to a relatively high acquisition rate over all the sensor input channels, the transfer function specifying the correspondence between the input voltage $X_n(t)$ and its output duty cycle measurement $D_n(t)$ is important to characterize so as to produce accurate measurements. To perform these measurements, DC



(a) (b)

Figure 10. Simulation of the PWM current driving the LED used to transmit signals from the FREND system to the data acquisition system and the PWM signal received by the microcontroller (a). A magnified plot showing the PWM waveform is shown in (b). Note that an artificial offset was added to each of the traces to improve their visibility and comparison.

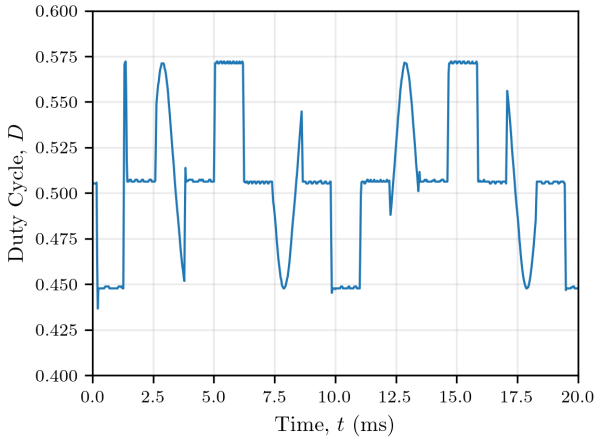


Figure 11. Example of a signal captured from the demodulated PWM waveform acquired by the FREND receiver.

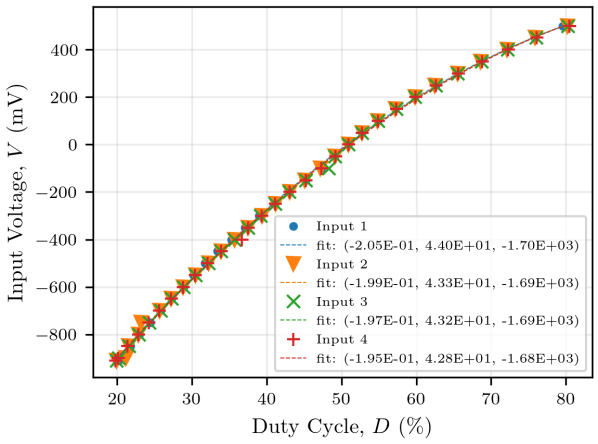


Figure 12. Channel input-to-receiver transfer function enabling the calculation of input signal voltage with duty cycle recorded by the FREND receiver.

input voltages were sequentially applied to each of the input channels, and the duty cycle of the PWM waveform at the receiver was measured using an oscilloscope. The transfer function for each input channel was characterized over the range [−910 mV, 500 mV], or approximately 20% to 80% duty cycle, in 50 mV increments (Figure 12). These data were then fit using a second-order binomial function of the form $a_n D_n^2 + b_n D_n + c_n$, and the tuple (a_n, b_n, c_n) was used to denote the best-fit parameters. The best-fit tuples for each channel were similar, though small differences were expected and exist in the physical implementation due to variation in the characteristics of the JFET circuitry and associated component tolerances unique to each input channel. The transfer function describing each channel was well approximated using a second-order binomial. Therefore, to reconstruct the input signal from the PWM waveform transmitted over the optical fiber and incident on the FREND receiver, the $D \rightarrow V$ mapping can be directly applied to the duty cycle measurements on each channel n.

3.3 THERMISTOR IMPLEMENTATION

To demonstrate the initial functionality of the FREND system, thermistors were selected for the simplicity of use and minimal requirement of accessory components. Figure 13(b) shows an implementation of a thermistor circuit that generates a voltage V_n proportional to the change in resistance of thermistor R_T as

$$V_n = \left(\frac{R_T}{R_b + R_T}\right) V_{DD}. \tag{9}$$

When connected to the input channels of the analog multiplexer (Figure 3), the supply voltage $V_{DD} = 3.0$ V, ground, and V_n connections are connected to the front end circuitry through the connectorized inputs. To calculate the resistance R_T from V_n, Eq. (9) can be rearranged as

$$R_T = R_B \left(\frac{V_n}{V_{DD} - V_n}\right). \tag{10}$$

In the present case, $R_b = 49.9$ kΩ (1% value) and the thermistor $R_T = 10$ kΩ at 25 °C and 1 kΩ at 100 °C (NTCG163JF103FT1; TDK Corp., Chuo City, Tokyo, Japan), giving a $\beta = 3.42 \times 10^3$ °C. According to its

β-parameter equation, which relates thermistor resistance to temperature,

$$T = \frac{\beta}{\ln(R_T/r_\infty)}, \tag{11}$$

where

$$r_\infty = R_0 \exp\left\{-\frac{\beta}{T_0}\right\}. \tag{12}$$

Under this parameterization, along with the $D \rightarrow V$ transfer functions (Figure 12), the temperature can be calculated from the input voltage on the n^{th} input channel as

$$T_n = \beta\left[\ln\left(\frac{1}{r_\infty}\left[\frac{R_B\,(a_n D_n^2 + b_n D_n + c_n)}{V_{DD} - a_n D_n^2 - b_n D_n - c_n}\right]\right)\right]^{-1}. \tag{13}$$

To demonstrate temperature measurements using thermistors with the FREND system and the use of the microcontroller input capture scheme for data acquisition (Eq. 7), three thermistor circuits were assembled (Figure 13(b)). Each of these was affixed to three distinct points on a hot plate: one in the center of the hot plate (sensor 3), one on the corner (sensor 4), and one at a radial location in between (sensor 2) (Figure 13(a)). The last input channel (sensor 1) was grounded using a pin header, and no sensor was connected so that its input voltage would be constant throughout the experiment and it could be used to mark the beginning of a new cycle in the TDM scheme. Because it was used as a marker, it was excluded from Figure 13. Data were recorded in bursts of 100,000 samples at a rate of 0.1 Hz using the dsPIC33F microcontroller's input capture functionality, and reconstructed using Equation 7, then logging the median value of from each channel during each sampling interval within the burst (Figure 13(c)). Data were isolated by identifying the transitions between channels and aligned using the grounded sensor 1 input.

The thermistor data acquired from the FREND system were consistent with the expected results: namely, that the radial temperatures of the hotplate decrease as the thermistor location from the center of the hotplate increases. The temperature indicated by the sensor 2 thermistor was the largest and peaked at approximately 65 °C between 7 and 8 min during the test before decreasing after the hotplate was turned off. The thermistor on sensor 3 reached 60 °C, which is within 5 °C of sensor 2, indicating that the center of the hotplate is relatively uniformly heated. Furthermore, the thermistor on sensor 4 indicated 10–20 °C lower than the other two sensor channels, which indicates that the extremities of the hot plate surface are significantly cooler than the center of the hot plate. Additionally, the sensor 2 thermistor had a greater maximum temperature than the sensor 3 thermistor, which was located in the center of the hotplate. As shown in the thermal images (Figure 13(a)), that the peak temperature of the sensor 2 thermistor is greater than the peak temperature of the sensor 3 thermistor is consistent with the temperature distribution on the hot plate, which peaks around the outside of its center, closer to the position of the sensor 2 thermistor. These data are also consistent with the thermal imaging data, which suggests the the thermistors peaked when the hotplate indicated it was heated to 100 °C at approximately 65 °C (sensor 2), 60 °C (sensor 3), and 45 °C (sensor 4). While this preliminary testing demonstrated the functionality of the FREND system, additional testing will be performed over a range of temperatures and compared to calibrated thermocouples to characterize specific sensor responses of sensors used with the FREND system. A similar testing regime will be adopted for other sensor types in future iterations of the FREND system.

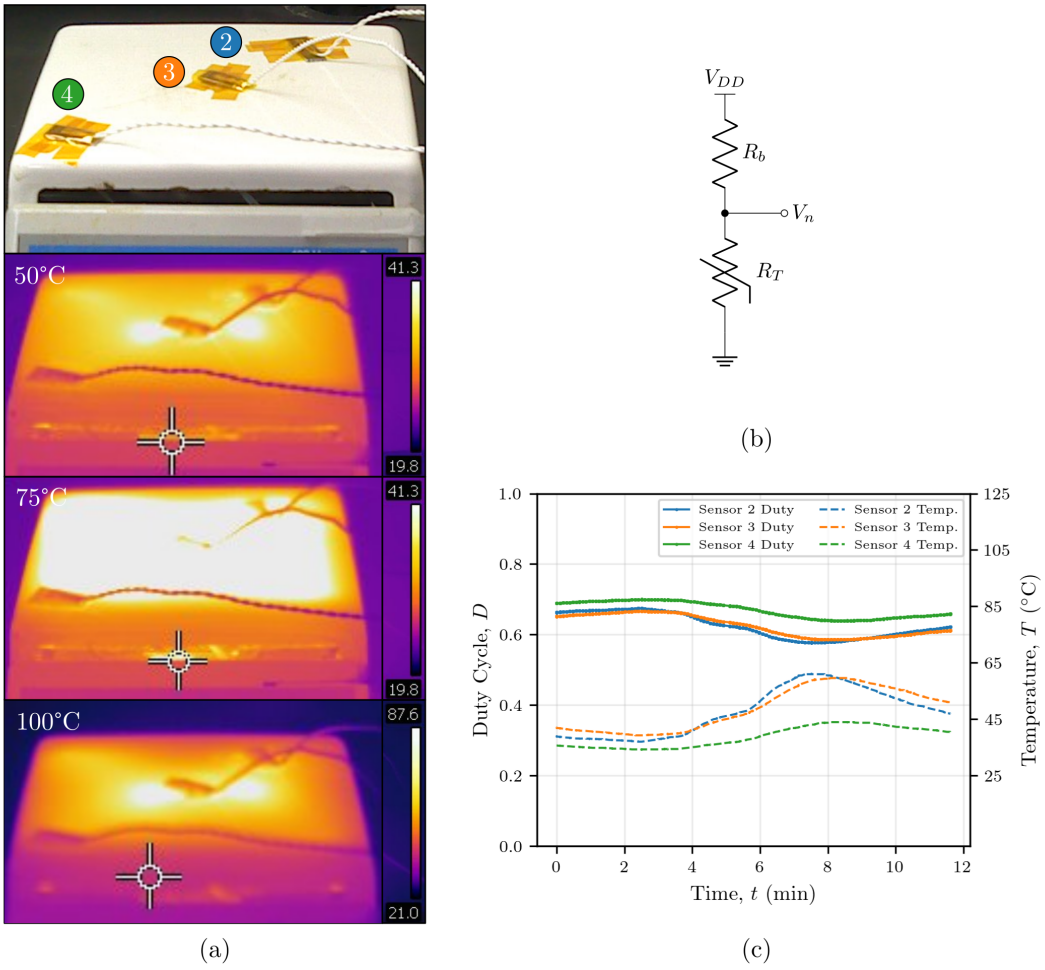


Figure 13. Demonstration data acquisition from thermistors using the FREND system. Three thermistors and associated front-end circuitry (a) were placed on a hotplate (b) and the temperature was varied while data was acquired with the FREND system.

4. DISCUSSION

4.1 SENSOR COMPATIBILITY

The present embodiment of the FREND system transmits signals from four sensor inputs with voltage ranges of approximately −1.0 to 0.5 V over an optical fiber and digitized using an optical PWM scheme. This system is, at present, limited to voltage inputs, rather than current inputs, on each of its four input channels (Figure 3). The prototype device was demonstrated using a resistive ladder incorporating a thermistor as the sensing element because a voltage proportional to the sensor's temperature can be easily calculated (Figure 13(b)). However, other types of voltage signals are good candidates for use with the system. For example, oscillator-based sensors or tank circuits with resonant frequencies on the order of 5–10 kHz may be good candidates for use with FREND, as signals from these sensors could be captured and analyzed on a per-window basis within the TDM scheme, provided that their output is within the appropriate voltage range. However, additional processing would need to take place on the host computer following digitization to analyze the shifts in frequency content. Thermocouples could also be used with the FREND system because they produce voltages on the order of 0.0 (0 °C) to 50.0 mV (1200 °C) through the Seebeck effect. However, challenges such as cold junction compensation and conductor material transitions would complicate their use. Current sensors could also be used with the FREND system but would require additional analog signal processing to convert the sensor current into a readable voltage.

Although the FREND system is capable of interfacing with a wide variety of relatively simple, single-ended sensors, the system's present embodiment cannot interface with sensors that operate using more complex mechanisms. For example, resistance temperature detectors (RTDs) designed to operate using a three- or four-wire scheme and would require additional circuitry to convert the differential measurement of the voltage across and current through the RTD from a differential measurement to a single-ended measurement. Other differential sensors face similar complications by requiring the conversion to a single-ended voltage value, including potentiostatic/galvanostatic measurements, Wheatstone bridge and other bridge-based strain sensors, and differential pressure or flow sensors. However, though differential measurements increase the complexity of interfacing with the FREND system, additional radiation-resistant modular analog front end circuitry to more easily interface with differential sensors is the focus of ongoing research efforts.

4.2 HARSH ENVIRONMENT DESIGN CONSIDERATIONS

The prototype FREND system described and demonstrated in this report is intended to serve as a radiation-tolerant proof-of-concept test unit that will inform the development of a second-generation rad-hard system capable of being deployed in harsh environments relevant to nuclear energy generation, namely at high temperatures and under irradiation. The FREND system is intended for use within, or just outside of, containment and should ideally be located in positions that do not exceed the temperature rating of the components on the PCBs. For the present prototype system, this limit was conservatively selected to be 100 °C. At higher temperatures, the maximum temperature rating of the components on the circuit board may be exceeded and generate unpredictable or errant behavior. Furthermore, the solder material used to affix the circuit components to the PCB may melt and may cause interrupted electrical connections beyond 150 °C without using high-temperature–rated solder. To ameliorate these concerns, it is recommended that the circuitry comprising the version one FREND system, and associated enclosures, be installed in relatively low-temperature regions in and around reactors. Radiation is also a central concern for sensors and instrumentation used in nuclear energy generation. These systems must survive the large γ

and neutron fluxes (10^{10}–10^{11} n/cm^2/s) generated during energy production. JFETs were selected as the basis for the circuitry developed in the present work because they have been demonstrated to survive > 100 Mrad (Si) γ-irradiation [15, 20]. JFETs are expected to have the highest probability of commercially available components to survive in these harsh environments. In addition to high-temperature and radiation considerations, the FREND enclosure must be water-tight when installed in and around reactor pools. Water leaking into an enclosure containing electronic circuitry could result in inadvertent shorts and other electrical damage, or long-term corrosion. To this end, the next embodiment of the FREND system will be enclosed in a water-tight housing to mitigate concerns of water damage. Penetrations through the enclosure walls for optical fibers, sensor leads, and power delivery will be minimized.

4.3 EXPECTED RADIATION EFFECTS

Under ionizing radiation, the discrete JFETs comprising the logic circuitry within FREND are expected to exhibit transconductance drift and variations in threshold voltages due to both TID and dose-rate effects. High ionizing dose rates lead to an increase of single-event effects (SEEs), which cause errors such as erroneous bit flips in digital circuits. MOSFETs are particularly susceptible to SEEs due to charge trapping in their gate insulators. JFETs are less sensitive to ionizing radiation, as their gates are non-insulated. However, JFETs may still be susceptible to ionizing radiation and SEEs from short-channel effects and surface charges on the insulating overlays. Additionally, the oscillator circuitry generating the clock signal relies on capacitors to determine its frequency. Capacitance has been shown to vary with radiation, mostly attributed to γ heating [15, 25]. The clock frequencies of FREND are expected to increase frequency when irradiated and will result in a loss of bit depth as the width of the PWM pulses (T_{PWM}) decreases (Eq. 8). Under neutron irradiation, silicon-based devices are expected to experience changes to the dopant profile as silicon neutron captures to phosphorus. The material lattice is also expected to change as a result of neutron knock-on reactions. These phenomena are expected to produce changes to the carrier recombination rate, reducing the minority carrier lifetime and causing changes to the gains of each individual JFET [4]. Matched JFET pairs will also have the potential to become unmatched. Ionizing radiation will be produced as a secondary effect to neutron capture and scattering, resulting in neutron-induced device failure through single-event burnout (SEB) [6, 7].

Though it is expected that the discrete circuit components (JFETs, resistors, capacitors, etc.) will fail long before the PCB itself fails, the circuit board and associated support material is expected to embrittle and potentially deform under irradiation. These material changes could result in shorts and broken traces forming between traces on the PCB, which will disrupt circuit operation. Another potential failure point will be the seals on the box enclosure, allowing admittance of water. This could result in immediate device failure or measurement corruption due to complete or partial shorts between normally separated conductors on the PCB. A tin-based, lead-free solder will γ heat less than leaded solder. Additionally, aluminum enclosure will remain cooler and activate less and for a shorter period of time than many alternatives. The optical components of the system and optical fiber are also expected to be damaged over time and potentially experience lens darkening of FREND's onboard transmitter LED and radiation-induced attenuation in the optical fiber, respectively. However, these concerns can be mostly ameliorated through careful material and component selection, as these failure modes are expected to occur long after device failure.

Future technology development efforts are focused on implementing the FREND system using wide bandgap (WBG) semiconductors, such as gallium nitride (GaN) or SiC, rather than silicon-based JFETs used in the present prototype system. These technologies will further harden the system against the effects

of radiation damage [21]. Of the WBG semiconductors, SiC is the most mature and has been studied under irradiation since the early 1990s [14]; presently, NASA Glenn (Cleveland, OH) maintains a SiC JFET process used for Venus exploration [17–19]. Other promising candidate WBG semiconductor technology, including GaN, is less mature, though WBG semiconductor use is part of planned research efforts for future generations of FREND.

5. FISCAL YEAR 2023 ACTIVITIES

In fiscal year 2023, irradiations are planned to test the prototype FREND system. The layout of the FREND prototype system will be revised to be more compact and include test points at strategic locations where characterization of the prototype's performance under irradiation can be monitored. An instrumented irradiation(s) will be performed and will target circuit failure under γ, neutron, and/or mixed γ-neutron sources, as available. The aim of these efforts is to characterize circuit behavior under irradiation and during component failure due to radiation damage. Should additional funding be made available, a subcontract with researchers at the University of Notre Dame (Notre Dame, IN) will be pursued to integrate thermo-electric generator (TEG) technologies into FREND toward the development of a self-contained and self-powered FREND system.

6. CONCLUSION

During fiscal year 2022, a prototype of the FREND system was designed, built, and bench-top (out of pile) tested. This system was designed using ionizing radiation–tolerant components, capable of reading four sensor input channels simultaneously, and transmitting the signals from all four inputs over a single optical fiber. To demonstrate the system's performance, the FREND system instrumented with three thermistor bridges was used to acquire data during thermal testing. Looking forward, irradiation tests to identify weak points and failure modes are planned for fiscal year 2023. A second-generation FREND system is also planned with the aim of including the ability to transmit data from an increased number of sensor types—namely, pressure sensors and thermocouples—to enable pressure, temperature, and flow measurements. Stretch goals for the 2023 fiscal year include the addition of power harvesting capabilities to the FREND system. The aim of these efforts is a self-powered analog multiplexer capable of transmitting signals from an array of sensors over a single optical fiber to reserve signal integrity in an EMI-rich environment.

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