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CRADA Final Report: CRADA Number NFE-18-07342 with Lux Semiconductors, LLC



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1. Abstract

Lux Semiconductors is a flexible microelectronics startup developing a new class of System-on-Foil electronics for rapidly emerging Internet-of-Things (IoT) markets. By leveraging its patent pending breakthrough in thin-film recrystallization, Lux is able to produce highly crystalline and flexible silicon substrates on a thin metal backing. This novel platform allows for high-speed silicon circuitry to be patterned directly into the substrate alongside low-cost printed electronics. The System-on-Foil approach has potential to enable the fabrication and integration of all core IoT functionality, including microprocessors, sensors, antennas, interconnects, and power supplies, required to enable highly durable, low profile, flexible electronics.

2. Statement of Objectives

The proposed project was aimed at producing crystalline semiconductor thin films atop flexible host substrates. The intended project outcome was:

1. To gain a deeper understanding of the thin film crystal growth mechanism of silicon
2. Develop an optimized crystal growth process for obtaining high mobility silicon films
3. Qualify the crystallized silicon films in electronic devices and construct a preliminary design for roll-to-roll process integration.

3. Benefits to the Funding DOE Office's Mission

The proposed project was aimed at producing crystalline silicon and germanium thin-films atop flexible host substrates. The project outcome was expected to be a deeper understanding of the thin film crystal growth mechanism of silicon and germanium, an optimized crystal growth process for obtaining high mobility silicon and germanium films, qualification of the crystallized silicon and germanium films in electronic devices, and a preliminary design for roll-to-roll process integration. If successful, the project would lead to the production of novel semiconductor films that could serve as the first ubiquitous flexible semiconductor platform for next generation electronic devices. The platform is suitable to host a range of electronic components and fully integrated system-on-chip designs including sensors, RF, displays, lighting, processors, memory, MEMS, and photovoltaics.

4. Technical Discussion of Work Performed by All Parties

4.1. Interlayer Design and Characterization

A successful study of thin-film recrystallization dynamics requires the engineering of appropriate buffer layers between the semiconductor film and the substrate. Interlayers were tested, evaluated, and optimized to block metallic species from diffusing into the semiconductor and potentially inhibiting epitaxial growth and degrading the semiconductor layer's electronic properties; minimize lattice mismatch and support thermodynamic stability against reactions so as to produce an abrupt, epitaxial buffer/semiconductor interface; and provide adhesive functions at the metal/buffer interface to prevent delamination of layers from the underlying foil during cool

down, to counteract differences in thermal expansion coefficients ($4.8 \times 10^{-6}/\text{K}$ for Mo to $2.6 \times 10^{-6}/\text{K}$ for Si). After extensive surveying of academic literature and consultation with subject matter experts, a number of buffer layer candidates were identified to perform these functions. During Rapid Access and General User awards at the Center for Nanophase Materials Sciences (CNMS), baseline deposition parameters for buffer layers and semiconductors were established. Before being tested in Lux's prototype heating chamber, several film stack designs were screened via an anneal in a rapid thermal annealing system. This screening method subjected candidate film stacks to heating and cooling rates of approximately 80°C/s , far in excess of the rates expected in Lux's heating chamber.

4.2. Improvements to Recrystallization Process

As discovered during previous work, when silicon films are melted in Lux's heating prototype system, if temperature gradients across the melt pool are too steep, radial contraction of the molten silicon can occur. This phenomenon is intended to be resolved in the long term by using advanced control systems in Lux's pilot-scale heating system to limit the overall size of the melt pool. However, for this work, the size of the melt pool was controlled by patterning the silicon layer into square "islands" of silicon measuring 1, 3 or 5 mm per side. To fabricate the "island" samples, and in consultation with CNMS staff, Lux developed an etch based process to pattern the silicon layer. Figure 1 depicts the mask used to pattern the silicon along with micrographs demonstrating the resulting islands.



Figure 1 - CAD rendering of pattern mask and micrographs of 1 mm silicon islands, at $20\ \mu\text{m}$ resolution.

4.3. Development of Planarization Processes

In order to use conventional silicon-wafer based lithography tools and processes, Lux's substrates have to match the planarity and surface roughness of a silicon wafer. This is a well-known challenge for metal foil-based substrates. Given that a silicon wafer surface roughness is on the order of 1 nm Ra (average roughness), and the best commercially available Mo foil (Lux's underlying metal foil) is on the order of 300 nm, considerable improvements were required before patterning of high performance circuits is possible. Leveraging CNMS facilities, Lux expanded on previous surface treatment processes to develop a more cost effective and scalable solution. Initially, Lux engaged with a commercial partner to develop a chemical-mechanical polishing (CMP) procedure for its Mo foils. This work successfully reduced the average surface roughness by two orders of magnitude, to near 10 nm Ra. Atomic force microscopy revealed, however, that the surface still retained two forms of defects, trenches (~ 10 nm deep lines) and divots (from granular inclusions, 50-100 nm deep). Rather than implement additional and expensive CMP processes, Lux instead developed a cost effective and scalable process to spin-coat an ultra-thin planarization layer of spin-on-glass, applied directly to the polished Mo foils. The spin-on-glass

process was effective in reducing the trenches and divots, for a net resulting surface roughness of sub 1 nm Ra, on par with a silicon wafer. The tabulated results, as shown in Figure 2, show the significant improvements in surface condition as a result of this critical milestone work. As an added benefit, the spin on glass serves doubly as a cost-effective dielectric coating to the substrate, with no appreciable impact to flexibility.

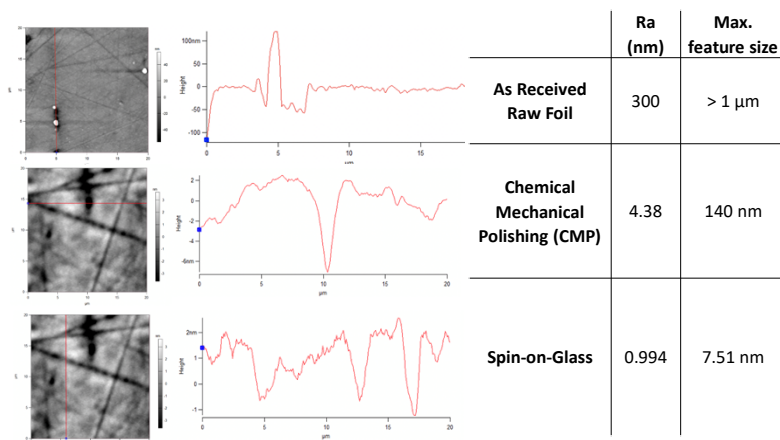


Figure 2 - Atomic force microscope measurements of Lux's Mo foil substrate, as received and post treatments.

Additionally, Lux sought to reduce the thickness of its Mo foil from 250 μm to 50 μm . This reduces material cost, reduces polishing requirements, increases flexibility, and dramatically increases the efficiency of its heating recrystallization process. This will be key for product development as device flexibility and weight are considered valuable to peel-and-stick structural integrity sensors, and even more so in alternative identified applications in space and medical wearables. To accomplish foil thinning, Lux worked with its metal foil supplier to create a custom spec of Mo foil that undergoes additional rolling procedures to obtain a desired thickness of 50 μm . This development effort will provide the company with sole access to the new material specification.

4.4. Lithographic Process Development

Following the improvements to surface roughness, Lux was then able to work with its academic partners to demonstrate conventional Complementary Metal Oxide Semiconductor (CMOS) processes, for integrated circuit fabrication, adapted to Lux's silicon substrates. As photolithography process development is crucial for the fabrication of high-performance integrated circuits on Lux's substrates, Lux partnered with Prof. Ivan Puchades at the Rochester Institute of Technology (RIT) to perform this work in parallel with Innovation Crossroads sponsored research. This work demonstrated that Lux's substrates are compatible with a number of CMOS-standard processes with little adaptation needed. Figure 3 depicts some early results from the work, most notably achieving 4 μm resolution using a contact photolithography tool. Ongoing work includes silicon-based circuit components, including metal and silicon resistors, interdigitated metal capacitors, MOS capacitors, metal inductors, Schottky diodes, PN and PIN junction diodes, and PMOS and NMOS transistors. These components form the basic building blocks of electronic circuits. Lux intends to continue to work to target elements of its proposed

wireless temperature and strain sensor that can be most readily patterned directly into the film by photolithography.

Figure 3 - Micrograph of various features in Lux silicon.

During a previous NSF Phase I award, a number of samples were measured for electron mobility using the Van Der Pauw method in a Hall Effect tool with 4 point probe. At the time of experiment, Lux had not yet begun doping effects characterization work and was still experimenting with intrinsic/undoped silicon. As a result, the resistivity of the undoped silicon often tested the limits of the measurement instruments being used. However, of the samples that were successfully measured, a median average of 117 cm²/Vs was recorded, see inset plot. In order to more accurately and reliably measure mobility, Lux has begun working with research partners at the Rochester Institute of Technology (RIT) to pattern micron scale Van Der Pauw devices directly into its silicon using lithographic processes. A lithography mask that includes these features has already been fabricated and the 2nd inset image shows the section of mask dedicated to Van Der Pauw measurements. As the silicon used in these experiments will be intentionally doped via ion implantation, it is expected that the difficulties encountered during earlier mobility measurements will be easily overcome.

Before Innovation Crossroads, Lux Semiconductors performed system upgrades and optimization work for its patent pending thin-film silicon recrystallization process in its small-scale prototype chamber. This custom-built chamber was sufficient for feasibility studies and exploration of optimal process parameters and thin-film layer stacks to support high quality recrystallization. The prototype chamber, however, is no longer capable of meeting the emerging technical and commercially-driven needs of the company. Recent advances in market discovery and commercial traction are now creating demand for larger material sizes, higher crystal quality, and higher processing throughput. The current prototype chamber is limited to a 1in2 recrystallization zone and only set up for small batch processing. Increasing the size, quality, and throughput will be essential for delivering sample material to potential customers and supporting the critical next phase of development, Complementary Metal Oxide Semiconductor (CMOS) lithographic patterning of electronic devices.

significantly increases sample quality, size, and throughput. This system will increase the silicon melt and recrystallization zone to a targeted 16 square inches, representing a 16X increase in sample size over the existing prototype chamber. The new chamber is also being designed as a modular unit capable of mating in-line to deposition tools, or as part of a cluster tool, so that thin-film depositions can be performed without breaking vacuum and immediately processed. Furthermore, unlike the prototype chamber, which was pieced together from a mix of retrofit components, the pilot scale recrystallization chamber will be a custom design to maximize the effectiveness of Lux's recrystallization process. Improvements in vacuum level, temperature control, stage level, and linear motion will facilitate much more sophisticated, lower tolerance controls over the critical parameters that dictate the final recrystallized film quality. Lastly, as the chamber and induction coil are scaled in width, the undesirable oval profile of the silicon melt transforms into an ideal line source. Scaling also increases the recrystallized area ratio of each substrate while improving the overall heating efficiency.

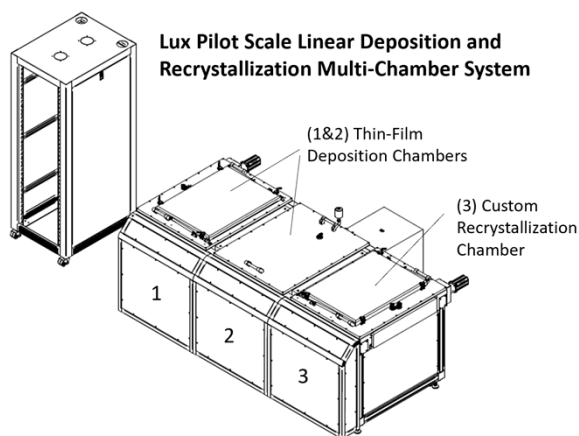


Figure 4 - Through an NSF SBIR Phase II, Lux intends to fund the design of a custom recrystallization chamber (Chamber 3). This modular chamber can then be added to with in-line deposition chambers.

4.7. CRADA Extension

Lux had requested an extension of its CRADA with the DOE to complete two critical objectives: Semiconductor Crystallization Process Optimization and Electronic Device Fabrication and Characterization. Since the extension, Lux has re-initiated sample production using processes developed prior to work from home orders, which include metal foil polishing and cleaning, semiconductor and buffer layer material deposition, and lithographic patterning (Figure 5), and has now completed semiconductor crystallization process optimization at the prototype scale. These efforts have motivated a scale up to a larger pilot scale production system (Figure 6). The new pilot scale system is being funded by an NSF SBIR Phase II and will be capable of handling wafers up to 200mm (8") in diameter, a 5X increase over the current prototype system.

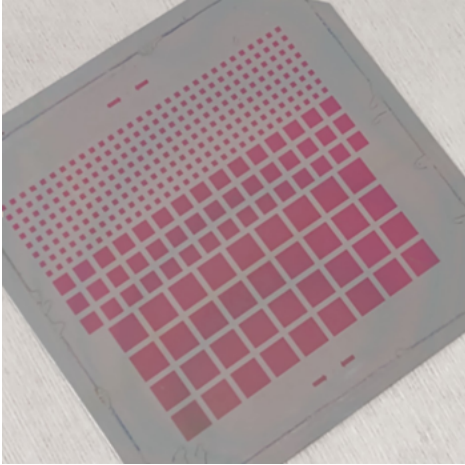


Figure 5 - Patterned silicon islands on metal foil substrate.

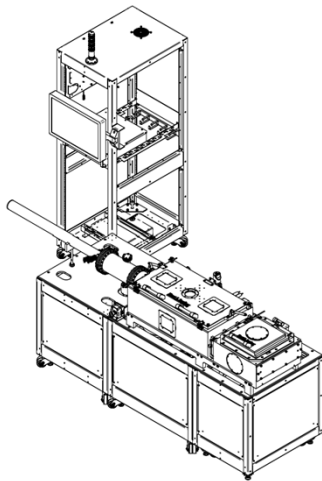


Figure 6 - Render of final approved system design for Lux's pilot scale recrystallization tool.

The second objective, electronic device fabrication, has also progressed towards completion. The goal was to develop lab-scale semiconductor fabrication processes that were compatible with Lux's silicon substrates. This included photolithography, etching, ion implantation, and thin film deposition. A number of critical devices have also been fabricated and tested, including resistors, sheet resistance structures, Schottky diodes, interdigitated metal capacitors, metal antennas, metal inductors, metal resistors, MOS capacitors, and silicon resistors. A couple example resistors are shown in Figures 7 and 8 below.

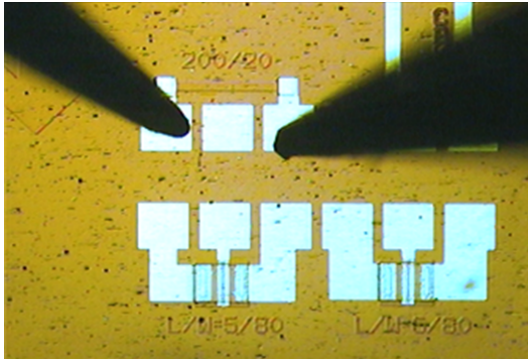


Figure 7 - P+ Resistor on Metal Foil.

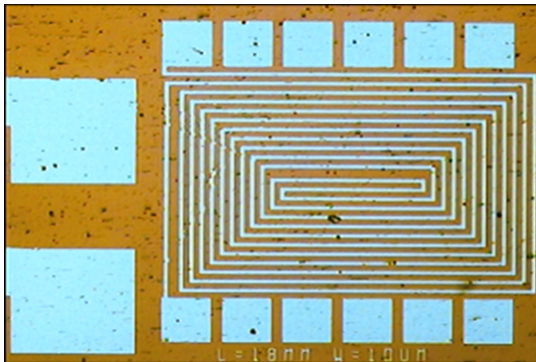


Figure 8 - Al Resistor on Metal Foil.

5. Subject Inventions (As defined in the CRADA)

None.

6. Commercialization Possibilities

Lux's strategy is to initially target niche applications for aerospace and defense where flexible form factors, durability, and low-SWaP are highly valued. With growing capability and economy of scale, the System-on-Foil platform will be easily adapted to address a wide range of subsequent applications beyond aerospace, including high volume and price-sensitive commercial markets. Early commercial beachhead customers are expected to include:

- Aircraft and Vehicle OEMs - Conformal solutions integrated into equipment. Sensors for digital manufacturing.
- Supply Chain Management - Wireless/RFID sensors to track and monitor the condition of shipments during transport.
- Utility Grid Operators - Retrofit of existing electronics systems with peel-and-stick equivalents.

In support of its customer discovery efforts in aerospace and defense, Lux has recently taken part in the T3 Transition Accelerator sponsored by AFRL, and the Techstars Starburst Space Accelerator. These 3-month-long concentrated programs have allowed Lux to focus on understanding the pain points associated with conventional electronics as present in air and space craft. The System-on-Foil approach has received validation for its expected improvements to device size, weight, and reliability, from a wide group of government representatives and contractors. Additionally, the military's desire for trusted and secure domestic electronics is seen as a salient advantage as well. Lux is also a member of the Nextflex consortium and has received support for its System-on-Foil approach from Boeing, Lockheed Martin, Raytheon, General Dynamics, and BAE Systems.

7. Conclusions

The unique opportunity to participate in the prestigious Innovation Crossroads program held at Oak Ridge National Laboratory has been one of the most rewarding educational and professional development experiences of my nascent career. During the program, I was fortunate enough to work alongside some of the leading research scientists in my field, including my principal investigator, Dr. Pooran Joshi. The many discussions I was privileged to have with Dr. Joshi were not only technically informative, they were also instructive in how I designed my research plans and experiments. And these proposed plans and experiments were effectively translated into high quality research conducted in ORNL's world class facilities, like the CNMS. There, with assistance from CNMS staff, I was able to achieve a number of technical milestones outlined at the onset of the program. However, as entrepreneurial fellows, it is not sufficient to merely advance our research, we must be sure to advance the business along with it. This is where the Innovation Crossroads program was a huge benefit to me professionally. Innovation Crossroads staff constantly supported the development of new grant proposals and investor pitches, both of which led to significant improvements in my written and public speaking skills. The program also exposed me to key business development principles, including customer discovery, business model development, and go-to-market strategy. Now equipped with the necessary technical and business knowledge, I look forward to making the transition from a technical founder to a startup CEO. Thank you, Innovation Crossroads!