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# Survey and Benchmark of Benefits of High Voltage SiC Applications in Medium Voltage Power Distribution Grids


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Electrification and Energy Infrastructures Division

# SURVEY AND BENCHMARK OF BENEFITS OF HIGH VOLTAGE SIC APPLICATIONS IN MEDIUM VOLTAGE POWER DISTRIBUTION GRIDS

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## EXECUTIVE SUMMARY

The main objective of this survey and benchmark study is to identify and document potential high-impact applications in today's and future medium voltage (MV) distribution grids that will significantly benefit from high voltage (HV) (i.e. > 3.3 kV) SiC-based power electronics equipment. In particular, it is desirable to identify applications that can utilize the high switching speed and high control bandwidth enabled by SiC-based equipment. Specifically, the benefits of using SiC are quantified through the benchmark analysis and design using simulation for the selected high-impact applications. In addition, to provide grid support services, it is necessary to consider grid requirements in the grid-connected converter's design. Therefore, the impact of grid requirements on the HV SiC-based grid-connected converter is evaluated.

To achieve the above objectives, five main tasks were carried out:

1) Surveyed and summarized the latest HV (in the range of 3.3 kV to 25 kV) SiC devices available from commercial vendors. The data were used in the analysis and benchmark study in comparison with Si devices.
2) Surveyed and summarized existing and emerging power electronics-based equipment for MV distribution grids, including current and future grids. The equipment included: a) "traditional" custom power equipment, such as power flow controller (e.g. solid-state transfer switch, solid-state breakers and fault current limiters), power conditioner, and compensator (e.g. distribution STATCOM, dynamic voltage restorer, unified power quality conditioner) and active power filter; b) emerging equipment, including renewable energy interface converters, energy storage converters, and microgrid interface converters (for both DC, AC, and AC asynchronous microgrids); and c) some more recent development and variations of the traditional equipment to address the size, cost, controllability, and reliability issues associated existing power electronics equipment. This category of equipment included solid-state transformers, controlled network transformers, and continuously variable series reactors. The survey and analysis led to the selection of microgrids for further benchmark study as a result of their inclusion of many distributed energy resources (DERs) and their importance for renewable energy integration and critical infrastructures including manufacturing facilities.
3) Analyzed the benefits of using HV SiC in the DER interface converters in conventional MV (13.8 kV) AC microgrids, including a) design comparison of Si- and SiC-based converter solutions in a MV microgrid. A utility-scale (1 MW, 13 kV) PV inverter was selected as the example; b) system benefits analysis including enhanced power quality, enhanced stability, and low voltage ride through (LVRT). The power quality was analyzed based on that the interface converters can double up as active harmonic filters. The stability issue was studied by evaluating the oscillation and stability of microgrids with paralleled converters as a function of converter control bandwidth. The LVRT was studied by simulating the LVRT performance of microgrids with DER interface converters.
4) Analyzed the benefits of using SiC in the power conditioning system (PCS) converters in MV (13.8 kV) asynchronous AC microgrids, including a) design comparison of Si- and SiC-based microgrid PCS in a MV microgrid. Both the three-level neutral-point-clamped (NPC) and modular multi-level converter (MMC) transformer-less SiC converters were designed and compared with Si three-level NPC; b) system benefits analysis including better LVRT and mode transition performance, stability enhancement, power quality enhancement, and black start. The approach for evaluating system-level benefits was based on simulation and similar to that used for conventional AC microgrids.
5) Evaluated the impact of grid requirements on the MV SiC-based grid-connected converter design. A baseline design is first conducted without considering grid requirements. Then, the grid requirements, including LVRT, high voltage ride through (HVRT), grid faults, frequency ride through, grid voltage angle change, and lightning transient, are considered one by one in the converter design. The converter component size and weight are compared between the baseline design and the design considering grid requirements to evaluate the impact.

The main findings of this report can be summarized as follows:

1) All power electronics equipment for MV distribution grids can benefit from HV SiC devices through direct substitution of Si devices with SiC devices, leading to lower loss, high efficiency, and reduced cooling need. Most power electronics equipment can also have simplified topology and smaller passive filters as a result of the higher voltage and faster switching capabilities of HV SiC devices. Fast switching of HV SiC devices will enable high control bandwidth, leading to enhanced functionalities and capabilities of some power electronics equipment, e.g., integrated filtering and system stabilizing functions for DER interface converters.
2) Microgrids, as an emerging application and an interface between the DERs and utility grid, involve many renewable energy sources, distributed generation (e.g. combined heat and power or CHP), loads (e.g. critical loads like manufacturing facilities), and energy storage systems. Microgrids can include multiple power electronic converters, e.g. DC/DC and DC/AC for battery and PV, AC/DC/AC or AC/AC for wind turbine generators, and AC/DC/AC for PCS in an asynchronous microgrid. HV SiC devices can help improve these converters and enhance their system capabilities and functionalities. Therefore, for better grid integration of renewable sources and high research impacts for future distribution grids, the microgrid was selected as the base benchmark case and the "killer application" in this report.
3) HV SiC devices can benefit DER converters in a conventional AC microgrid at both the converter and system levels. At the converter level, the SiC-based DER converter will have a significant weight and size advantage compared with the Si counterpart, e.g. an 82.9% weight reduction and 73.2% size reduction can be achieved for a 1 MW, 13.8 kV PV interface converter using HV SiC devices. The SiC-based DER converters can work with a higher switching frequency (e.g. 3 times that of Si-based converters), and therefore have a higher control bandwidth. At the system level, the high control bandwidth results in power quality improvement (e.g., saving the need for a dedicated active power filter which can be 14% of the total converter rating in the example study), system stability enhancement (maintaining stability even in weak grid conditions) and better LVRT dynamic performance.
4) HV SiC devices can also benefit PCS converters in asynchronous microgrids both at the converter level and system level. At the converter level, the SiC-based PCS has significant benefits in weight and size (e.g., 83% weight reduction and 81% size reduction with SiC-based three-level 13.8 kV, 1 MW NPC, 60% weight reduction and 67% size reduction with SiC-based MMC, compared with a Si-based three-level NPC, even without considering low-frequency transformers), and even in efficiency if the switching frequency is limited to 10 kHz (e.g., 46.6% loss reduction with SiC-based three-level NPC and 31.8% reduction with SiC-based MMC). The HV SiC-based PCS converters can work with a higher switching frequency (around 10 to 20 times higher than that of Si-based PCS converters), and therefore have a higher control bandwidth. At the system level, the high control bandwidth of the PCS converters can result in enhanced performance of the microgrids on power quality, system stability, LVRT, transition between islanded mode and grid-connected mode, and black start capability. On power quality, SiC-based PCS can have integrated harmonic filtering capability and therefore eliminate the need for additional harmonic filters (e.g., saving an APF that can be 14% of the PCS converter or load rating). On stability, the SiC PCS can isolate the impact of the grid impedance and enhance the system stability in grid-connected mode and operates as a stabilizer to enhance the stability in islanded mode. On LVRT, mode transition between grid-connected and islanded modes, and black start, with the PCS, the load in the microgrid can be supplied normally even during the LVRT and mode transition periods, and the black start can be easier.
5) Grid requirements have impact on the grid-connected converter design. The grid voltage disturbances, such as LVRT, HVRT, voltage angle change, temporary overvoltage, and transient overvoltage can lead to inrush current and DC-link overvoltage. A PWM mask method can be adopted to limit the inrush current induced by the grid voltage sudden change by temporarily masking the PWMs so that the inrush current flow through the MOSFET body diode and is reduced by the DC-link voltage. However, when the grid voltage amplitude is higher than the DC-link voltage, the PWM mask method can only reduce the inrush current rising rate but cannot limit it. For temporary overvoltage higher than 1.2 p.u., which

can be induced by grid faults, the converter is designed to temporarily stop operation, and restart within 3 seconds when the grid voltage recovers to below 1.2 p.u. A dynamic braking circuit is introduced to suppress the DC-link overvoltage and ensure a quick restart. Although arresters are installed to protect the converter from lightning surges, the voltage clamped by the arrester is still much higher than the converter's normal operation voltage, and the high voltage leads to a large inrush current, DC-link voltage variation, as well as insulation consideration. An online simulation consisting of the converter switching mode, the arrester mode, the coupling and decoupling network, as well as the combined wave generator is utilized to verify the lightning impact on the converter operation. A larger filter inductance helps to reduce the inrush current, but the converter size and cost will also be increased. A larger grounding impedance also helps to reduce the inrush current, but the converter components have a higher transient potential during the lightning surge, which results in a higher insulation requirement. Based on the converter design comparison, after considering the grid requirements, the converter size and weight increased by 26% and 90%, respectively for the benchmark case.

# 1. INTRODUCTION

## 1.1 BACKGROUND

Enabled by the high power handling capability, power electronics-based equipment has been proven to be much more flexible and faster than their electromechanical or electromagnetic counterparts for electric energy transfer and control. Since the advent of power electronics in the 1950s, power electronics have progressed steadily in all aspects, including semiconductor devices, passives, circuits, control, and system integration, leading to converter systems with better performance, higher efficiency, higher power density, higher reliability, and lower cost. Because of these progress, the power electronics applications in power systems have become more and more widespread [1] - [3].

Among these applications, microgrids, with their distributed energy resources (DERs) and ability to operate both in grid-connected and islanded modes have attracted tremendous research and development interests for higher reliability and resilience of the power grid. With natural disasters such as Hurricane Sandy causing millions of customers to be without electricity for weeks and billions of dollars of economic losses [4], microgrids would have made appreciable differences. In fact, as an aftermath reaction, DOE and The State of New Jersey partnered to develop a 50 MW NJ Transit microgrid that will keep the NJ Transit up and running in future emergencies [5].

Following this trend, the microgrids interconnected to the medium voltage (MV) distribution networks have been studied in detail recently for better integration of MW-scale bulky renewable power resources. The research efforts have been focused on power management [10] [11], system stability [12], control structure [13], and protection schemes [14]. Moreover, the asynchronous microgrid through a power conditioning system (PCS) has been proposed and promoted recently [15]. Compared with the conventional AC synchronous microgrid, an asynchronous microgrid has decoupled dynamics with the distribution grid. As a result, it can result in numerous system-level benefits: a) easier integration of renewable energy sources (RES) into microgrids without the need to consider RES and distribution grid interactions; b) better low-voltage/frequency ride-through capability; c) easier transition between grid-connected and islanded modes and elimination of the need for resynchronization control; d) isolation of unbalance and faults, for easier microgrid protection coordination and control. Furthermore, the PCS converters can provide independent var support to micro- and macro-grids, and even allow integration of energy storage and other distributed energy resources on the DC link [16].

In both MV synchronous and asynchronous microgrids, with the state-of-the-art silicon (Si) device-based converters, a bulky and lossy step-up transformer is generally required to match the voltage rating. Otherwise, a series connection of Si devices or multilevel converters becomes inevitable, leading to complexity and reliability issues [17]. Moreover, the low switching frequency of Si devices in MV applications (typically ≤ 3 kHz) greatly limits the control bandwidth, which may lead to power quality and stability issues [18]. High voltage (mainly ≥10 kV) silicon carbide (SiC) devices, with their higher breakdown voltage, lower loss, and faster switching capability, on the other hand, could enable significant improvement of microgrids and thus high penetration of the renewable energy resources in MV power distribution grids.

While in general, it is expected that using SiC will benefit, microgrids have different configurations and are required to accomplish various system functions and performance requirements, hence can expect to benefit differently in various application scenarios. Some may benefit more, and others may benefit less or not at all. In addition, SiC may pose multiple new challenges, for example, the fast switching SiC will bring new constraints to the gate drive, protection, and thermal management design.

It is therefore important to understand how SiC, especially HV SiC, can benefit MV distribution grids, in particular, microgrids in various applications. To answer this question and help to determine the future research needs in this area, the power electronics team of the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT) at the University of Tennessee, Knoxville (UTK) carried out a survey and benchmark analysis, sponsored by DOE/ORNL. This report summarizes the sponsored work.

## 1.2 OBJECTIVE AND MAIN TASKS

The objective of this survey and design analysis is to: 1) identify and document potential high-impact applications in today's and/or future distribution grids that will significantly benefit from HV SiC-based power electronics equipment; 2) in particular, identify applications that can utilize the high switching speed and high control bandwidth enabled by SiC-based equipment; 3) determine the benefits of SiC over Si in implementing the MV asynchronous microgrid power conditioning system (PCS) converters; 4) evaluate the impact of grid requirements on the HV SiC-based grid-connected converter design.

There are four main tasks in the survey and analysis study:

1) Survey and summarize all existing and emerging power electronics-based equipment for MV distribution grids, including today and future grids. The equipment can include the following categories: a) "Traditional" custom power equipment, including equipment for power flow control (e.g. solid-state transfer switch, solid-state breakers and fault current limiters), power conditioning (e.g. distribution STATCOM, dynamic voltage restorer, unified power quality conditioner) and active power filters. b) Emerging equipment, including renewable energy interface converters, energy storage/charging converters, and microgrid interface converters (for both DC, AC, and AC asynchronous). c) Some more recent variations to address the size, cost, controllability, reliability, and issues associated with the high renewable energy systems. The equipment includes solid-state transformers, controlled network transformers, and continuously variable series reactors.
2) Analyze the benefits of using SiC in the DER interface converter in MV conventional AC microgrid including a) Design comparison of Si- and SiC-based converter solutions in MV microgrid. A utility-scale MW medium voltage PV inverter is selected as an example; b) System benefits analysis including enhanced power quality, enhanced stability, and low voltage ride through (LVRT). The power quality is analyzed based on that the interface converters can double up as active harmonic filters. The stability issue is studied by evaluating the oscillation and stability of microgrids with paralleled converters as a function of converter control bandwidth. The LVRT is studied by simulating the LVRT performance of microgrids with interface converters.
3) Analyze the benefits of using SiC in the PCS converters in MV asynchronous AC microgrid including 1) Design comparison of Si- and SiC-based microgrid PCS in MV microgrid. Both the three-level NPC and MMC transformer-less SiC converters are designed and compared with Si three-level NPC; 2) System benefits analysis including better LVRT and mode transition performance, stability enhancement, power quality enhancement, and black start.
4) Evaluated the impact of grid requirements on the MV SiC-based grid-connected converter design. A baseline design is first conducted without considering grid requirements. Then, the grid requirements, including LVRT, high voltage ride through (HVRT), grid faults, frequency ride through, grid voltage angle change, and lightning transient, are considered one by one in the converter design. The converter component size and weight are compared between the baseline design and the design considering grid requirements to evaluate the impact.

The voltage level is assumed at 13.8 kV and the total microgrid power level is 1 MW. The benchmark design is carried out both at the converter level and the system level. The benefits of using HV SiC are determined both for the converters and for the system. The converter level benefits refer to the efficiency, power density, and specific power improvement, and the system level benefits refer to performance (power quality, stability, and reliability or ability to ride through abnormal conditions) as a function of control bandwidth. The system level benchmark considers all operation modes of a microgrid, including grid-connected mode, islanded mode, and LVRT mode, and their transitions. The system-level performance specs

(e.g. specified by relevant IEEE standards) need to be met, including power quality (frequency, voltage) and ride-through capability.

## 1.3 TECHNICAL APPROACHES

Based on the objective and the tasks, we have adopted the following technical approaches in this survey benchmark study:

### 1.3.1 Device Survey and Analysis

First, we collected information available to us on as many HV SiC devices as we can find, ranging from 3.3 kV to above 15 kV. The key characteristics are current ratings, die sizes, conduction and switching loss, and thermal characteristics. These serve as the bases for comparison analysis with Si and low voltage SiC devices in a MV power grid. Among the available devices, the ones with the best performance and most appropriate voltage ratings will be selected in the comparison study with Si. Since most HV SiC devices are still in developmental or early commercial stages, their current ratings are small and voltage ratings are also incomplete. A certain level of scaling is generally needed for comparison with Si devices.

### 1.3.2 Medium Voltage Power Equipment Survey and Analysis

Next, we conducted an extensive survey of the existing and emerging power electronics-based equipment for MV distribution grids, including today's and future grids. The survey first covers the existing or conventional custom power equipment, such as solid-state transfer switch, solid-state breakers and fault current limiters, etc., for power flow control/interruption, and DSTATCOM, dynamic voltage restorer, unified power quality conditioner, etc., for power conditioning and compensation. In addition, it also covers emerging equipment including renewable energy interface converters, energy storage/charging converters, and microgrids. Associated variant technologies to address the size, cost, controllability, and reliability, and issues associated with high renewables are also surveyed, e.g. solid-state transformer, controlled network transformer, magnetic transformer, etc. A representative application is expected to be selected in this section for the benefit evaluation of HV SiC devices.

### 1.3.3 Identify the Suitable Applications for HV SiC

For different MV applications and technologies, utilization of HV SiC devices is expected to be beneficial, some may benefit more, and others may benefit less. Therefore, in this step, we will identify the more suitable or "killer" applications that HV SiC devices can benefit most for the quantitative benefit assessment. These "killer" applications can be determined by the following approaches:

1) Substitution of Si devices with SiC devices – By direct replacement of the Si devices with SiC devices, improved efficiency and power density are expected for the power conversion system. Also, because of the increased voltage rating of SiC devices, simplified topology could be involved in this process, e.g., a two-level converter with step-down transformation for Si, while a multilevel converter for SiC. Furthermore, the multilevel modular converter topologies with SiC devices will be beneficial for better dynamics, less complexity, and improved power quality.
2) Determine the potential system-level benefits enabled by SiC devices– Substitution focuses on converter-level benefits. SiC technologies also offer the opportunity to achieve further benefits at the system level. For example, SiC devices allow a high switching frequency power conversion system as compared to today's high-power Si-based converters whose switching frequency is limited due to efficiency and thermal concerns. With the increased switching frequency and its resultant high control bandwidth, the SiC-based power electronic converters are expected to support more ancillary services for power grids and overcome issues in the

traditional AC grids.

3) Investigation of SiC benefits for various system configurations – Substitution and system-level benefits evaluation may not fully utilize the capability of HV SiC due to the various system configurations. For instance, the contributions of SiC devices for an asynchronous microgrid may differ significantly from those in a conventional synchronous microgrid. Therefore, for completeness, the benefit assessment should be conducted for both cases.

It is expected almost all MV power grids (microgrid as a representative) can benefit from 1) substitution with HV SiC devices, and many can benefit from 2) enabled new or enhanced system-level capability and functionality, but only microgrids with interfacing PCS can benefit from c) enabled new configurations. The criteria for "killer" application identification therefore should be for those satisfying all three categories. Consequently, microgrids will be selected as the high-impact application that we will focus on. The benchmark system based on a MV microgrid should potentially serve a manufacturing facility to satisfy DOE interest.

### 1.3.4 Benefit Assessment of HV SiC Based MV Power Distribution Grids

With the identified killer applications, a detailed comparison to quantitatively illustrate the benefits of the HV SiC will be carried out. The representative equipment/application selected above will be used to conduct the comparison study. In addition, the overall system will be considered, e.g. the isolation transformer, the converters for PVs, ESSs, and PCS, and also the load characteristics for a microgrid system. The different designs to be compared should include the best possible Si-based designs and the HV SiC-based designs with different converter topologies. The focus of the comparison will be on the converter-level benefits (e.g. efficiency, power density, footprint), and system-level benefits (e.g. power quality, stability, and LVRT).

It is expected that some relationships between the SiC device and converter parameters with the system performance can be established through the comparison study, such that some key design parameters and performance metrics can be defined for future HV SiC converters used in MV power grids, to realize their significant advantages over the Si-based systems. In addition, we also will try to identify some key research needs for achieving the high-performance SiC MV converters identified in the study, although it is not the main focus of this survey and report.

### 1.3.5 Evaluation of Grid Requirements on HV SiC-based Grid-connected Converter Design

First, the grid requirements will be identified based on grid codes and possible operating conditions. Then, a baseline design will be conducted without considering these grid requirements. The converter hardware design will be conducted, and the size and weight of the main components will be estimated. After that, the grid requirements will be considered in the converter design one by one. Control methods, if any, will be first adopted to reduce the hardware change to achieve a cost-effective design. Simulation and/or experimental tests will be conducted to verify the design approach. The size and weight of converter main components will also be estimated, and the size and weight comparisons between the baseline design and the design considering grid requirements will be conducted to show the impact.

## 1.4 ORGANIZATION OF THE REPORT

The rest of the report is organized as follows:

Chapter 2: "Review of High Voltage SiC Semiconductor Devices" collects the key characteristics of the latest HV SiC devices from commercial vendors and provides a comparison review with Si counterparts;

Chapter 3: “Application Survey and Analysis” presents the survey and summarizes existing and emerging power electronics-based equipment for MV distribution grids;

Chapter 4: “Benchmark of HV SiC Benefits in Conventional AC Microgrids” provides a preliminary assessment of the benefits of the HV SiC-based DER interface converter in comparison with the Si-based approach including converter-level and system-level benefits;

Chapter 5: “Benchmark of HV SiC Benefits in Asynchronous Microgrids” provides a preliminary assessment of benefits for HV SiC-based asynchronous MG PCS in comparison with the Si-based approach including converter level benefits and system-level benefits;

Chapter 6: “HV SiC-based PCS Converter Design Considering Grid Requirements” provides an evaluation of the impact of grid requirements on the HV SiC-based grid-connected converter.

Chapter 7: “Summary and Conclusion” provides a concise summary of the work with major findings listed.

# 2. REVIEW OF HIGH VOLTAGE SIC SEMICONDUCTOR DEVICES

This chapter reviews the state-of-the-art high voltage SiC semiconductor devices. It includes key characteristics of the latest HV SiC devices from commercial vendors and a comparison review with Si counterparts. The ones with the best performance and most appropriate voltage ratings will be selected in the comparison study with Si in Chapters 4 and 5.

Nowadays, high voltage (>3.3 kV) Si power devices such as SCR thyristors, gate turnoff thyristors (GTO), gate-commutated thyristors (GCT), and insulated-gate bipolar junction transistors (IGBT), have reached a zenith of development due to Si physical material limits [19][20]. The voltage capability of Si devices is typically below 6 to 12 kV and, more importantly, the switching frequency capability is nominally less than 1 kHz for these high voltage devices. Moreover, the junction temperatures are usually kept below 125°C which pose cooling challenges and limit their applications in some harsh environment [19].

## 2.1 GENERAL CHARACTERISTICS

Recent breakthroughs in wide bandgap (WBG) SiC material and fabrication technology have led to the development of high-voltage, high-frequency (HV-HF) power devices [21]. SiC exists in a variety of polymorphic crystalline structures called polytypes e.g., 3C-SiC, 6H-SiC, and 4H-SiC. Presently 4H-SiC is generally preferred in practical power device manufacturing for its higher carrier mobility and lower dopant ionization energy [22]. Table 2-1 lists the comparison of the main characteristics between 4H-SiC and Si at 300K [22][23].

Table 2-1. Comparison of Electrical Properties of Si and 4H- SiC

| **Material Property** | **Si** | **4H-SiC** |
|---|---|---|
| **Energy Bandgap $E_G$ (eV)** | 1.12 | 3.26 |
| **Breakdown Field $E_B$ (V/cm)** | $2.5 \times 10^5$ | $2.2 \times 10^6$ |
| **Thermal Conductivity (W/cm°C)** | 1.5 | 4.9 |
| **Saturation Drift Velocity $v_s$ (cm/s)** | $1.0 \times 10^7$ | $2.1 \times 10^7$ |

Compared with high-voltage Si devices, some benefits of SiC devices can be drawn based on the electrical properties:

### 2.1.1 Lower Specific on-Resistance at Same Breakdown Voltage [24][25]

With the breakdown field 10 times higher than that of Si, a thinner drift layer (0.1 times that of Si devices) with a higher doping concentration (more than 10 times higher) can be used for SiC power devices at the same blocking voltage. For unipolar devices such as Schottky diodes and MOSFETS, the combination of a thinner blocking layer and higher doping concentration yields a lower specific on-resistance compared with Si majority carrier devices [19][21].

### 2.1.2 Faster Switching Speed

Two factors contribute to the fast switching characteristic in SiC devices: higher breakdown voltage and higher saturated drift velocity.

First, with lower on-resistance at the same breakdown voltage, a smaller chip size is achieved in SiC unipolar devices such as MOSFET. Therefore, the capacitance is smaller due to the reduced size, and a faster switching speed is realized. For minority carrier conductivity modulated devices such as PiN diodes or IGBTs, as the diffusion length $L$ (required to modulate the conductivity of the blocking layer) is reduced, the lifetime $\tau$ is further reduced according to $L = \sqrt{D\tau}$ ($D$ is the diffusion coefficient) thus resulting in a faster switching speed in SiC IGBTs [21].

Second, minority carriers are swept out of the depletion region at the saturated drift velocity during the turn-off transient. For the reason that the electron saturated drift velocity of 4H-SiC is twice the saturated drift velocity of Si, a higher saturated drift velocity will increase the SiC device switching speed.

### 2.1.3 Higher Current Density and Higher Temperature Operation

The thermal conductivity of SiC is more than 3 times that of Si. Higher thermal conductivity allows dissipated heat to be readily extracted from the device. Hence, a larger power can be applied to the device at a given junction temperature. Also, higher thermal conductivity together with a wide bandgap makes it possible for SiC devices to work in high-temperature applications.

## 2.2 HV SIC CHARACTERISTICS

After intensive developments, the low voltage (600V, 1200V, and to some extent 1700V) SiC devices are becoming commercially available, though still with limited current ratings, and have started to be applied in commercial products. On the other hand, the HV SiC (referred here as 3.3 kV and above) is generally in developmental stages with very limited commercial availability and generally small current ratings. This section summarizes the available information on HV SiC devices and modules from Wolfspeed (formerly Cree), GenSiC, USCi, and Fuji. There are reports of devices from other vendors but we have not found any data on them at the time of this report. Table 2-2 to Table 2-8 summarize the key characteristics of devices, including voltage/current ratings, static and dynamic characteristics, and die sizes.

Table 2-2. Summary of HV SiC Diodes

| Vender | Voltage/current | Static Characteristics | Dynamic Characteristics | Die Size |
|---|---|---|---|---|
| Wolfspeed [25],[26] | 10 kV/10A JBS diode | 4V @10A | $t_{rr}$ = 365 ns, $Q_{rr}$ = 0.84 µC @3.15A | 8.3 mm* 10.6 mm |
| Wolfspeed [21],[27] | 10kV/50A 4H-SiC PiN diode | 3.9V @50A 5.9V @328A | $t_{rr}$ = 200 ns, $di/dt$ = 330 kA/s @10kV/20A | 8.7 mm* 8.7 mm |
| GeneSiC [28] | 12.9 kV SiC PiN diode | 2.8V, 3.3 mΩ-cm$^2$ @ 25 °C | | 2.4 mm* 2.4 mm |
| GeneSiC [28] | 10 kV SiC PiN diode | 2.8V, 5.75 mΩ-cm$^2$ @ 25 °C | $t_{rr}$ = 250 ns, $Q_{rr}$ = 1.67 µC @2.4kV/24A | 6.4 mm* 6.4 mm |
| GeneSiC [28] | 10 kV/2A SiC JBS diode | 0.6V, 114.7 mΩ-cm$^2$ @ 25 °C | | 4.25 mm* 4.25 mm |
| GeneSiC [28] | 10 kV/7A SiC JBS diode | 0.6V, 127.5 mΩ-cm$^2$ @ 25 °C | | 6.89 mm* 6.89 mm |
| USCi [29] | 3.3 kV/50 A SiC JBS diode | 2.3 V | | |
| USCi [29][30] | 6.5 kV/15 A SiC JBS diode | 3.8 V | | 6 mm* 6 mm |
| USCi [30] | 8 kV/5 A SiC JBS diode | 4.0 V | | |

Table 2-3. Summary of HV SiC MOSFETs

| Vender | Voltage / current | Static Characteristics | Dynamic Characteristics | Die Size | Active Area |
|---|---|---|---|---|---|
| Wolfspeed [31] | 1.7kV Gen-3 MOSFET | 3.4 mΩ-cm$^2$ @$V_{gs}$=20V | NG | 2.35 mm * 2.9 mm | 3.41 mm$^2$ |
| Wolfspeed [31] | 3.3kV/25A Gen-3 MOSFET | 10.6 mΩ-cm$^2$ @$V_{gs}$=20V | $E_{on}$ = 0.70 mJ, $E_{off}$ = 0.63 mJ @ 1.8kV/ 25A, 25°C | 5.1 mm * 9.16 mm | NG |
| Wolfspeed [32] | 3.3kV/45A Gen-3 MOSFET | 45 mΩ @ $V_{gs}$=20V, 25°C | $E_{total}$ = 1.1 mJ @ 1.8kV/ 20A, 25°C | 5.1 mm * 9.16 mm | NG |
| Wolfspeed [32] | 3.3kV improved Gen-3 MOSFET | 40 mΩ @ $V_{gs}$=20V, 25°C | NG | 4.82 mm * 8.86 mm | NG |
| Wolfspeed [33],[34] | 10 kV/5A 4H-SiC DMOSFET | 111 mΩ-cm$^2$ @ $V_{gs}$=15V,25°C 313 mΩ-cm$^2$ @200°C | $E_{on}$ = 240 µJ, $E_{off}$ = 50 µJ @ 1.0kV/ 3A, | 5.5 mm * 5.5 mm | 0.15 cm$^2$ |
| Wolfspeed [32] | 6.5kV/30A Gen-3 MOSSFET | 100 mΩ @ 25°C 171 mΩ @ 90°C | NG | NG | NG |
| Wolfspeed [20],[26] | 4H-SiC 10kV/10A MOSFET | 127 mΩ-cm$^2$ @ $V_{gs}$=20V,25°C 283 mΩ-cm$^2$ @ $V_{gs}$=20V,125°C | $E_{on}$ =4.48 mJ, $E_{off}$ =0.81 mJ @ 5.3kV/10A | 8.1 mm * 8.1 mm | NG |
| Wolfspeed [31] | 10kV/20A Gen-3 MOSFET | 86 mΩ-cm$^2$ @$V_{gs}$=20V | $E_{on}$ = 6.5 mJ, $E_{off}$ = 1 mJ @ 6kV/ 20A | 0.54 cm$^2$ | 0.28 cm$^2$ |
| Wolfspeed [32] | 10kV enhanced short circuit Gen-3 MOSFET | 350 mΩ @$V_{gs}$=20V | $E_{total}$ = 21 mJ @ 7kV/15A, FET/FET configuration $E_{total}$ = 6.5 mJ @ 6kV/15A, FET/diode configuration | NG | NG |
| Wolfspeed [20], [23], [35] | 4H-SiC 15kV/10A MOSFET | 580 mΩ-cm$^2$ @25°C | $E_{on}$=14.46 mJ,$E_{off}$=1.88 mJ @ 6kV/10A, 25°C | NG | NG |
| Wolfspeed [31] | 15kV/10A Gen-3 DMOSFET | 208 mΩ-cm$^2$ @$V_{gs}$=20V | $E_{on}$ = 4.8 mJ, $E_{off}$ = 1 mJ @ 6kV/10A, | 0.63 cm$^2$ | 0.32 cm$^2$ |

Table 2-4. Summary of HV SiC IGBTs

| Vender | Voltage / current | Static Characteristics | Dynamic Characteristics | Die Size | Active area |
|---|---|---|---|---|---|
| Wolfspeed [36] | 12kV/0.5A 4H-SiC p-IGBT | 5.3V, 18.6 mΩ-cm$^2$ @ 25°C 5.1V @ 150°C | $t_{on}$ = 40 ns $t_{off}$ =2.8 µs @ 1.5kV/0.55A | NG | 0.4 mm$^2$ |
| Wolfspeed [25],[37] | 12.5kV/35A SiC n-IGBT | 4.1V @5A, 25°C 6.1V, 5.3 mΩ-cm$^2$ @32A, 25°C | $t_{off}$ = 0.65 µs @5kV/5A 25°C, w/ 2umF-S buffer | 6.7 mm * 6.7 mm | NG |

| | | | | | |
|---|---|---|---|---|---|
| | | | $t_{off}$ = 2.3 µs @ 5kV/5A<br>175°C, w/ 2umF-S buffer | | |
| Wolfspeed [25] | 15kV/20A p-IGBT | 6.5V @20A, 25°C | NG | 8.4 mm * 8.4 mm | 0.32 $cm^2$ |
| Wolfspeed [25] | 15kV/20A n-IGBT | 7.0V @20A, 25°C | NG | 8.4 mm * 8.4 mm | 0.32 $cm^2$ |
| Fuji Electric [38] | 16kV flip-type n-IGBT | 6.5V @20A | NG | 5.3 mm * 5.3 mm | 0.09 $cm^2$ |
| Wolfspeed [11] | 22.6kV/20A n-IGBT | NG | NG | 1.0 cm * 1.0 cm | NG |

Table 2-5. Summary of HV SiC BJTs

| Vender | Voltage / current | Static Characteristics | Dynamic Characteristics | Die Size |
|---|---|---|---|---|
| GeneSiC [28] | 10kV/8A SiC BJT | 110 mΩ-$cm^2$ and β > 75 | $E_{on}$ = 4.2 mJ, $E_{off}$ =1.6 mJ @ 5kV/8A | 7.3 mm* 7.3 mm |

Table 2-6. Summary of HV SiC Thyristors

| Vender | Voltage / current | Static Characteristics | Dynamic Characteristics | Die Size |
|---|---|---|---|---|
| GeneSiC [28] | 6.5kV SiC Thyristors | 2.8 mΩ-$cm^2$ | $dv/dt$ = 1920 V/µs @ 3.6 kV/14.5 A | 5.3 mm* 5.3 mm |

Table 2-7. Summary of HV SiC JFETs

| Vender | Voltage / current | Static Characteristics | Dynamic Characteristics | Die Size |
|---|---|---|---|---|
| USCi [30],[39] | 6.5kV/15A normally-off SiC JFET | 350 mΩ @ 25°C | $E_{on}$ = 2.71 mJ, $E_{off}$ = 1.54 mJ @ 3kV/11A | 6.0 mm* 6.0 mm |
| USCi [40] | 6.5kV super cascode SiC JFET | ~ 230 mΩ @ 25°C | $E_{on}$ = 1.2 mJ, $E_{off}$ = 0.53 mJ @ 3kV/11A | NG |

Table 2-8. Summary of HV SiC Power Modules

| Vender | Voltage / current | Static Characteristics | Dynamic Characteristics | Package | Parasitics |
|---|---|---|---|---|---|
| Wolfspeed [32] | 3.3kV/180A SiC MOSFET half-bridge power module | 11.3 mΩ @ 25°C | $E_{total}$ = 45 mJ @ 2.2kV/ 180A, 25°C | 62mm module | NG |
| Wolfspeed [32] | 3.3kV SiC MOSFET half-bridge power module | 5.7 mΩ | NG | XHP™ | < 20nH power loop |
| Wolfspeed [32] | 10kV/240A SiC MOSFET half-bridge power module | 19.4 mΩ | NG | XHV-6 | ~16nH power loop / ~10nH gate loop |
| USCi [30],[39] | 6.5kV/60A SiC normally-off JFET half-bridge module | 100 mΩ @ 25°C | $E_{on}$ =28 mJ,$E_{off}$=9.2 mJ @ 3kV/60A, 25°C | | NG |

From the collected data, several observations can be made. Fig. 2-1 shows the relationship between specific on-resistance and the device breakdown voltage for various SiC MOSFETs from Wolfspeed, including the LV devices [31]. It can be seen that the HV SiC MOSFET characteristics closely follow the SiC material 1-D limit, indicating that the on-resistance is dominated by the drift layer resistance for these devices. Since the $R_{on,sp}$ is proportional to the square of the breakdown voltage for the 1-D limit, it means the lower voltage devices will have lower normalized resistance. For example, $R_{on,sp}$ of a 6.5 kV device is roughly 4 times that of a 3.3 kV device. In other words, with today's technology, the lowest voltage devices (e.g. 3.3 kV) have the lowest $R_{on,sp}$ or normalized forward voltage drop. Table 2-9 shows the normalized behavior under a selected condition, illustrating the same "high voltage penalty". Si MOSFET is subject to its similar 1-D material limit, which has been overcome through structural innovations such as super junctions and trench gates. As a result, Si MOSFET below 1000 V does not suffer the "high voltage penalty". Theoretically, according to the vendors, similar structural innovations could be applied to SiC, though they are not necessarily on the near-term development roadmap for other more important work. In our report, we will use the data for the existing devices rather than those based on projections. It should be noted some of the HV devices use larger die areas for the normalized current ratings, which are not "corrected" in our study either.

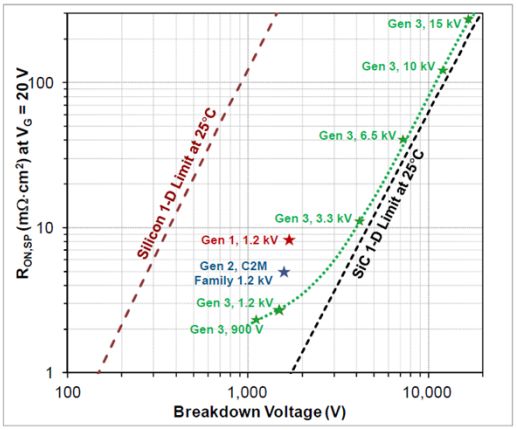



Fig. 2-1 Specific On-resistance as function breakdown voltage (Copy page 24 of the Wolfspeed presentation)

Table 2-9. Conduction and switching loss comparison among different devices @ 25 °C

| Device model | $V_{on}$ for 3.3 kV/1.5kA | Normalized die size | $R_{DSONsp}$ | $E_{on}$ @ 1.8kV/1.5kA | $E_{off}$ @ 1.8kV/1.5kA |
|---|---|---|---|---|---|
| 3.3 kV/1500 A Si IGBT (FZ1500R33HL3) | 2.40 V | N/A | N/A | 2300 mJ | 2400 mJ |
| 4.5 kV/1200 A Si IGBT (FZ1200R45HL3) | 1.90 V | N/A | N/A | 3300 mJ | 3380 mJ |
| 6.5 kV/750 A Si IGBT (FZ750R65KE3) | 2.08 V | N/A | N/A | 4200 mJ | 3600 mJ |
| 3.3 kV/25 A SiC MOSFET | 0.95 V | 1.08 $mm^2/A$ | 10.6 $\Omega \cdot cm^2$ | 42 mJ | 38 mJ |
| 6.5 kV/25 A SiC MOSFET | 1.69 V | 1.2 $mm^2/A$ | 40 $\Omega \cdot cm^2$ | N/A | N/A |
| 10 kV/20 A SiC MOSFET | 2.04 V | 1.4 $mm^2/A$ | 86 $\Omega \cdot cm^2$ | 146 mJ | 23 mJ |
| 10 kV/8A SiC BJT | 1.42 V | 6.7 $mm^2/A$ | 143 $\Omega \cdot cm^2$ | 283.5 mJ | 108 mJ |
| 15 kV/10 A SiC MOSFET | 1.43 V | 3.2 $mm^2/A$ | 208 $\Omega \cdot cm^2$ | 216 mJ | 45 mJ |

As can be seen from the device summary tables, for the active switches, the HV SiC MOSFET are the most developed with some IGBT, BJT, and thyristors also available. From Table 2-9, it can be seen that the advantage of IGBT over MOSFET is very limited. This could be because of the relative developmental immaturity of IGBT or the voltage rating of ~15 kV. In the Si case, IGBT is more advantageous beyond 600 V to 1000 V compared with the MOSFET. For SiC, a similar trend should hold, probably at much higher voltages, that is perhaps at higher voltages (>15 kV), SiC IGBT will be superior to SiC MOSFET. SiC BJT and thyristors may be superior in some cases. As a result, in this study, we primarily focus on SiC MOSFET. For HV diodes, as compared to PiN diodes, Schottky diodes have poor static performance and large conduction loss but with excellent reverse recovery characteristics. Also, considering MOSFET is capable of operating at the third quadrant, therefore, HV SiC Schottky diode is selected as the anti-parallel diode of SiC MOSFET for the later comparison.

In addition, since most HV SiC devices are still in developmental or early commercial stages, their current ratings are small. Therefore, scaling is needed for the comparison with Si devices. Generally, SiC devices with a large current rating can be assumed by paralleling a sufficient number of low current rating SiC devices. Hence, the equivalent on-state resistance is approximately equal to on-state resistance per each small current rating device divided by the number of paralleled devices; the equivalent on-state voltage is kept the same as the on-state voltage per each small device. For dynamic characteristics, the switching losses are scaled based on the linearization of the tested operating voltage/current at the actual operating voltage/current. For example, Table 2-9 data is for scaled devices at 1.8 kV and 1500 A.

# 3. APPLICATION SURVEY AND ANALYSIS

## 3.1 INTRODUCTION

The main objective of this chapter is to survey and summarize all existing and emerging power electronics-based equipment for medium voltage distribution grids, including today's and future grids. The equipment can include the following categories: a) "traditional" custom power equipment, including equipment for power flow control (e.g. solid-state transfer switch, solid-state breakers and fault current limiters), power conditioning (e.g. STATCOM, dynamic voltage restorer, unified power quality conditioner) and active filtering; b) emerging equipment, including renewable energy interface converters, energy storage/charging converters, microgrid interface converters (for both DC and AC) and microgrids; c) some more recent variations of traditional equipment to address the size, cost, controllability, reliability, and issues associated with the high renewables, including solid-state transformer, controlled network transformer and continuously variable series reactor. After the survey and summary, the potential impact of HV SiC on these traditional and emerging applications will be analyzed. The applications with the most promises will be identified and selected for benchmark and design comparison in subsequent chapters.

## 3.2 "TRADITIONAL" CUSTOM POWER EQUIPMENT

Due to better controllability and faster dynamic response over traditional electrical equipment, the power electronics-based equipment can improve the performance of the conventional distribution grid. Like FACTS for flexible ac transmission systems (FACTS) for transmission systems, the term custom power (CP) pertains to the use of power electronic controllers for distribution systems. Just as FACTS improves the reliability and quality of power transmission by simultaneously enhancing both power transfer volume and stability, the custom power enhances the quality and reliability of power that is delivered to customers. There are many different types of custom power devices. In this report, they are grouped into three categories: power flow control/interruption devices, power conditioning and compensation devices, and active harmonic filters.

### 3.2.1 Power Flow Control/Interruption

In this case, the power electronics equipment is used as the switch and can replace the conventional mechanical switches for power flow control and interruption. Several types of equipment developed are described below.

#### 3.2.1.1 Solid-state transfer switch

Many industrial and commercial operations suffer from various types of outages and service interruptions that can cost significant financial loss per incident in terms of lost production, process down-time, and other tangible effects. A solid-state transfer switch (SSTS) can be one of the most cost-effective solutions for these types of power quality problems [150]. The SSTS, which essentially consists of a pair of bi-directional thyristor switching devices, enables seamless transfer of energy from a primary source to an alternate source, thus avoiding service interruption upon the detection of power quality deficiency. The typical schematic diagram is shown in Fig.3-1. Both pure SSTS and hybrid transfer switches with SSTS and mechanical switches were developed [151]. A hybrid transfer switch shows benefits in power loss reduction while pure SSTS has better performance in switching dynamics.

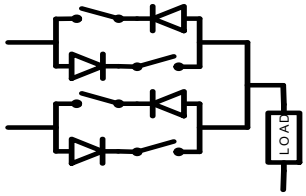



Fig.3-1. Schematic diagram of SSTS.

#### 3.2.1.2 Solid-state circuit breaker

A solid-state circuit breaker (SSCB) can replace the conventional mechanical circuit breaker to achieve a faster dynamic response. Furthermore, the SSCB can be used to interrupt DC current which does not have a zero current crossing and is essential for a DC grid. The typical schematic diagram is shown in Fig.3-2. Both pure SSCB and hybrid circuit breakers with SSCB and a mechanical breaker were developed. The mechanical switch is slow, and the semiconductor switch is lossy. The hybrid DC circuit breaker can achieve both low loss and fast breaking time, which is the trend for future DC breaker development [50].

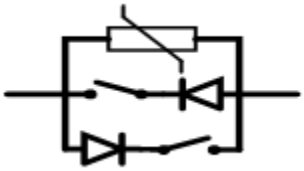


Fig.3-2. Schematic diagram of SSCB.

#### 3.2.1.3 Solid state fault current limiter

The typical schematic diagram of solid state FCL (SSFCL) is shown in Fig.3-3. In normal operation, the solid state switch turns on and the impedance of FCL is nearly zero. When a fault occurs, the switch turns off and the current will flow through an inductor and the fault current is limited. In recent years, many types of SSFCL, such as series switch type, bridge type, and resonant type, were developed based on SCR, GTO, IGCT, and IGBT [152].

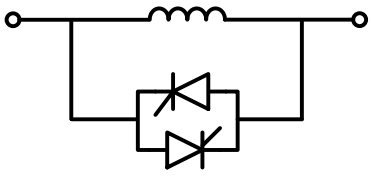


Fig.3-3. Schematic diagram of SSFCL.

### 3.2.2 Power System Conditioning and Compensation

The power system conditioning and compensation equipment is applied to improve the quality of the power that is delivered to electrical load equipment by regulating voltage and compensating reactive power. In conventional distribution grids, these functions are achieved mainly by passive components such as inductors, capacitors, tap changing transformers. To improve the controllability of the grid, power electronics equipment has been developed to replace the passive components as conditioning and

compensation devices [41][42]. Based on their connection schemes in the distribution lines, these conditioning and compensation devices can be categorized into several types [179], which are described below.

#### 3.2.2.1 Distribution static synchronous compensator (DSTATCOM)

The DSTATCOM is shunt connected with the distribution grid, often through a transformer, as shown in Fig.3-4. DSTATCOM is generally based on VSCs and can control the reactive power output by controlling the reactive current injected into the distribution grid.

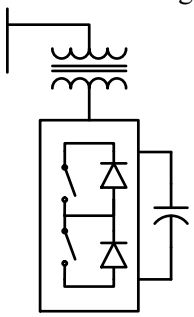


Fig.3-4. Schematic diagram of DSTATCOM.

#### 3.2.2.2 Dynamic voltage restorer

The dynamic voltage restorer (DVR) is a series connected with the distribution line, as shown in Fig.3-5. The function of DVR is similar to that of DSTATCOM which compensates for voltage sags and voltage swells. But different from the operation of DSTATCOM, it is designed to inject a dynamically controlled voltage. The controllable converter is also generally VSC based.

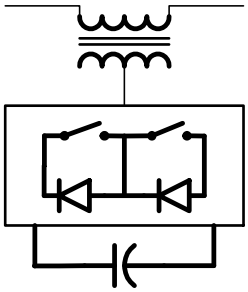


Fig.3-5. Schematic diagram of DVR.

#### 3.2.2.3 Unified power quality conditioner

The unified power quality conditioner (UPQC) is a combination of DSTATCOM and DVR, as shown in Fig.3-6. An UPQC comprises two PWM-controlled converters that use one common DC bus. Two parameters of shunt current and series voltage are used as a reference for the control. In addition to achieving the benefits of the DSTATCOM and DVR, UPQC will allow real power exchange between the shunt- and series-connected VSCs, leading to more benefits.

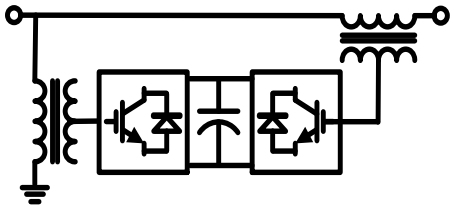


Fig.3-6. Schematic diagram of UPQC.

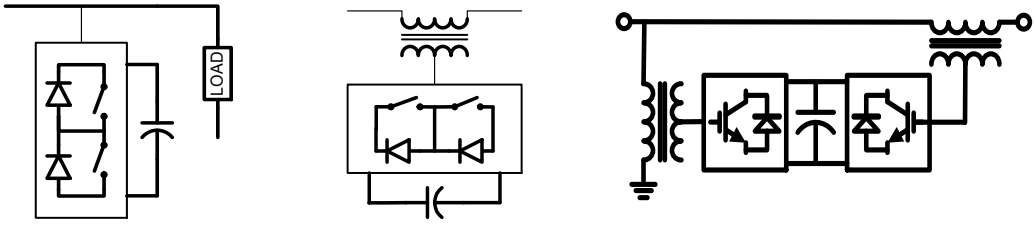
Some other commonly used custom power equipment shown in Fig.3-7 includes static VAR compensator (SVC) and thyristor-controlled voltage regulator (TCVR). These devices are less likely to be impacted by SiC since they do not involve fully controlled switching devices. SVC functions similarly as and can be replaced by the more capable DSTATCOM. TCVR can more smoothly change the transformer turns ratio compared with the traditional tap-changing transformer.

(a) SVC (b) TCVR

Fig.3-7. Schematic diagram of SVC and TCVR.

### 3.2.3 Active Power Filter (APF)

APF works as a controlled current source to compensate for the harmonic currents in the grid. APFs can be categorized as shunt-connected, series-connected, and hybrid-connected APFs according to their connections in a grid, as shown in Fig.3-8. Their topologies are very similar to the compensators.




(a) shunt (b) series (c) hybrid

Fig.3-8. Schematic diagram of APF.

## 3.3 EMERGING APPLICATIONS

This section deals with the emerging power electronics applications at the distribution level, i.e., those associated with distributed energy resources (DER), including photovoltaic (PV), wind, battery, and flywheel energy storage, micro-turbines, fuel cells, and so on. Many of the DERs are included in emerging microgrids (MGs). Therefore, microgrids including AC microgrids, DC microgrids, and asynchronous microgrids are also covered.

### 3.3.1 Renewable Energy Systems

#### 3.3.1.1 Photovoltaic (PV)

PV technology involves converting solar energy directly into electrical energy using a solar cell. For a PV system, the voltage output is a constant DC whose magnitude depends on the configuration in which the solar cells/modules are connected. The main requirement of power electronic interfaces for the PV systems is to convert the generated DC voltage into a suitable AC for consumer use or utility connection. Generally speaking, the DC voltage magnitude of the PV array is required to be boosted to a higher level by using DC-DC converters and then, the DC-AC inverters are utilized to convert the voltage to 60 Hz AC at the standard voltage level. The most common operating mode for a PV system is so-called maximum power point tracking (MPPT). The MPPT control process and the voltage boosting are usually implemented in the DC-DC converter, whereas the DC-AC inverter is used for grid-current control [51].

For PV converters, among the commercial products, the string and modular topologies are the most commonly used configurations [52]. For the string converter, several PV panels are connected in series to form a PV string, and each string is connected to the interface converter. For a modular converter, each PV panel is connected to an interface converter with a lower power rating, which is called a micro-inverter, and multiple micro-inverters are synchronized and connected on their AC sides. Since the medium voltage and high power applications are the main interests of this report, modular PV converters, which are usually used in residential PV systems, are out of scope. We will focus on PV string inverters.

Based on the investigation of existing products of PV string converters, the frequently used configuration is shown in Fig. 3-9 [53-55]. As aforementioned, each PV string is connected to an interface converter, and the voltage rating of this converter is within the low voltage range. Several interface converters are paralleled and collected at the AC side by using a multi-winding step-up transformer, and the secondary side of the transformer has medium voltage output. There are also collections using DC-DC converters and then convert to AC using a large central DC-AC inverter. The transformer then steps up the voltage to the MV distribution level.

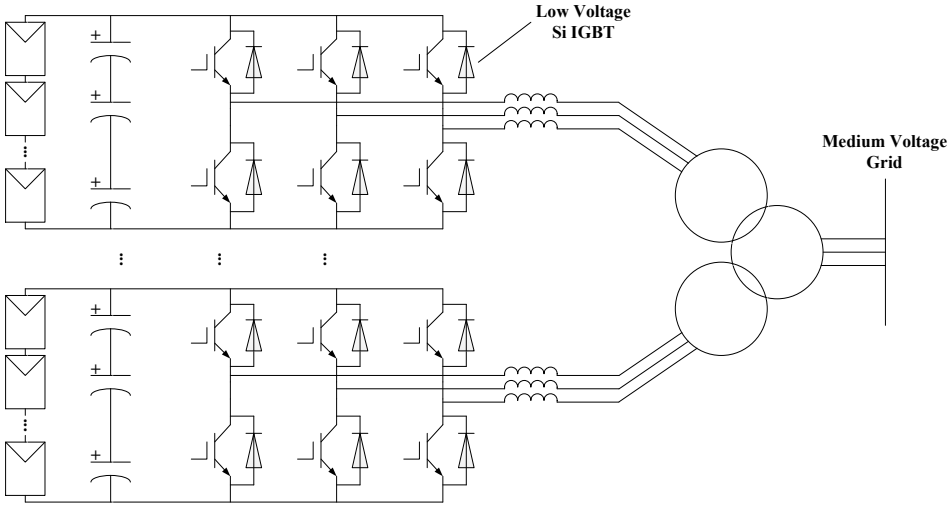



Fig.3-9. Configuration of PV string converter.

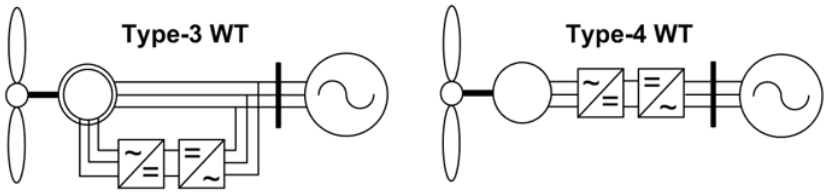
Some of the existing products using the configuration in Fig. 3-9 are listed in Table 3-1[53-55].

Table 3-1. Summary of PV String Converters

| Manufacturer | Power Rating (MW/Module) | DC Voltage (kV) | Topology | Semiconductor |
|---|---|---|---|---|
| ABB | 1.2 | 0.6 – 0.85 | Parallel Two-Level | LV IGBT |
| GE | 1 | 1 | Parallel Two-Level | LV IGBT |
| Advanced Energy | 1 | 0.6 – 1 | Parallel Two-Level | LV IGBT |

#### 3.3.1.2 Wind energy

There are four types of wind turbine generators (Types 1 through 4). Most modern wind turbine generators are Types 3 and 4 which involve power electronics converters and have the ability to perform voltage or reactive power control, similar to synchronous machines. Common control modes include constant power factor control, coordinated control across a wind farm to maintain a constant interconnection point voltage, and constant reactive power control [155]. Type 3 is also called a doubly-fed induction generator (DFIG), which uses a partial power converter; and Type 4 uses a synchronous generator with a full power converter. The configurations of Type 3 and Type 4 wind turbine generators are shown in Fig.3-10.




(a) Type 3. (b) Type 4.

Fig.3-10. Configurations of wind turbines.

For wind converters, single or paralleled two-level converters are widely used in low-voltage range, and multilevel converters are the main topologies in MV applications. Considering the existing products of MV wind converters, the frequently used configurations include three-level or five-level neutral point clamped (3L-NPC, 5L-NPC) converter, and cascaded H-bridge (CHB) converter [57]. As shown in Fig.3-11, the 3L-NPC converter is selected as an example to show the multilevel configuration for a medium voltage wind converter.

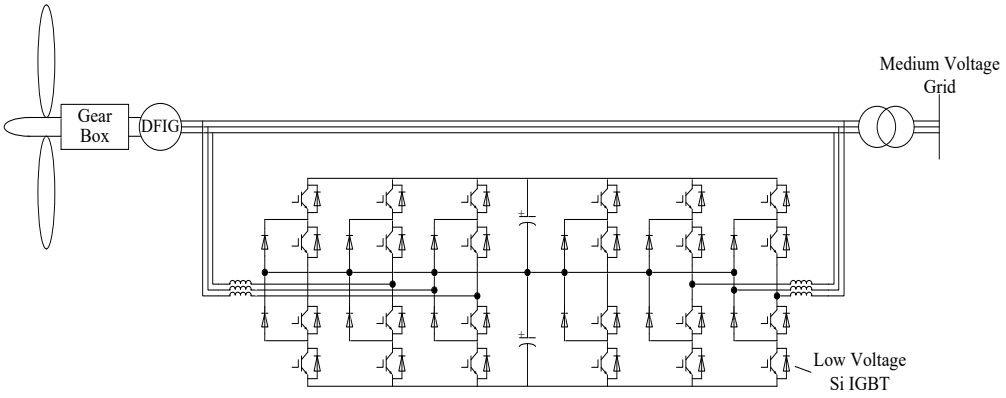


Fig.3-11. 3L-NPC wind converter.

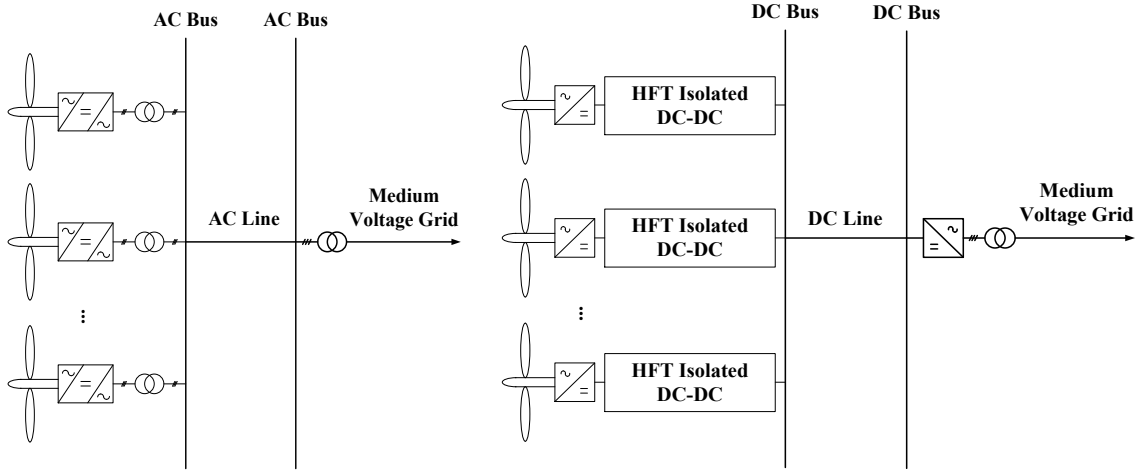
Some of the existing products of MV wind converters are listed in Table 3-2 [56].

Table 3-2. Summary of Wind Converters

| Manufacturer | Power Rating (MW) | Voltage (kV) | Topology | Semiconductor |
|---|---|---|---|---|
| ABB | 4 – 9 | 3.3 – 4.16 | 3L-NPC | IGCT |
| Siemens | 0.6 – 10.1 | 2.3 – 6.6 | 3L-NPC | IGBT |
| GE | 7.5 | 4 – 4.2 | 3L-NPC | IGBT |

Considering the existing complex converter topology (e.g. multiple parallel-connected in PV and three-level and multi-level in wind turbine) and the huge transformer, the HV SiC device can be employed to simplify the topology and increase the power density of the whole system. With the high switching frequency of SiC devices, the AC filter size can be reduced, further improving the system power density.

One wind application that may benefit particularly from HV SiC devices is offshore wind farms. The configuration of the AC grid-based offshore wind farm is shown in Fig.3-12(a). In this conventional configuration, since the line frequency or low-frequency transformer (LFT) is employed, the power density is relatively low. Considering the actual implementation and maintenance of offshore wind farms, compact energy conversion system is desirable. By employing the MV SiC device, the system configuration can be modified with the DC/DC converter with a high-frequency transformer (HFT) to form a solid-state transformer (SST). By using SST, the LFT can be eliminated. Meanwhile, the conventional two-stage topology of the AC-DC-AC converter can be simplified as an AC-DC converter, so the DC-AC stage is moved to the on-shore system. Hence, the power density of the offshore system can be improved. The configuration of the DC-based offshore system is shown in Fig.3-12 (b).




(a) AC-based wind farm. (b) DC-based wind farm.

Fig.3-12. Configuration of the off-shore wind farm.

### 3.3.2 Energy Storage Systems

There are a variety of technologies that can be used to store energy in the utility power system, including batteries, superconducting magnetic energy storage (SMES), flywheels, electrochemical capacitors (ultracapacitors), compressed air energy storage (CAES), pumped hydro; and production and storage of

gases such as hydrogen (to run fuel cells or hydrogen IC engines). Of these technologies, batteries and flywheels are commonly integrated at the distribution system level and are commercially available.

#### 3.3.2.1 Battery

A battery produces DC voltage that must be converted to AC to connect to the utility. The individual battery cells are generally connected in different configurations in series and/or parallel to achieve the required voltage and current outputs. The power conditioning systems, including inverters and DC-DC converters, are often required for the battery energy storage systems (BESS). The unique aspect of power electronics for energy storage is that they must be bidirectional, that is both taking power (during charging) and providing power (during discharge) from/to the grid. Unlike PV and fuel cell inverters, however, BESS inverters are not expected to consider the peak power operations. They only provide the power level demanded by the system that can be sustained by the battery.

The simplest form of battery energy storage system configuration, as shown in Fig.3-13, consists of a battery system followed by the DC-AC converter. If the isolation or a high ratio of the voltage conversion is required, a transformer is usually integrated into the system. The current at full operating power determines the rating of the inverter. The current, in turn, is dependent on the BESS voltage at full operating power, which varies substantially from no-load to full load.

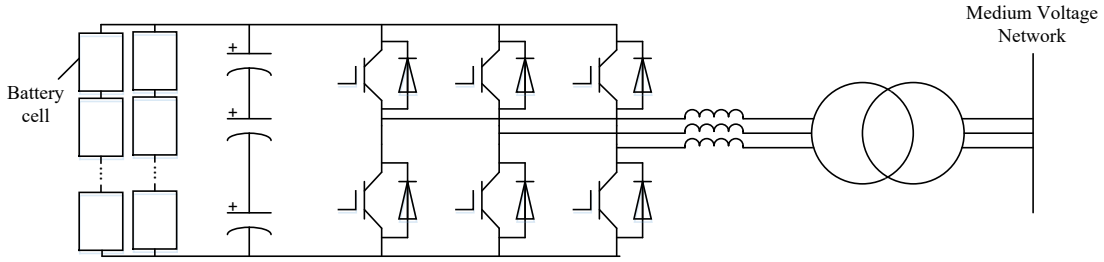



Fig.3-13. Configuration of BESS.

Some of the existing products of MV BESS converters are listed in Table 3-3 [59-61]. The real project of MW BESS M5BAT (6.3 MW/5.4 MWh) is also in construction [62].

Table 3-3. Summary of BESS Converters

| Manufacturer | Power Rating (MW) | Voltage (kV) | Topology | Semiconductor |
|---|---|---|---|---|
| Siemens | 0.36 – 2.16 (scalable) | 0.4 | Parallel Two-Level | IGBT |
| ABB | 0.5 – 4 | up to 0.69 | Parallel Two-Level | IGBT |
| GE | 1.262 | 0.48 | Parallel Two-Level | IGBT |

The main drawback of this configuration is that the low-frequency transformer placed at the output of the inverter makes the system very bulky and expensive [63]. With HV SiC devices, the bulky and lossy low-frequency transformer can be replaced by a lighter and more efficient high-frequency transformer.

#### 3.3.2.2 Flywheel

A Flywheel energy storage system (FESS) stores energy in the form of the kinetic energy of a spinning mass. Conversion from kinetic to electric energy is accomplished by electric machines. FESS utilizes power electronics that convert and regulate the power output from the flywheel. The major electrical components

of a flywheel energy storage system include a bidirectional inverter (Converter 2) and variable-speed motor drive (Converter 1 plus motor/generator) as shown in Fig.3-14.

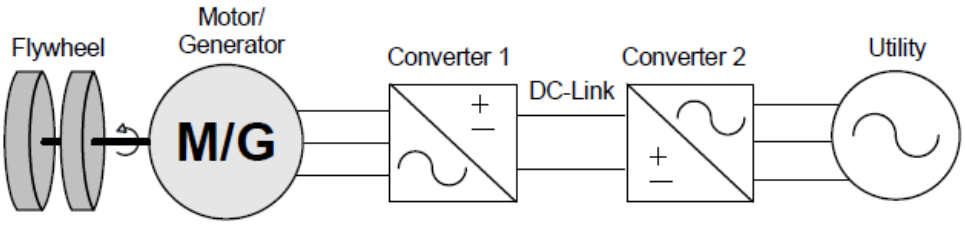


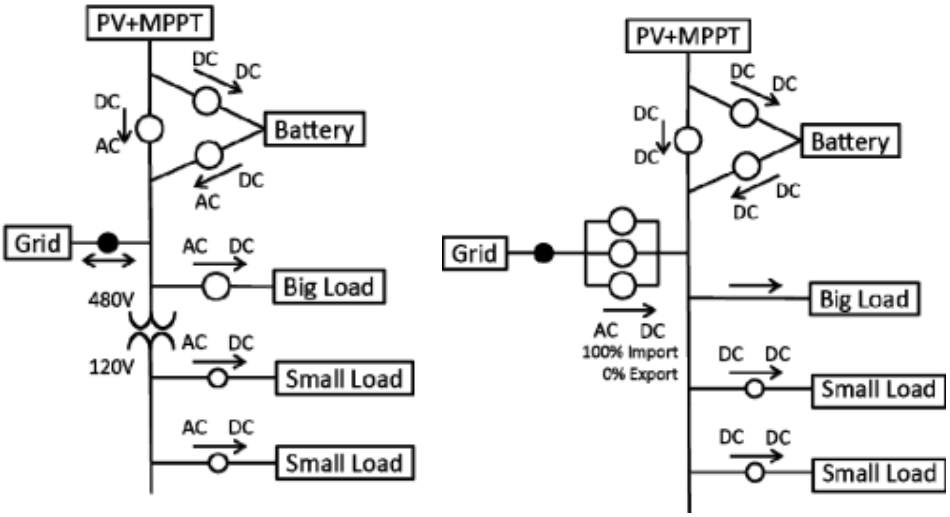

Fig.3-14. Configuration of the flywheel.

The flywheel energy storage systems (FESS) can be classified into two categories. The first technology is based on low-speed flywheels (up to 6000 rpm) with steel rotors and conventional bearings. The second involves more recent high-speed flywheel systems (up to 60000 rpm) that are available commercially and make use of advanced composite wheels that have a much higher energy and power density than steel wheels [66].

Due to the high speed of the motor in flywheel systems, the switching frequency of Converter 1 is required to be high. An induction machine-based FESS which consists of a 20 kHz high-frequency back-to-back pulse density modulated (PDM) converters was published [156]. Therefore, the HV SiC devices are very attractive in the FESS due to their high switching frequency.

### 3.3.3 Microgrids

The microgrid concept has been proposed [158] as a solution to integrating large amounts of distributed energy resources (DER) without disrupting the operation of the utility grid. Microgrids can even provide ancillary services such as local voltage control. During disturbances on the main grid, microgrids can island disconnect and continue to operate autonomously. As a result, microgrids can improve reliability and power quality. The microgrids can be categorized into AC microgrids and DC microgrids depending on the microgrid voltage types [159], as shown in Fig.3-15.




(a) AC microgrid. (b) DC microgrid.

Fig.3-15. Architectures of microgrids.

The asynchronous microgrid through a power conditioning system (PCS) has been proposed and promoted recently [15][176]. A typical architecture of an asynchronous microgrid is shown in Fig.3-16. The asynchronous microgrid has two features: a) It can decouple the conventional AC microgrid from the utility distribution grids with the PCS; b) Considering the DC link of the PCS can be used to interface DERs, the asynchronous microgrid could be a hybrid microgrid that comprises a DC link and AC microgrid [177]. Some studies have shown the benefits of the asynchronous microgrid in power quality, power loss, and operation in transitions and short circuits [15][176]. The converter control in the asynchronous microgrid has been studied as well [177].

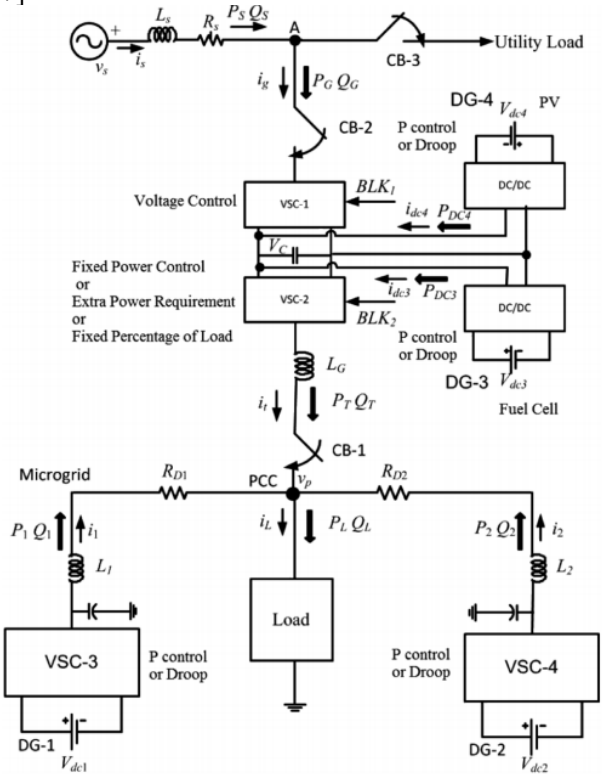



Fig.3-16. Architectures of the asynchronous microgrid.

## 3.4 RECENT DEVELOPMENT AND VARIATIONS

The traditional power electronics-based custom power equipment has limited applications in distribution grids mainly due to their cost and reliability concerns. Some more recent variations have been developed to address these issues, as well as to improve density, controllability, and easy integration with renewable energy sources. The equipment in this category includes solid-state transformers, controllable network transformers, and continuously variable series reactors.

### 3.4.1 Solid State Transformer

With the development of high voltage high-frequency power semiconductor devices (e.g. SiC device) and high-frequency magnetic material, the solid-state transformer (SST) was proposed to replace conventional transformers in some applications [23]. The configuration of SST is shown in Fig.3-17. Compared to conventional transformers, it has benefits in weight, size, as well as flexible controllability. The SST has shown significant benefits over conventional transformers in traction systems and smart grids [67].

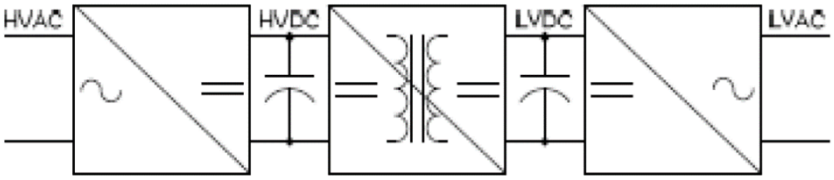



Fig.3-17. Configuration of SST.

The ABB's medium frequency transformer (MFT) based converter system for locomotives [68] weighs 4500 kg, and the specific power density of its front-end MFT and rectifier is 0.5 ~ 0.75 kVA/kg. For a comparable conventional system, the specific power density of the front-end LFT and rectifier is 0.2 ~ 0.35 kVA/kg. Therefore, the power density has increased by over 100%. With the HV SiC-based HFT, the power density improvement is expected to be even higher.

A 1 MW, 4160 VAC/ 1000 VDC converter with a 40 kHz isolation transformer, developed under DARPA-ONR High Power Electronics (HPE) program using the prototype Wolfspeed 10 kV SiC MOSFET, has been designed and built by GE. This prototype unit weighs 900 kg, which is approximately 10% of the 60 Hz transformer-rectifier unit used currently. The volume is also reduced to a third of the existing unit [69].

All applications can make use of SST to replace the LFT for significantly improved power density while maintaining high efficiency. Due to the high requirement for the switching frequency in SST, HV SiC can play a major role in the development of this technology.

### 3.4.2 Controllable Network Transformer

The controllable network transformer (CNT), as shown in Fig.3-18, can achieve power flow control by providing simultaneous control of bus voltage magnitudes and phase angles by augmenting an existing load tapped transformer with a small converter [178]. The load tapped transformer has two taps at (1+N) p.u. and (1-N) p.u.. By controlling the switches using a fixed duty cycle, the voltage magnitude of the output voltage can be varied between (1+N) p.u. and (1-N) p.u.. One way to achieve output voltage phase angle control is by using the dual virtual quadrature sources technique. It has been shown that if an even harmonic is introduced in the duty cycle, the phase of the output fundamental voltage can be shifted and controlled. The resulting output voltage consists of a third (or an odd) harmonic component in addition to the phase-shifted fundamental component [178]. In this way, the active power and reactive can be both controlled by the CNT.

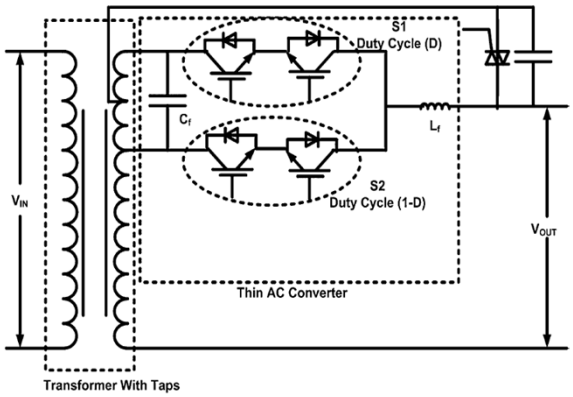



Fig.3-18. Schematic diagram of CNT.

### 3.4.3 Continuously Variable Series Reactor

The continuously variable series reactor (CVSR), as shown in Fig.3-19, can be used to control the power flow by regulating the impedance in grids. The AC winding is the controlled element that can be connected to an AC line, while the DC current regulator is the controlling element for CVSR through DC winding, which can vary the DC bias flux as well as the magnetization level of the saturable core. As a result, the AC reactance reaches the maximum value when the bias DC flux equals zero, and the minimum value when the core is fully saturated. The DC current controller is realized through a power electronics converter with a rating of only a small fraction of the AC winding.

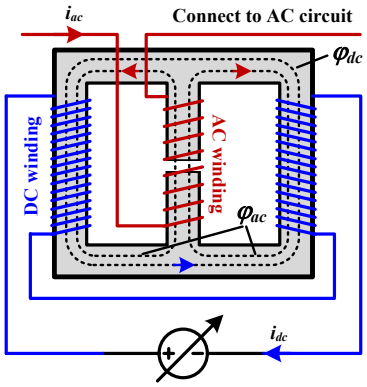



Fig.3-19. Schematic diagram of CVSR.

## 3.5 POTENTIAL BENEFITS OF HV SIC

There are in general three ways that HV SiC can benefit any application, including distribution grid applications: direct device substitution, topology simplification, and new or enhanced functionality or even applications. They are briefly described here corresponding to the distribution grid application.

### 3.5.1 Direct Device Substitution

Due to the lower power loss of SiC devices over Si devices, a direct substitution using SiC devices can lead to gains in efficiency and a corresponding reduced need for cooling. All equipment could benefit from this to some extent.

### 3.5.2 Topology Simplification

HV SiC devices have high breakdown voltages than Si and LV SiC devices. In addition, SiC can switch much faster than Si. As a result, some converter designs can be simplified, especially, those topologies requiring many series/paralleled Si devices or many levels to achieve the needed voltage level or needed equivalent switching frequency. Most power electronics converters for medium voltage applications exceed the voltage capabilities of the available Si devices (e.g. the highest Si IGBT voltage is 6.5 kV). In addition, the HV Si devices have limited switching capabilities (e.g. the 6.5 kV Si IGBT nominally switches at about 1 kHz or less), resulting in low control bandwidth and large pulsating ripple or energy. As a result, multi-level converters, paralleled converters, and/or large passive components for filtering and energy storage will be needed. With faster switching of HV SiC devices, the need for complex topology and large filters can be alleviated. The topology simplification should lead to lower cost, higher reliability, and high power density.

### 3.5.3 New/Enhanced Functionality/Applications

With high switching speed and frequency, HV SiC devices can enable MV power converters with higher control bandwidth and faster dynamic response. These features can lead to new or enhanced functionality in existing applications or even new applications. Let's examine the benefits of different categories of equipment:

- For traditional custom power equipment: a) The APF functions can be integrated into power conditioning and compensation equipment, given the switching frequency can be much higher than the harmonic frequencies. The integration can reduce the need for dedicated APF, leading to lower overall converter ratings and cost; b) For interruption equipment like SSTS, SSCB, and SSFCL, the HV SiC device can potentially speed up the response time and improve system reliability and reduce cost for energy storage passive components; c) The high control bandwidth could enable the equipment to be used in stabilizing the system.
- For emerging equipment, mainly the DER interface converters, the items a) and c) above are both still valid. For microgrids that can involve DERs and traditional custom power equipment (power conditioning/compensation devices, interruption devices, and APF), the benefits of the HV SiC can potentially all be on display. Furthermore, there are more requirements for microgrids and their DERs, such as operation in different modes (grid-connected and islanded modes) and abnormal conditions (e.g. low-voltage and low-frequency ride through, black start). With higher switching frequency and higher control bandwidth, SiC-based interface converters can have a better transition between different modes and faster response to abnormal conditions.

For recent variations and development, SST will directly benefit from the high switching capability of the HV SiCs, as already discussed in Section 3.4.

## 3.6 SELECTION OF THE "KILLER APPLICATION"

From the above discussions, it can be seen clearly that all power electronics equipment for MV distribution grids can benefit from HV SiC devices in terms of direct substitution, most equipment can also have simplified topologies and smaller filters, and some equipment will have enhanced functionality of integrated filtering and system stabilizer. Some new applications, such as SST, will be enabled by the HV SiC.

Because of the environmental concerns and greatly increased percentage of DERs in the grid, microgrids are being promoted world widely in the last decade. Microgrids also can enhance reliability, important for critical infrastructures including manufacturing facilities. Different from the stand-alone power electronics equipment, the microgrid, as an interface between the DERs and utility grid, is a combination of DERs, loads, and storage systems. Seen from the main grid, the microgrid can be regarded as a "single controllable entity", which can connect to the main distribution system and provide ancillary grid support functions, or be totally separated from it when the grid fails or the power quality is not satisfactory. However, the control capabilities of power electronics converters have not been fully utilized to help address some potential issues existing in the main grid. On the other hand, including multiple power electronic converters (e.g. DC/DC and DC/AC for battery and PV, AC/DC/AC or AC/AC for wind turbine generators), the microgrid itself, is facing various challenges, e.g. MV converter design, stability, control mode transition, etc., and should be fully investigated and understood. As discussed above, HV SiC can also help improve these converters and enhance their system capabilities and functionalities. Therefore, for better grid integration of renewable sources and high research impacts for future distribution grids, the microgrid is selected as the base benchmark case in this report. In other words, the MV microgrid is identified as the "killer application" for HV SiC devices for further evaluation and comparison with the Si device-based solutions.

Note that applications such as MV SST and SSCB have been identified as “killer applications” in some previous work and will not be the focus of this report. They can both be used in MV microgrids and even integrated into some other equipment.

# 4. BENCHMARK OF HV SIC BENEFITS IN CONVENTIONAL AC MICROGRIDS

## 4.1 INTRODUCTION

Based on the survey and evaluation in Chapter 3, the microgrid is selected as the high-impact application for the further benchmark of potential benefits of HV SiC. A more "conventional" AC microgrid, which operates synchronously with the main grid, is benchmarked in this chapter. A microgrid may contain a large number of distributed energy resources (DER), such as photovoltaic (PV), battery energy storage system (BESS), wind energy, etc. Considering the characteristics are similar between different kinds of DER converters, a PV system and a BESS system are selected as representatives of DERs. The configuration of the benchmark based on a MV conventional synchronous microgrid is shown in Fig.4-1.

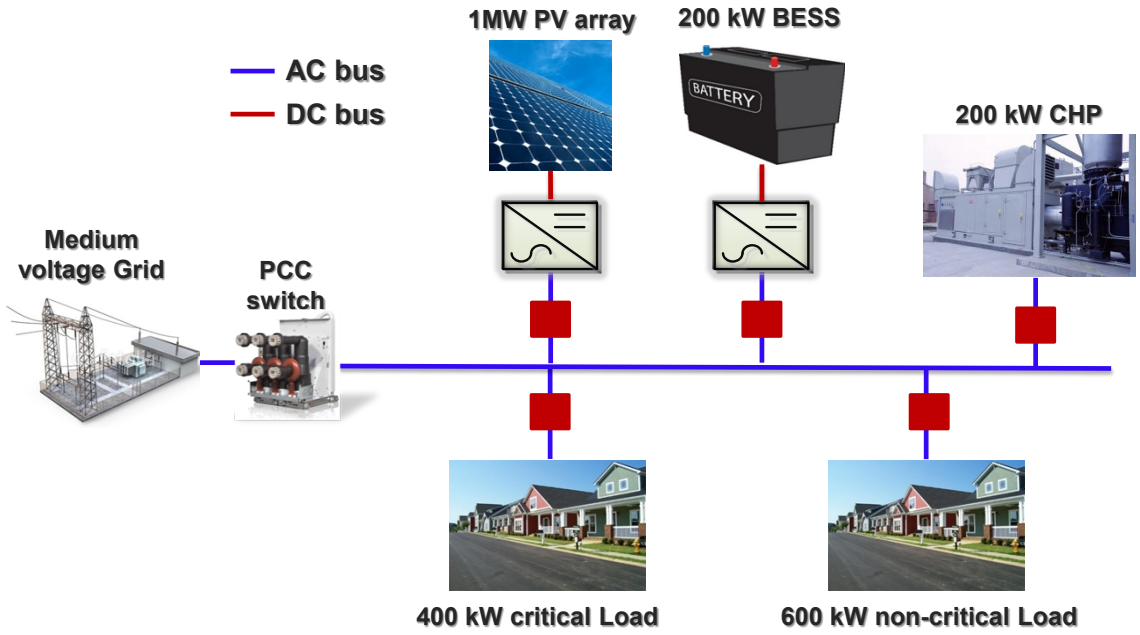



Fig. 4-1. Configuration of MV conventional synchronous microgrid.

The main objective of this chapter is to assess the potential benefits of the HV SiC device-based DER converter both at the converter level and system level. At the converter level, designs of Si- and SiC-based converter solutions are compared using a utility-scale MW-class medium voltage PV inverter as an example. For the system level benefits, the enhanced power quality, enhanced system stability, and low voltage ride through (LVRT) capability are illustrated through simulation.

## 4.2 CONVERTER LEVEL BENCHMARK

Power electronics converters in a conventional microgrid can include interface converters for PV, wind, BESS, and like. In this section, a MW-class PV interface converter, the most popular DER interface converter, is designed based on HV SiC devices, and compared with the Si device-based solution.

Table 4-1. Specifications of the PV converter

| | | | |
|---|---|---|---|
| **Input (DC)** | | | |
| **Peak input power** | 1.2 MW | **Peak DC current** | 1.71 kA |
| **DC voltage, MPPT** | 600 ~ 850 V | **Peak DC voltage** | 1.1 kV |
| **Output (Three-phase AC)** | | | |
| **Nominal output power** | 1 MW | **Peak output power** | 1.2 MW |
| **Nominal AC voltage** | 400 V (±10%) (Si)<br>13.8 kV (±10%) (SiC) | **Nominal AC current (rms)** | 1,519 A (Si)<br>44 A (SiC) |
| **EMC** | FCC 15 CLASS B | **THD** | <3% |
| **Maximum efficiency** | 98.8% | **Power factor** | 0.95 |
| **Grid function** | Reactive power compensation, power curtailment, low voltage ride-through (LVRT) | | |
| **Ambient temp range** | -15ºC ~ 55ºC | **Cooling** | Forced air |

The specifications of the PV converter are listed in Table 4-1. The power rating of the PV converter is selected as 1 MW (1.2 MW maximum input power which is used in the design). The input voltage is 600 ~ 800 V DC and the output voltage is 13.8 kV AC, corresponding to the voltage of the MV AC microgrid. A commercial Si-based PV interface converter topology that uses a two-level voltage source inverter with 400 V AC output and a 400 V/13.8 kV low-frequency step-up transformer is selected as the basis for design comparison.

With HV SiC devices, the SiC-based design can use the combination of a DC-DC converter with a high-frequency transformer and a three-level neutral point clamped (NPC) inverter, eliminating the low-frequency transformer. The device selection for each comparison group is based on the following criteria: 1) Voltage rating of devices should have a sufficient margin per DC link voltage requirement; 2) Current rating of devices is twice the peak load current corresponding to 200% of the rated load current, assuming a 100% overload capability; 3) Since the available HV SiC devices have relatively low current ratings, it is assumed that a sufficient number of these low current devices can be paralleled to achieve the required current capability per MW-class converter need.

The design of Si-based and SiC-based PV interface converters are presented in Sections 4.2.1 and 4.2.2, respectively; their comparison is discussed in Section 4.2.3. The comparison here focuses on power loss and efficiency, weight, and size.

### 4.2.1 Si-Based PV Converter Design

The topology of the Si-based PV converter as shown in Fig.4-2 consists of a two-level voltage source inverter (600~850 V DC input, 400 V AC output), LCL filter, EMI filter, and 400 V/13.8 kV low-frequency transformer.

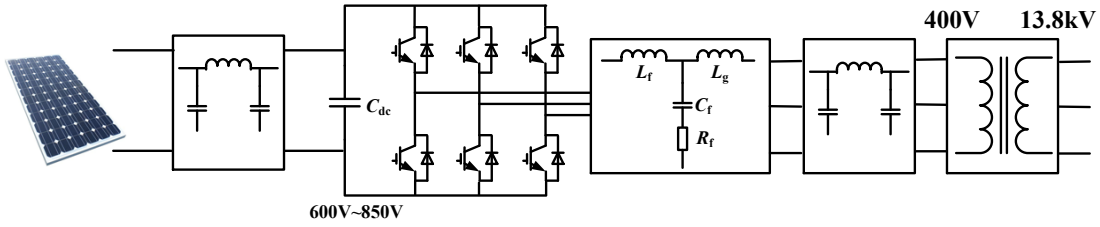



Fig. 4-2. Si-based PV converter.

#### 4.2.1.1 Main circuit

Table 4-2. Parameters of the main circuit

| Parameters | Value |
|---|---|
| **DC-link voltage** | 600 V ~ 850 V |
| **Peak power** | 1.2 MW |
| **Peak current** | 2,865 A |
| **Power electronics device** | 1.7 kV/5.73 kA IGBT |
| **Switching frequency** | 3 kHz |
| **DC-link capacitor** | 50 mF |
| **Modulation** | DPWM |

The main circuit of the converter is a two-level voltage source inverter with LV Si IGBT. The parameters are listed in Table 4-2. The maximum power output of the PV cells is 1.2 MW. Considering a 0.95 power factor at a 10% low line condition, the peak current reaches 2,865 A. Therefore, 1.7 kV/5.73 kA IGBT is used here, and a switching frequency of 3 kHz is selected. DC-link capacitance is decided by the following criteria: with maximum power output and zero power input in one switching cycle, the voltage change does not exceed 3% of the rated DC-link voltage. Therefore, the DC-link capacitance is selected as 50 mF. Discontinued pulse width modulation (DPWM) is adopted.

Based on the main circuit parameters, the power loss can be calculated by simulation and the heatsink is designed based on the power loss calculation. The loss calculation and heatsink design are listed in Table 4-3. The power loss is calculated both at 25°C and 125°C junction temperatures. The output characteristics and switching loss of the devices are from the datasheet of commercial Si IGBT (FZ1800R17HE4). The maximum allowed junction temperature is 125°C and the power loss @125°C is used to design the heatsink. The forced air cooling is applied, and the air flow velocity is 4.3 m/s (based on the cooling system of ABB PVS800). The maximum ambient temperature of operation is 55°C. The maximum allowed case to ambient thermal resistance can be obtained based on the power loss @125°C. 6063-T5 Aluminum Extrusion Alloy is used as the heatsink material. The total weight of the heatsink in the Si-based PV converter is 72.6 kg. The total weight and size of the overall power electronics devices are 13.3 kg and 0.012 $m^3$.

Table 4-3. Power loss calculation and heatsink design

| **Power loss calculation** | |
|---|---|
| **IGBT conduction** | 917 W@25°C / 1.04 kW@125°C |
| **IGBT switching** | 457 W@25°C / 706 W@125°C |
| **Diode conduction** | 144 W@25°C / 120 W@125°C |
| **Diode switching** | 80 W@25°C / 208 W@125°C |
| **Total loss** | 9.6 kW@25°C / 12.4 kW@125°C |
| **Heatsink design** | |
| **Cooling** | Forced air |
| **Rj-c** | 5.5 K/kW |
| **Airflow** | 4.3 m/s |
| **Rc-a** | 4.8 K/kW |

| | |
|---|---|
| **Material** | 6063-T5 Aluminum Extrusion Alloy |
| **Weight** | 72.6 kg |
| **Size** | 0.06 $m^3$ |

#### 4.2.1.2 LCL filter

The LCL filter is designed according to the THD requirement (THD<3%). The electrical parameters are listed in Table 4-4. The simulation result in Fig.4-3 shows that the THD satisfies the requirement (THD=2.65%<3%). Based on the electrical parameters and current rating, the physical design is done using silicon steel as the core material. The physical parameters are also listed in Table 4-4. The total weight of the LCL filter is 1,917 kg and the total loss is 1,371 W.

Table 4-4. LCL filter design

| | |
|---|---|
| **Electrical parameters** | |
| **Inverter-side inductor** | 64.8 μH (0.153 p.u.) |
| **Grid-side inductor** | 45.4 μH (0.107 p.u.) |
| **Filter capacitor** | 498 μF (0.03 p.u.) |
| **Damping resistor** | 0.08 Ω (1/3 of $Z_{Cf}$ at the resonance frequency) |
| **Resonance frequency** | 1.382 kHz (46% of the switching frequency 3 kHz) |
| **Physical parameters** | |
| **Material** | Silicon steel |
| **Copper weight** | 101 kg (64.8 μH)/71 kg (45.4 μH) |
| **Coil weight** | 712 kg (64.8 μH)/499 kg (45.4 μH) |
| **Accessories** | 314 kg (64.8 μH)/220 kg (45.4 μH) |
| **Total weight** | 1,127 kg (64.8 μH)/790 kg (45.4 μH) |
| **Power loss** | 796 W (64.8 μH)/575 W (45.4 μH) |
| **Size** | 0.7 $m^3$(64.8 μH)/0.5 $m^3$(45.4 μH) |

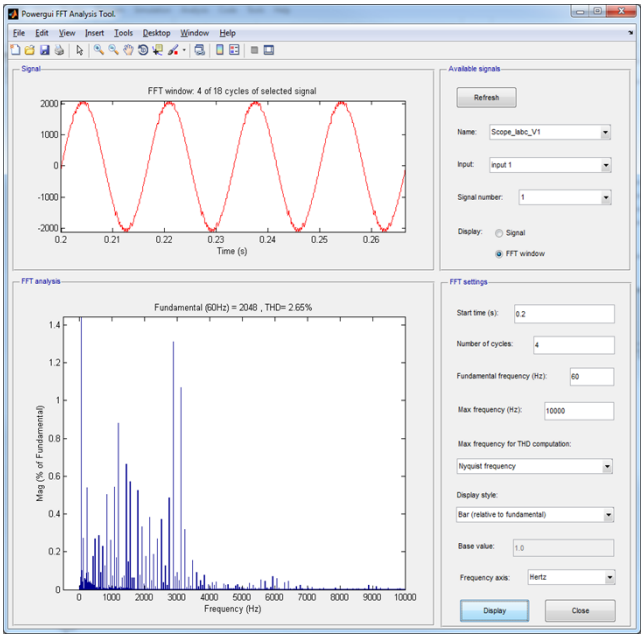
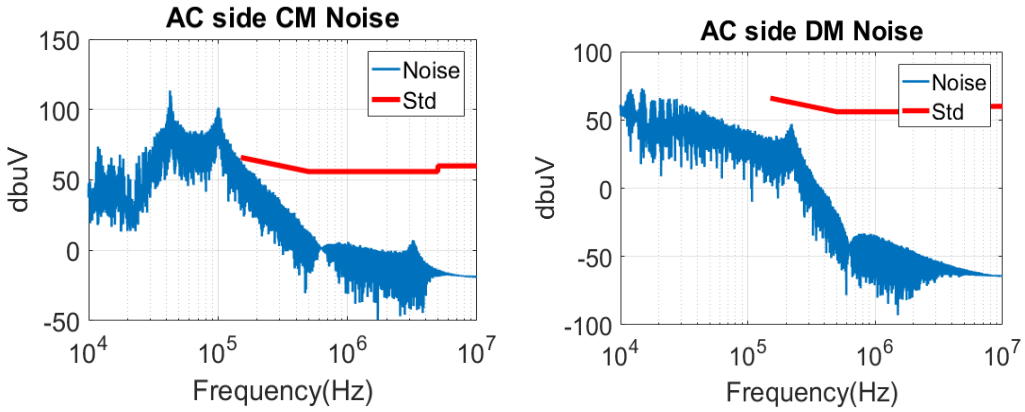



Fig. 4-3. THD simulation.

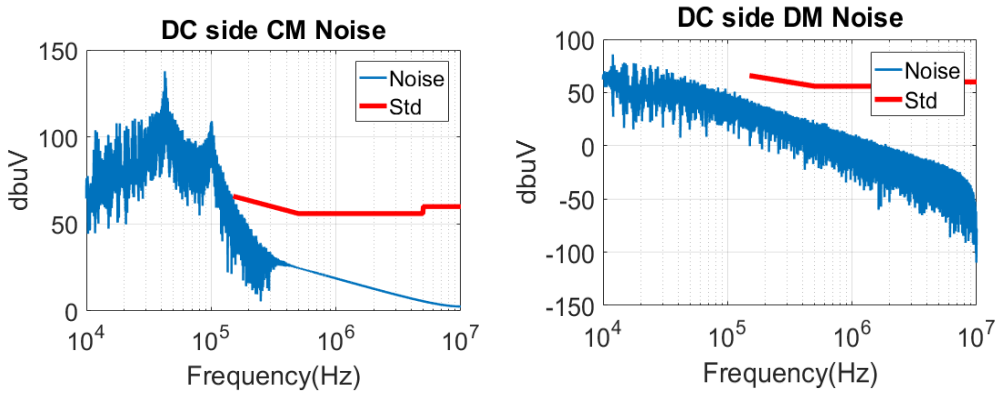
#### 4.2.1.3 EMI filter

The EMI filter is designed to satisfy FCC 15 CLASS B standard. The EMI filters are required on both AC and DC sides. The LCL and CLCL type EMI filters are applied respectively. The electrical parameters are listed in Table 4-5. The simulation result in Fig.4-4 shows common mode (CM) and differential mode (DM) noise satisfy the requirement. Based on the electrical parameters and current rating, the physical design is done using FT-3M (high frequency nanocrystalline magnetic material). The physical parameters are also listed in Table 4-5. The total weight of the EMI filter is 259 kg, and the total loss is 275 W.




(a) CM noise in AC side

(b) DM noise in AC side




(a) CM noise in DC side (b) DM noise in DC side

Fig. 4-4. CM and DM noise simulation.

Table 4-5. EMI filter design

| | | |
|---|---|---|
| **Electrical parameters** | | |
| EMI filter on AC side (LCL filter) | $L_{cmac}$ | 50 μH |
| | $C_{cmac}$ | 40 nF |
| EMI filter on DC side (CLCL filter) | $L_{cmdc}$ | 400 μH |
| | $C_{cmdc}$ | 20 nF |
| **Physical parameters** | | |
| Material | | FT-3M |
| **Copper weight** | | 13.3 kg (400 μH) / 2.9 kg (50 μH) |
| **Coil weight** | | 150.5 kg (400 μH) / 20.3 kg (50 μH) |
| **Accessories** | | 63 kg (400 μH) / 9 kg (50 μH) |
| **Total weight** | | 226.8 kg (400 μH) / 32.2 kg (50 μH) |
| **Power loss** | | 188 W (400 μH) / 87 W (50 μH) |
| **Size** | | 0.14 $m^3$(400 μH)/0.02 $m^3$(50 μH) |

#### 4.2.1.4 Low-frequency transformer

A commercial 400 V/13.8 kV 60 Hz transformer is used here and the data is listed in Table 4-6. Considering a 1.2 MW maximum output power and a 0.95 power factor, the capacity is selected as 1.25 MVA. The weight is 3,000 kg and the efficiency is 99.5%.

Table 4-6. Low-frequency transformer design

| | |
|---|---|
| **Electrical parameters** | |
| **Capacity** | 1.25 MVA |
| **Turns ratio** | 400 V / 13.8 kV |
| **Frequency** | 60 Hz |
| **Physical parameters** | |

| | |
|---|---|
| **Material** | Silicon steel |
| **Weight** | 3,000 kg |
| **Power loss** | 5 kW |
| **Size** | 1.95 $m^3$ |

### 4.2.2 SiC-Based PV Converter Design

The topology of the SiC-based PV converter as shown in Fig.4-5 consists of a DC-DC converter with phase shift full bridge topology (PSFB), a three-level NPC DC-AC inverter, LCL filter, and EMI filter.

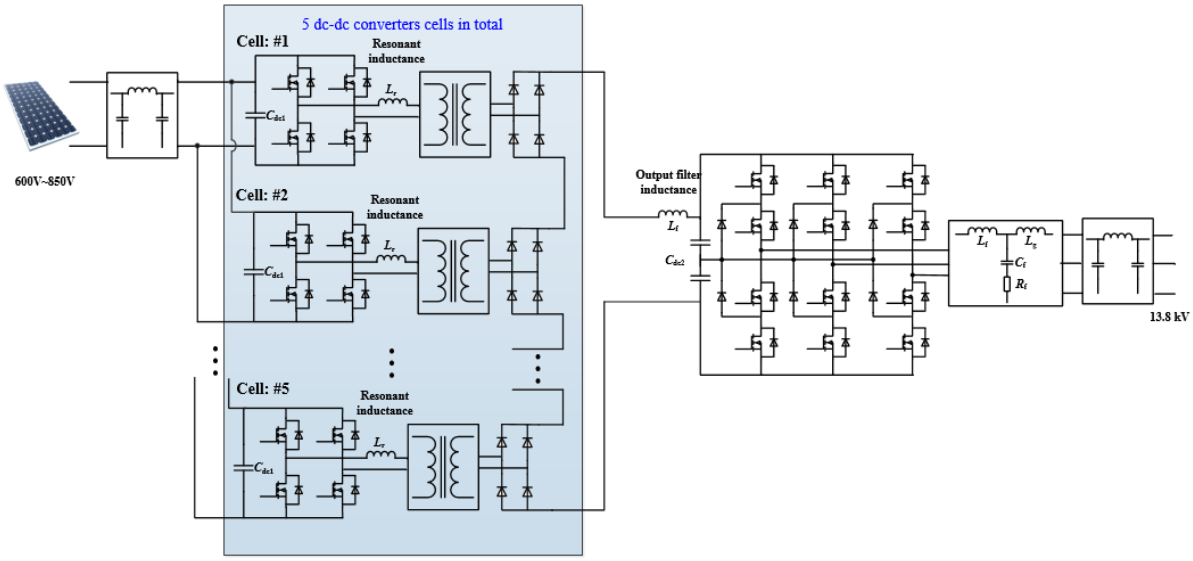



Fig. 4-5. The SiC-based PV converter.

#### 4.2.2.1 Main circuit

The main circuit of the SiC-based PV converter consists of a PSFB DC-DC converter and a three-level NPC DC-AC inverter, some parameters are shown in Table 4-7.

The PSFB DC-DC converter steps up the voltage from 600~850 V DC (output voltage of PV cells) to 21 kV DC (input voltage of next stage). On the low voltage side, five SiC MOSFET-based full bridges are in parallel connection. The 1.7 kV/1 kA SiC MOSFETs are used for the LV side converters. Due to the low power loss of SiC devices, a switching frequency of 10 kHz is selected. The DC-link capacitance decreases dramatically because of the increase in the switching frequency. On the high voltage side, five SiC diode-based full bridges are in series connection to achieve the required DC-link voltage. The 10 kV/114 A diode is adopted. Output filter inductance is selected as 42 mH. The low voltage side and high voltage side are connected to a 10 kHz high-frequency transformer. The transformer will be designed in the following section.

The DC-AC inverter transfers the 21 kV DC input into 13.8 kV AC output. The three-level NPC topology and the 15 kV/166 A MOSFET and diode are selected. The switching frequency is still 10 kHz. The DC-link capacitance is 28 μF based on the same criteria as in the Si case. Continuous space vector PWM (SVPWM) is used as a modulation method considering the need for neutral point voltage control.

Table 4-7. Main circuit design

| PSFB | | Three-level NPC | |
|---|---|---|---|
| **Parameters** | **Value** | **Parameters** | **Value** |
| **DC-link voltage** | 600~850 V(LV)/36.8 kV (HV) | **DC-link voltage** | 21 kV |
| **DC-link capacitance** | 15 mF (LV) | **DC-link capacitance** | 28 μF |
| **Peak current** | 508 A (LV)/57 A (HV) | **Peak current** | 83 A |
| **Switching frequency** | 10 kHz | **Switching frequency** | 10 kHz |
| **SiC devices** | 1.7 kV/1 kA MOSFET<br>10 kV/114 A diode | **SiC devices** | 15 kV/166 A MOSFET, diode |
| **Output inductance** | 42 mH | **Modulation** | SVPWM |
| **Control strategy** | Phase shift full bridge | | |
| **Dead time** | 213 ns | | |

Based on the main circuit parameters, the power loss can be calculated by simulation both for the PSFB DC-DC converter and three-level NPC at 25°C and 125°C junction temperatures. The output characteristics and switching loss of LV devices are from the datasheet of commercial SiC MOSFET (CAS300M17BM2) while those of HV devices are from the demo chips of 3rd generation MOSFET and diodes (See Chapter 2). The 125°C maximum allowed junction temperature is still selected in the SiC-based converter and the power loss @125°C is used to design the heatsink. The cooling system and operation conditions are the same as in the Si-based case. The total weight of the heatsink in the SiC-based PV converter is 84.5 kg (the sum of the PSFB and three-level NPC). The power loss calculation and heatsink design parameters are listed in Table 4-8. The total weight and size of the overall power electronics devices are 16.4 kg and 0.02 $m^3$.

Table 4-8. Power loss calculation and heatsink design

| **Power loss calculation** | | | |
|---|---|---|---|
| **PSFB** | | **Three-level NPC** | |
| **MOSFET conduction** | 871W@25°C/<br>1.33kW@125°C | **MOSFET 1 conduction** | 80W@25°C/147W@125°C |
| | | **MOSFET1 switching** | 730W@25°C/703W@125°C |
| **MOSFET Switching** | 380W@25°C/466 W@125°C | **MOSFET 2 conduction** | 106W@25°C/195W@125°C |
| **Diode conduction** | 258W@25°C/527 W@125°C | **MOSFET 2 switching** | 4W@25°C/4W@125°C |
| | | **Clamping diode conduction** | 11W@25°C/31W@125°C |
| **Total loss** | 6.0kW@25°C/9.3kW@125°C | **Total loss** | 5.6kW@25°C/6.5kW@125°C |
| **Heatsink design** | | | |

| | | |
|---|---|---|
| **Cooling** | Forced air | |
| **Rj-c** | 2.9 K/kW | 6.4 K/kW |
| **Air-flow** | 4.3 m/s | |
| **Rc-a** | 7 K/kW | 10 K/kW |
| **Material** | 6063-T5 Aluminum Extrusion Alloy | |
| **Weight** | 50 kg | 34.5 kg |
| **Size** | 0.04 $m^3$ | 0.03 $m^3$ |

#### 4.2.2.2 LCL filter

The LCL filter is designed per THD requirement (THD<3%). The electrical parameters are listed in Table 4-9. The simulation result in Fig.4-6 shows that THD satisfies the requirement (THD=0.98%<3%). Based on the electrical parameters and current rating, the physical design is done using silicon steel. The physical parameters are listed in Table 4-9. The total weight of the LCL filter is 356 kg and the total loss is 483 W.

The output filter inductor in the PSFB is also designed with a silicon steel core. The weight is 64 kg and the power loss is 340 W.

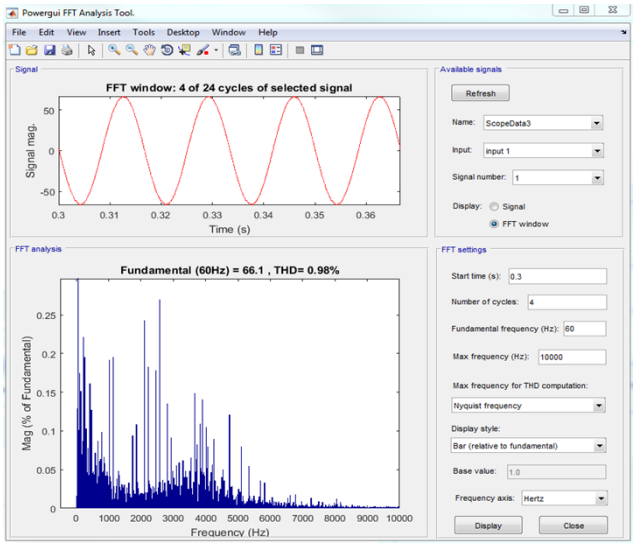



Fig. 4-6. THD simulation.

Table 4-9. LCL filter design

| | |
|---|---|
| **Electrical parameters** | |
| **Inverter-side inductor** | 15.6 mH (0.0309 p.u.) |
| **Grid-side inductor** | 11.7 mH (0.0232 p.u.) |
| **Filter capacitor** | 190 nF (0.0148 p.u.) |
| **Damping resistor** | 50 Ω (1/3 of $Z_{Cf}$ at the resonance frequency) |
| **Resonance frequency** | 4.3 kHz (43% of the switching frequency 10 kHz) |
| **Physical parameters** | |
| **Material** | Silicon steel |

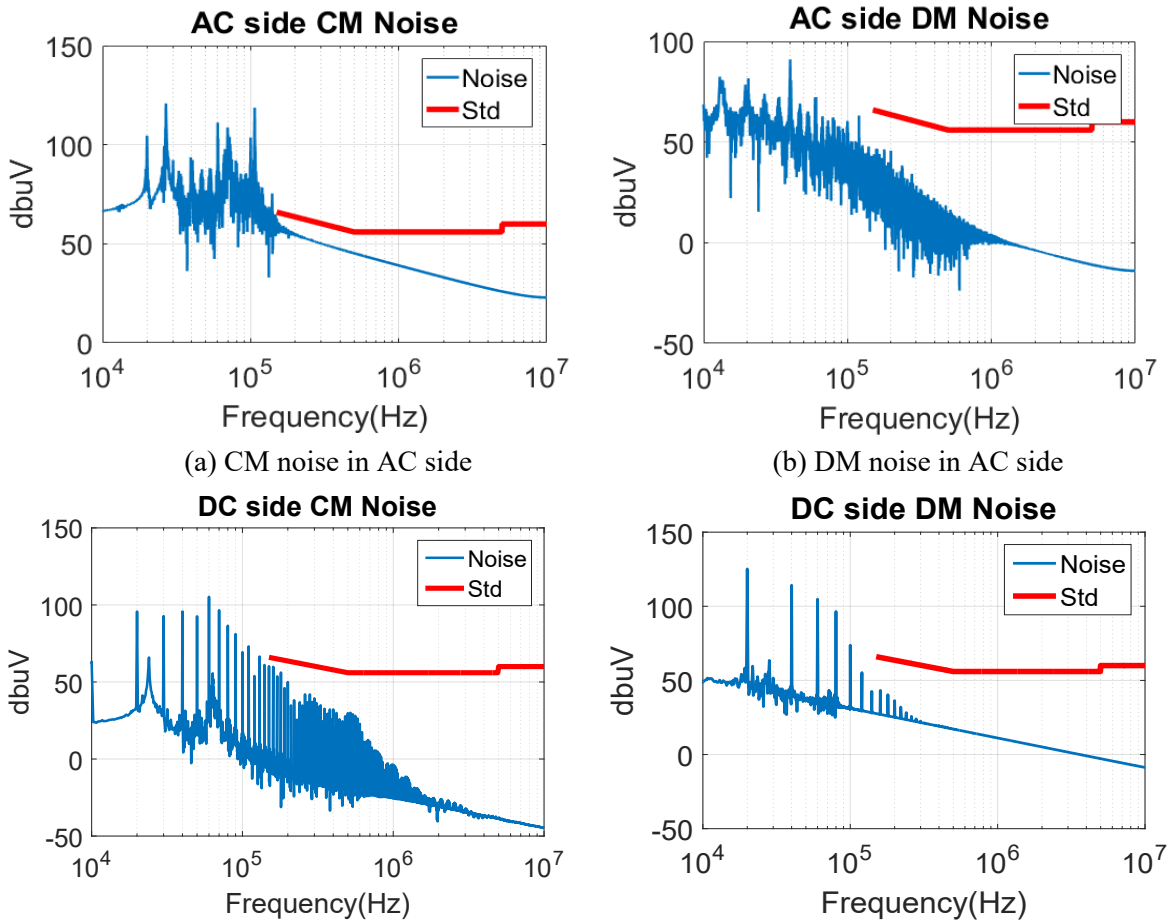
| | |
|---|---|
| **Copper weight** | 16.6 kg(15.6 mH)/12.7 kg(11.7 mH) |
| **Coil weight** | 131 kg(15.6 mH)/97 kg(11.7 mH) |
| **Accessories** | 57 kg(15.6 mH)/42 kg(11.7 mH) |
| **Total weight** | 204 kg(15.6 mH)/152 kg(11.7 mH) |
| **Power loss** | 271 W(15.6mH)/212 W(11.7mH) |
| **Size** | 0.2 $m^3$(15.6 mH)/0.14 $m^3$(11.7 mH) |

#### 4.2.2.3 EMI filter

The EMI filter is designed to satisfy FCC 15 CLASS B standard. The EMI filters are both required on AC and DC sides with both of them adopting CLCL topology. The simulation result in Fig.4-7 shows CM and DM noises are below the limit. Based on the electrical parameters and current rating, the physical design is done using FT-3M. The electrical and physical parameters are listed in Table 4-10. The total weight of the EMI filter is 16.3 kg and the total loss is 39 W.

Table 4-10. EMI filter design

| | | |
|---|---|---|
| **Electrical parameters** | | |
| EMI filter in AC side (CLCL filter) | $L_{cmac}$ | 2 mH |
| | $C_{cmac}$ | 2 nF |
| EMI filter in DC side (CLCL filter) | $L_{cmdc}$ | 317 μH |
| | $C_{cmdc}$ | 25 nF |
| **Physical parameters** | | |
| **Material** | | FT-3M |
| **Copper weight** | | 8.6 kg(317 μH)/0.236 kg(2 mH) |
| **Coil weight** | | 2.6 kg(317 μH)/0.335 kg(2 mH) |
| **Accessories** | | 4.3 kg(317 μH)/0.22 kg(2 mH) |
| **Total weight** | | 15.5 kg(317 μH)/0.791 kg(2 mH) |
| **Power loss** | | 28 W(317 μH)/11 W(2 mH) |
| **Size** | | 0.015 $m^3$(317 μH)/0.002 $m^3$(2 mH) |




(a) CM noise in AC side

(b) DM noise in AC side

(c) CM noise in DC side

(d) DM noise in DC side

Fig. 4-7. CM and DM noise simulation.

#### 4.2.2.4 High-frequency transformer

The PSFB uses five 10 kHz high-frequency transformers in series connection. For each one, the capacity is 240 kVA, and the ratio is 1:9. The FT-3M is selected as the material. The design results are shown in Table 4-11. The weight is 345 kg, and the loss is 3.3 kW.

Table 4-11. High-frequency transformer design

| **Electrical parameters** | |
|---|---|
| **Capacity** | 5×240 kVA |
| **Ratio** | 1:9 |
| **Frequency** | 10 kHz |
| **Leak inductance** | 0.5 μH |
| **Physical parameters** | |
| **Material** | FT-3M |
| **Weight** | 5×69 kg |
| **Power loss** | 3.3 kW |
| **Size** | 0.21 $m^3$ |

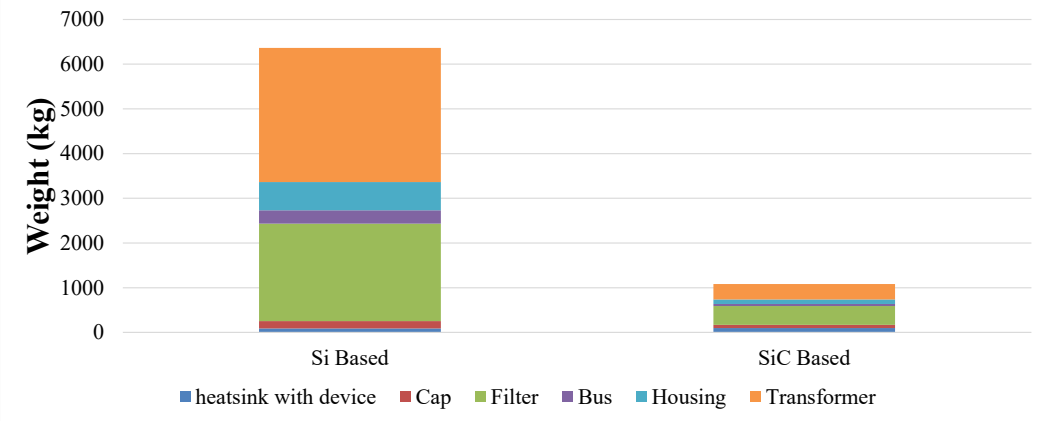
### 4.2.3 Comparison

Fig.4-8 displays the weight, size, and power loss comparison and the corresponding breakdown. The values are listed in Table 4-12. The power losses of Si-based and SiC-based converters are nearly the same (15.7 kW in SiC-based and 16.2 kW in Si-based) per efficiency requirement. But the weight and size of the SiC-based PV converter are reduced by 82.9% and 73.2% compared to the Si-based converter. Most of the savings come from the transformer and the filter inductors. Consequently, the power density of SiC-based converter is 3.75 times that of Si-based converter (0.81 MW/m$^3$ for SiC-based and 0.216 MW/m$^3$ for Si-based) and the specific power of SiC-based converter is 5.87 times that of Si-based converter (1.11 MW/ton for SiC-based and 0.189 MW/ton for Si-based).

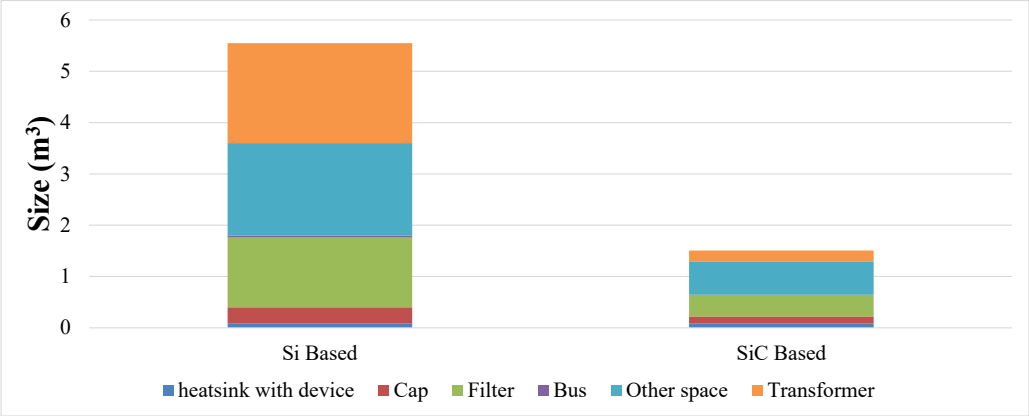
Based on the preliminary design, it can be concluded that: 1) the improvement of SiC-based PV converter is significant (82.9% weight reduction and 73.2% size reduction); 2) with the same efficiency, the switching frequency of SiC-based PV converter can be much higher (triple that of Si-based PV converter). It can lead to many system-level benefits, which will be discussed in the next section.

Table 4-12. Comparison of Si-based and SiC-based PV converter

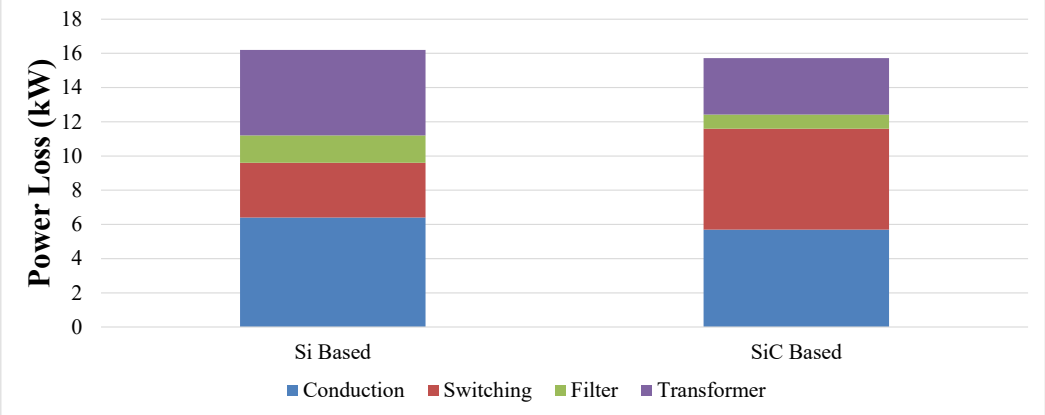
| | Si-based converter | | | SiC-based converter | | |
|---|---|---|---|---|---|---|
| | **Weight** | **Loss** | **Size** | **Weight** | **Loss** | **Size** |
| **Active device with heat sink** | 91 kg | 9.6 kW | 0.08 m$^3$ | 98 kg | 11.6 kW | 0.08 m$^3$ |
| **Transformer** | 3,000 kg | 5 kW | 1.95 m$^3$ | 345 kg | 3.3 kW | 0.21 m$^3$ |
| **Filter inductors** | 2,176 kg | 1.6 kW | 1.36 m$^3$ | 420 kg | 823 W | 0.42 m$^3$ |
| **Capacitor** | 165 kg | - | 0.32 m$^3$ | 72 kg | - | 0.14 m$^3$ |
| **Bus bar** | 301 kg | - | 0.04 m$^3$ | 46 kg | - | 0.01 m$^3$ |
| **Housing** | 629 kg | - | - | 103 kg | - | - |
| **Total** | 6,362 kg | 16.2 kW (98.4%) | 5.55 m$^3$ | 1,088 kg | 15.7 kW (98.4%) | 1.49 m$^3$ |




(a) Weight




(b) Size




(c) Power loss

Fig. 4-8. Comparison of Si based and SiC based PV converters.

## 4.3 SYSTEM LEVEL BENEFITS

Based on the results in Section 4.2, the switching frequency of the SiC-based DER converter is higher than Si-based (10 kHz in SiC-based and 3 kHz in Si-based). As a result, the SiC-based converter can have increased control bandwidth. The high control bandwidth brings benefits to the system level such as power quality improvement, system stability enhancement, and low voltage ride through (LVRT).

The configuration of the microgrid benchmarked in this section is shown in Fig.4-1. The microgrid contains 1 MW PV, 200 kW BESS, 200 kW combined heat and power (CHP), and 1 MW load (400 kW is a critical load while the remaining 600 kW is a non-critical load). During the normal operation, in both grid-connected and islanded modes, the loads are supplied by PV as much as possible, with the grid, CHP, and BESS making up the difference. CHP (and/or other backup generators) and BESS will help maintain the critical load even when PV and utility grid are unavailable. The PV and BESS are connected with the microgrid through Si or SiC-based interface converters. The comparison in power quality, system stability, and LVRT with Si and SiC-based interface converters will be carried out in this section based on simulation results, to investigate the system benefits of SiC-based interface converters.

### 4.3.1 Power Quality Improvement

The growing use of electronic equipment can result in significant harmonics in the power distribution systems because of non-sinusoidal currents consumed by non-linear loads. Some of the examples for non-linear loads are diode- or thyristor-rectifiers used for heating-ventilation-air conditioning (HVAC) and adjustable speed drives, furnaces, computer/data center power supplies, uninterruptible power supplies, etc. Even though these devices are economical, flexible, and energy-efficient, they may degrade power quality by generating harmonic currents and voltages.

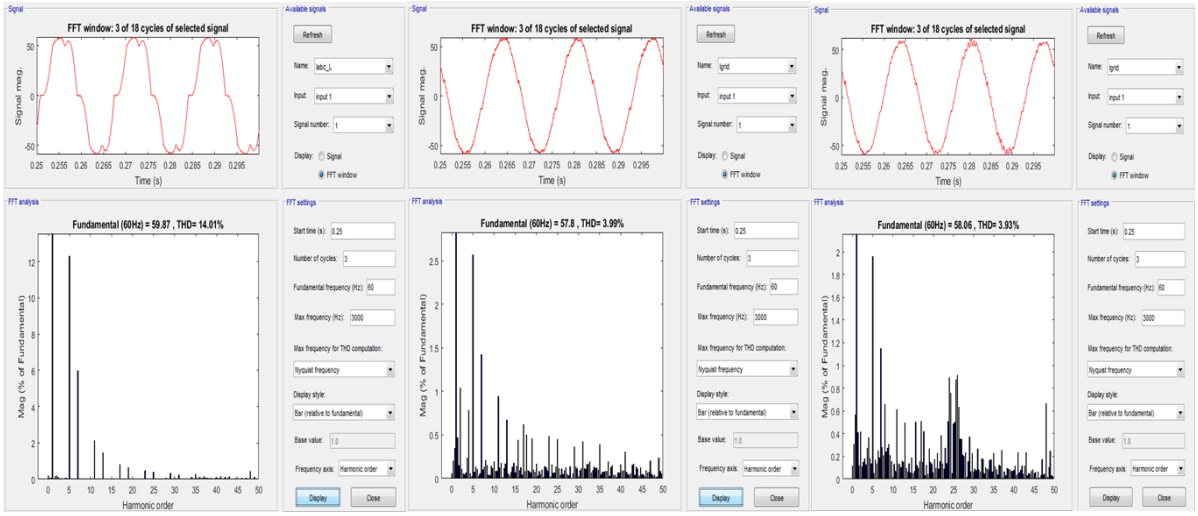
Harmonic distortion in power distribution systems can be suppressed using two approaches, namely, passive and active power filtering. Passive filters using inductors and capacitors have drawbacks such as bulky size, the possibility of resonance, and fixed inflexible compensation. Since SiC-based converter can provide an active filtering function, only active filtering is studied here. Two active solutions are compared: Si-based solution, and SiC-based solution.

For the Si-based solution, a dedicated Si-based active power filter (APF) with a high switching frequency is needed; for the SiC-based solution, thanks to the high switching frequency capability and corresponding high control bandwidth of SiC-based converters, the filtering function can be integrated into the DER interface converters themselves, and therefore no additional APF is required. The setup for comparing the two solutions is listed in Table 4-13. In this case, the SiC-based PV interface converter is used for harmonics compensation. The target is to maintain the Total Demand Distortion (TDD) of the PCC on the grid side below 5%. The base current is selected as 41.8 A rms corresponding to $P_{base}$ = 1 MW and $V_{base}$ = 13.8 kV. The two solutions are compared in terms of the total converter power rating requirement.

Table 4-13. Solutions of harmonics compensation

| | **Solution 1: Si-based** | **Solution 2: SiC-based** |
|---|---|---|
| **Converter type** | Si-based (BESS, PV, APF) | SiC-based (BESS, PV) |
| **Switching frequency** | 3 kHz (BESS, PV)<br>10 kHz (APF) | 10 kHz (BESS, PV) |
| **Current control bandwidth** | 600 Hz (BESS, PV)<br>2 kHz (APF) | 2 kHz (BESS, PV) |
| **Load** | six-pulse uncontrolled rectifier | six-pulse uncontrolled rectifier |

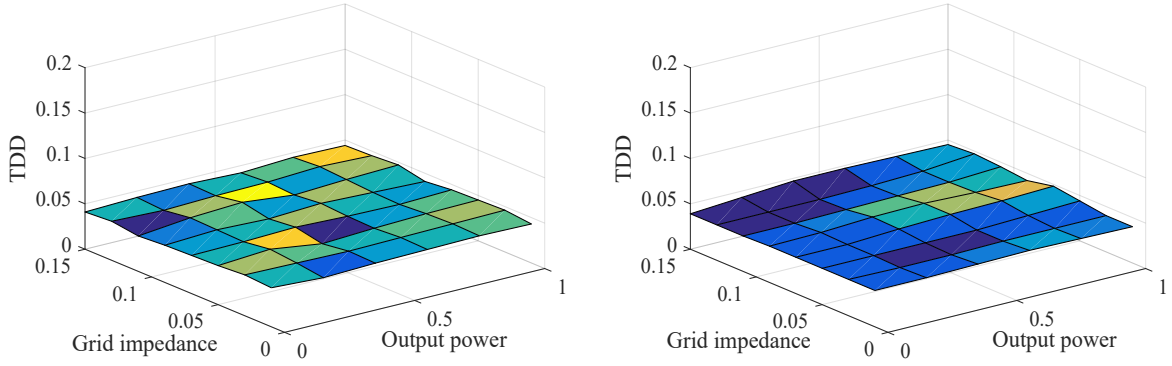
The TDD simulation results (grid impedance is 0.05 p.u. and the output power of PV is zero) are shown in Fig.4-9. Without harmonics compensation, 14% harmonic current, which is from the non-linear six-pulse uncontrolled rectifier load, is injected into the grid. TDD becomes less than 5% both with Si-based and SiC-based solutions.




(a) without harmonic compensation (b) Si-based solution (c) SiC-based solution

Fig. 4-9. TDD simulation.

The TDD varies with grid impedance and output power of the PV. The simulation results of TDD are shown in Fig.4-10. TDD is lower than 5% when grid impedance varies from 0.01p.u. to 0.15p.u. and PV output power varies from 0 to 1 MW. Fig.4-11 shows the relationship between grid impedance and rating current. For the Si-based solution, the total apparent current rating (corresponding to the KVA rating) equals the sum of the PV output current and the APF output current. In the SiC-based solution, the total apparent current rating is the PV output current itself.




(a) Si based solution (b) SiC based solution

Fig. 4-10. TDD variation with output power and grid impedance.

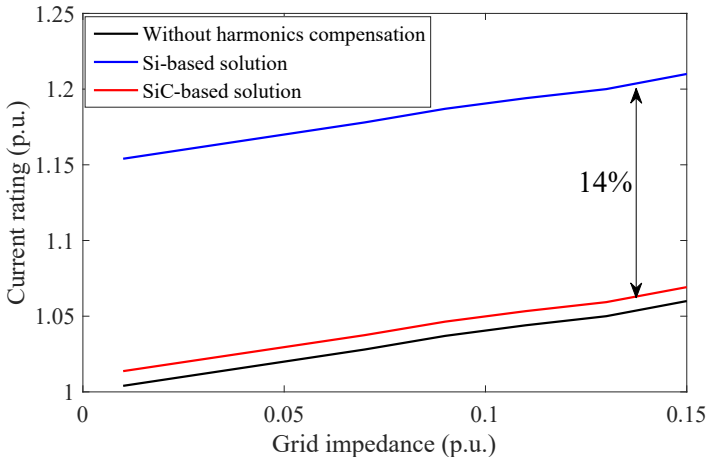


Fig. 4-11. Apparent current rating (corresponding to kVA rating) comparison.

It can be concluded that in Si-based solution, it needs an extra 150 kVA (15% more) converter for Si-based APF while the impact on SiC-based converter rating is minimal (~1%). By eliminating the dedicated active filters, the SiC-based solution saves a 14% converter rating.

### 4.3.2 System Stability Enhancement

Multiple renewable energy and energy storage interface converters in microgrids, connected to relatively weak grids, can lead to harmonic resonance and stability issues. SiC-based converters, with their switching frequency and high control bandwidth, can help damp the resonance/oscillation and enhance stability.

To investigate the benefits of SiC-based DER interface converters on system stability, two cases are set up and compared, as listed in Table 4-14. In Case 1, Si-based converters are used in the BESS and the PV system, with a lower switching frequency (3 kHz) and a lower current control bandwidth (300 Hz) due to the limited switching capability of Si devices. In Case 2, SiC-based converters are adopted for the BESS and the PV, and a higher switching frequency (10 kHz) and a higher control bandwidth (1 kHz) can be achieved.

The impedance-based stability criteria are effective in analyzing the small-signal stability of systems consisting of power electronics converters. The interconnected system is stable if and only if the impedance ratio at the interconnection interface meets the Nyquist stability criterion. A conservative derivative of the Nyquist stability criterion is the passivity-based stability criterion, that is, the overall system stability is guaranteed if the impedance phase angle of each subsystem is between [−90°, 90°].

Table 4-14. Case setups for the system stability study

| | **Case 1** | **Case 2** |
|---|---|---|
| **Converter type** | Si-based (BESS, PV) | SiC-based (BESS, PV) |
| **Switching frequency** | 3 kHz (BESS, PV) | 10 kHz (BESS, PV) |
| **Current control bandwidth** | 300 Hz (BESS, PV) | 1 kHz (BESS, PV) |
| **Load** | 1 MW, 80% is active rectifier load, 20% is resistor, cap load | 1 MW, 80% is active rectifier load, 20% is resistor, cap load |

For three-phase converters with LCL filters and grid-side current control, the non-passive frequency range, where the phase angle of the converter output admittance is outside of [−90°, 90°], is between the resonance frequency $\omega_r$ of the converter-side inductor $L_f$ and the filter capacitor $C_f$ as expressed in (4-1), and the critical frequency $\omega_d$ determined by the delay time $T_d$ in the converter control loop as expressed in

(4-2), where $T_d$ is 1.5 switching period ($T_s$). According to the passivity-based stability criterion, the negative conductance of converters could trigger unstable resonances in the system.

$$\omega_r = \frac{1}{\sqrt{L_f C_f}} \tag{4-1}$$

$$\omega_d = \frac{\pi}{2T_d} = \frac{\pi}{3T_s} \tag{4-2}$$

For the Si-based converter designed in the previous sections, the non-passive range is [$\omega_{d1}$, $\omega_{r1}$], where $\omega_{d1}$=500×2π rad/s and $\omega_{r1}$=886×2π rad/s. And for the SiC-based converter designed above, the non-passive range is [$\omega_{d2}$, $\omega_{r2}$], where $\omega_{d2}$=1667×2π rad/s and $\omega_{r2}$=3207×2π rad/s. Fig.4-12 shows the Bode plots of the current open-loop gains of the Si-based converter and the SiC-based converter with control bandwidths of $\omega_{c1}$=300×2π rad/s and $\omega_{c2}$=1000×2π rad/s, respectively. Fig.4-13 illustrates the Bode plots of output admittances of both converters, where the non-passive ranges can be clearly observed.

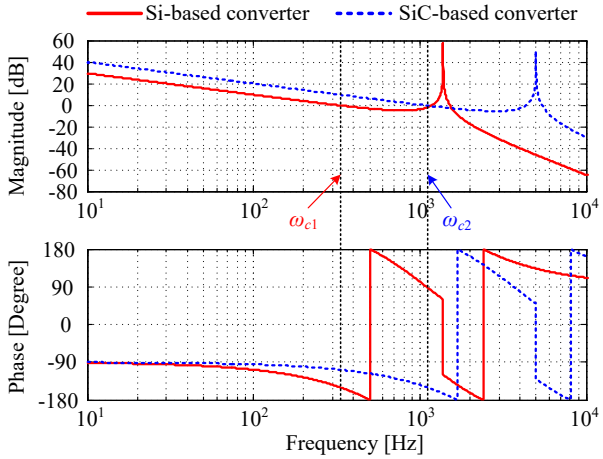



Fig. 4-12. Bode plots of the current open-loop gains of the Si-based converter and the SiC-based converter.

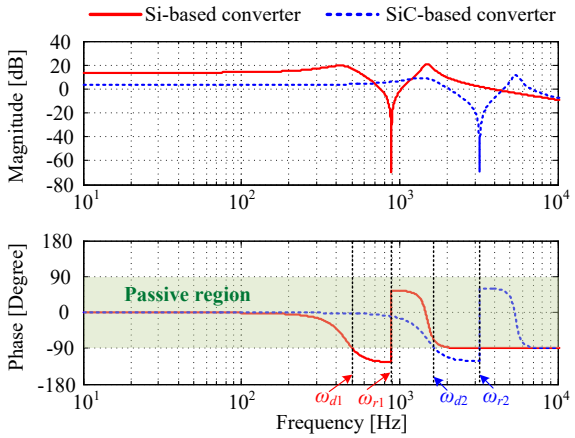


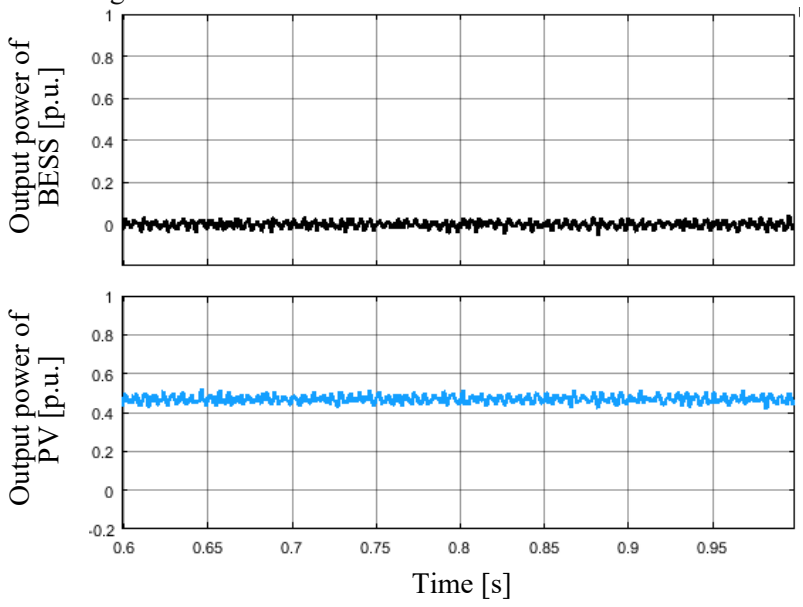

Fig. 4-13. Bode plots of the output admittances of the Si-based converter and the SiC-based converter.

When connecting the DER interface converters to a weak grid, a potential resonance circuit is formed by the large grid inductor $L_s$ and parasitic capacitors along the cable or the Power Factor Correction (PFC) capacitors installed at the PCC, denoted as $C_p$, and the potential resonance frequency $\omega_{rg}$ is expressed in (4-3). For a weaker grid with a larger grid inductance $L_s$, the resonance frequency $\omega_{rg}$ is lower.

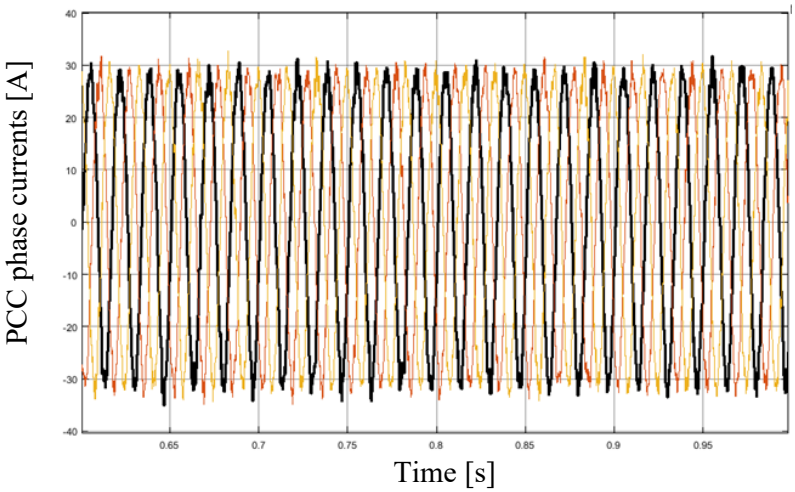
$$\omega_{rg} = \frac{1}{\sqrt{L_s C_p}} \tag{4-3}$$

Thanks to the advantage of a higher switching frequency and a smaller time delay in the control loop, the SiC-based converter possesses a non-passive range in the higher frequency range, compared with that of the Si-based converter. Therefore, when connecting to a weak grid, the SiC-based converter has a smaller destabilization effect on the system stability, compared with the Si-based converter. In other words, weak grids with SiC-based converters have better stability than those with Si-based converters.

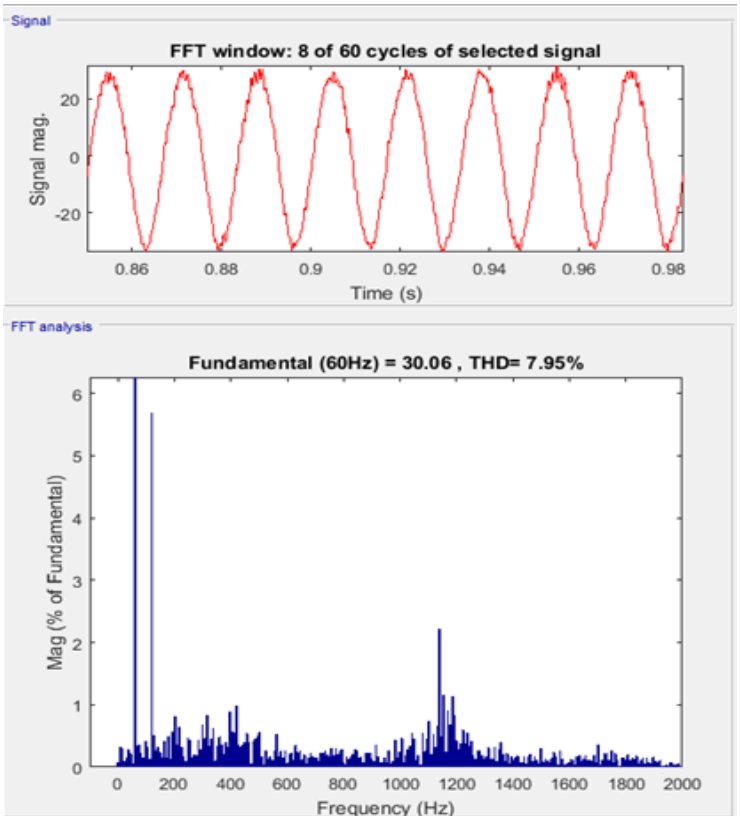
Several simulations are carried out in MATLAB/Simulink to verify the benefit of system stability enhancement brought by the SiC-based converters. In the following simulations, two grid conditions are considered: a strong grid with an impedance of 0.05 p.u., and a weak grid with an impedance of 0.1 p.u.. The shunt grid capacitor is assumed as 0.044 p.u.. For Case 1 with Si-based DER interface converters, Fig.4-14(a) shows the power outputs of the BESS and the PV, Fig.4-14(b) shows the current waveforms at the PCC, and Fig.4-14(c) depicts the FFT analysis results of the PCC current, when the grid impedance is 0.05 p.u., while Fig.4-15 illustrates the corresponding simulation results when the grid impedance is 0.1 p.u.. It can be seen that the integration of Si-based converters to a strong grid is stable but the integration to a weak grid is unstable with unstable resonances of about 1000 Hz. On the other hand, for Case 2 with SiC-based DER interface converters, both the integration to a strong grid as shown in Fig.4-16 and the integration to a weak grid as shown in Fig.4-17 are stable. It is demonstrated that the high switching frequency and high control bandwidth enabled by SiC-based DER interface converters can enhance the system stability under weak grid condition.




(a) Active power outputs of the BESS and PV

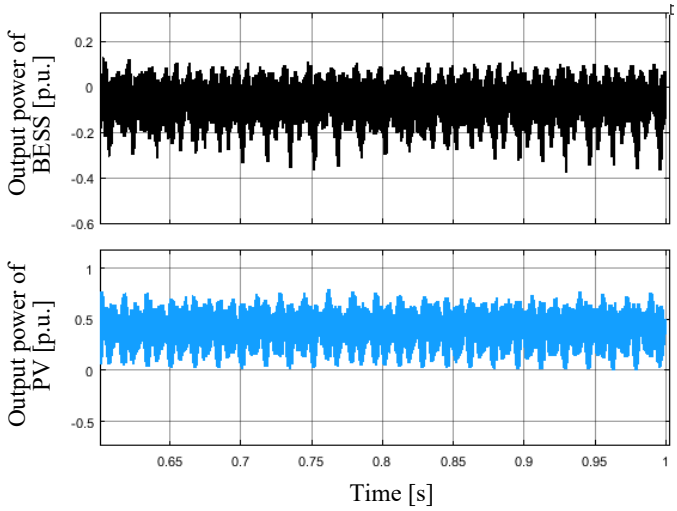



(b) PCC phase current

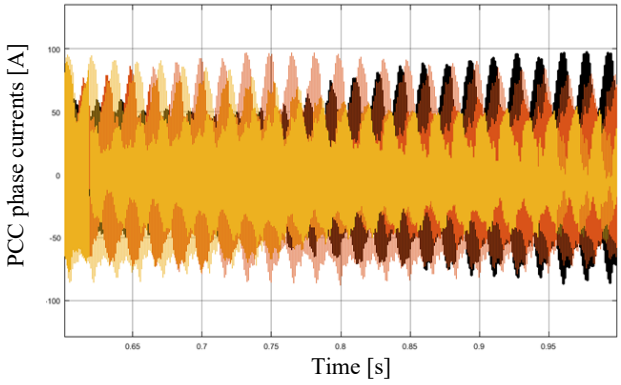



(c) FFT analysis of PCC phase current

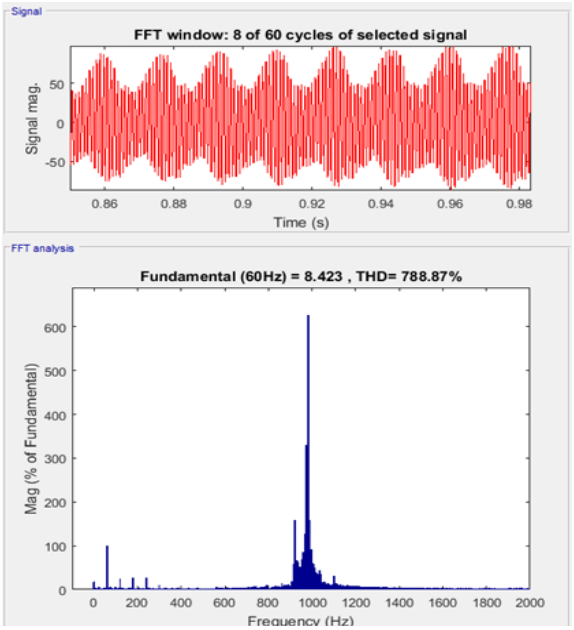
Fig. 4-14. Simulation results of Case 1 when the grid impedance is 0.05 p.u..




(a) Active power outputs of the BESS and PV

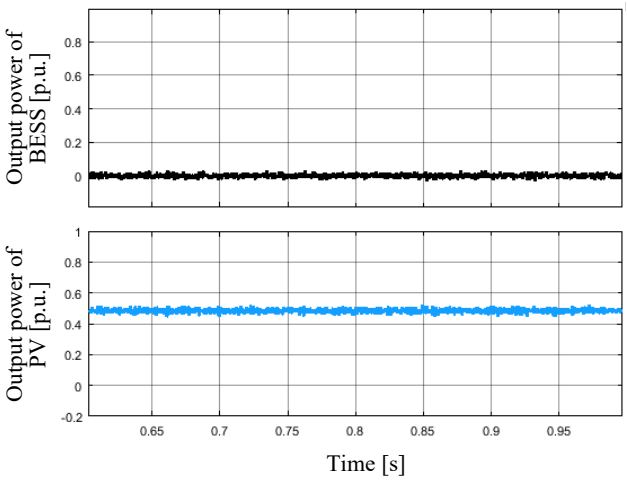



(b) PCC phase current

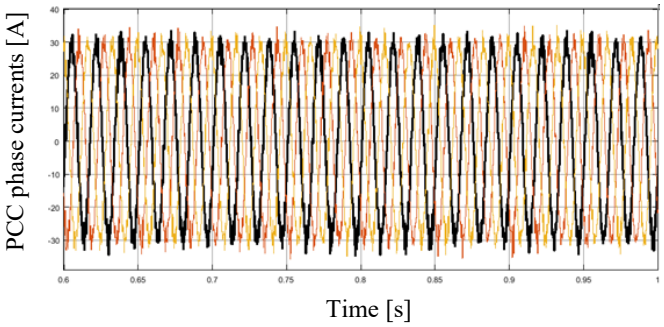



(c) FFT analysis of PCC phase current

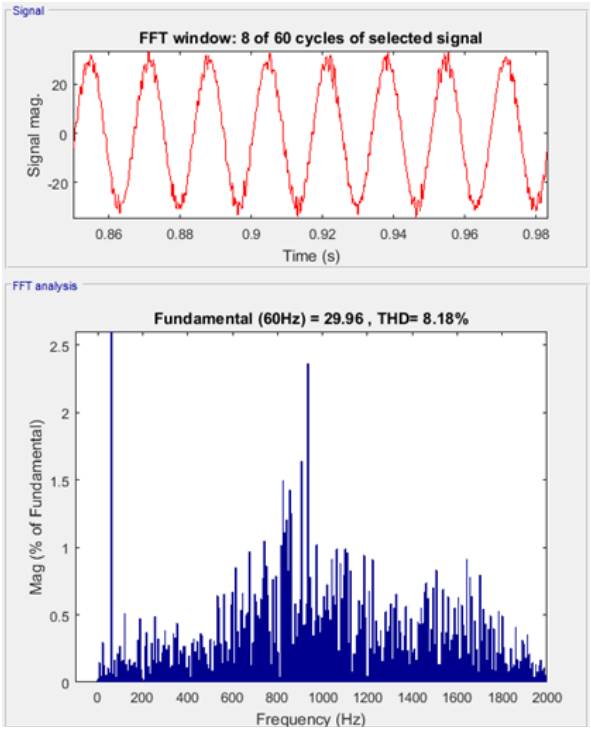
Fig. 4-15. Simulation results of Case 1 when the grid impedance is 0.1 p.u..




(a) Active power outputs of the BESS and PV

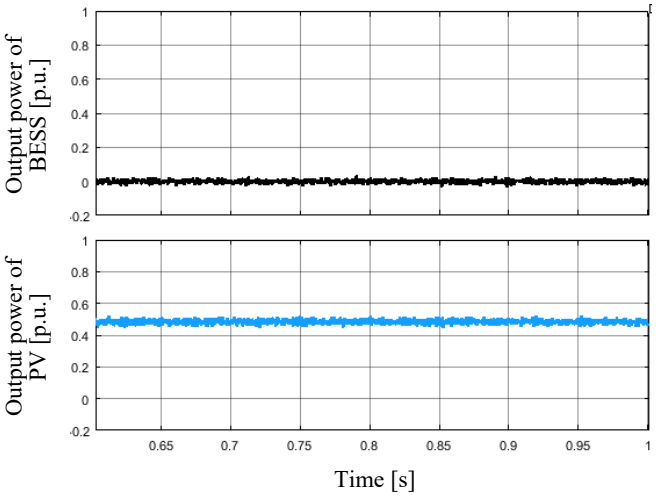



(b) PCC phase current

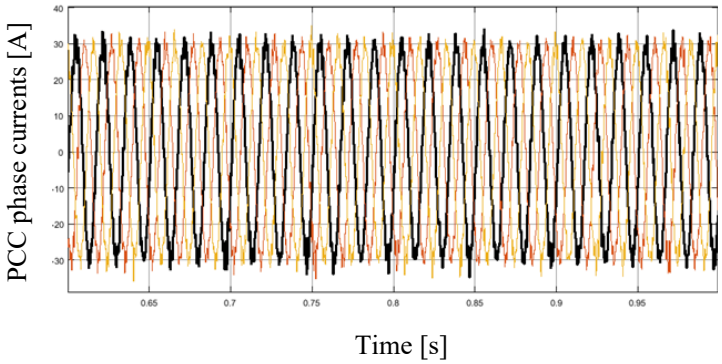



(c) FFT analysis of PCC phase current

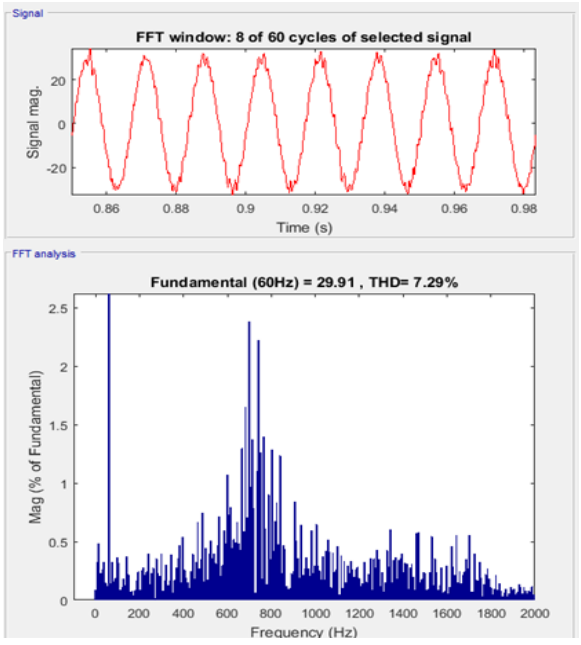
Fig. 4-16. Simulation results of Case 2 when the grid impedance is 0.05 p.u..




(a) Active power outputs of the BESS and PV




(b) PCC phase current




(c) FFT analysis of PCC phase current

Fig. 4-17. Simulation results of Case 2 when the grid impedance is 0.1 p.u..

### 4.3.3 Low Voltage Ride Through

In electric power systems, low-voltage ride through (LVRT) is the capability of electric generators to stay connected in short periods of lower electric network voltage. It is needed at the distribution level (wind farms, PV systems, BESS systems, distributed cogeneration, etc.) to avoid that a short circuit fault leads to a widespread loss of generation.

The detailed requirement for the performance of LVRT for DER is given in IEEE Std 1547-2014, as shown in Fig.4-18. In the microgrid, the PV and BESS should stay connected during the clearing time when PCC voltage drops to the corresponding values. And during the LVRT period, the interface converter of PV and BESS should protect the system from overcurrent and supply reactive power to support the grid as well.

**Table 1—Interconnection system default response to abnormal voltages**

| Default settings[a] | | |
|---|---|---|
| **Voltage range (% of base voltage[b])** | **Clearing time (s)** | **Clearing time: adjustable up to and including (s)** |
| V < 45 | 0.16 | 0.16 |
| 45 ≤ V < 60 | 1 | 11 |
| 60 ≤ V < 88 | 2 | 21 |
| 110 < V < 120 | 1 | 13 |
| V ≥ 120 | 0.16 | 0.16 |

[a] Under mutual agreement between the EPS and DR operators, other static or dynamic voltage and clearing time trip settings shall be permitted

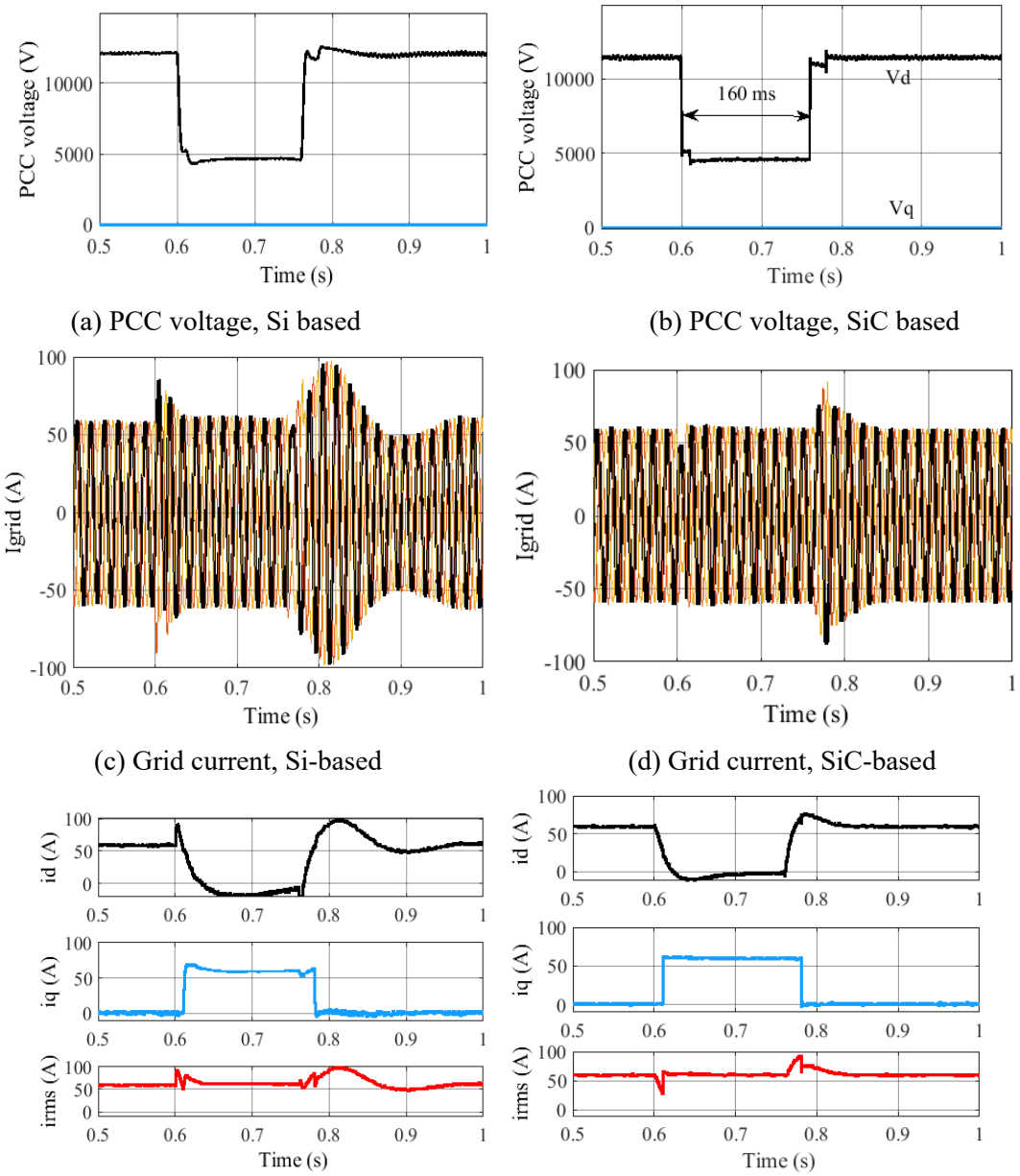
[b] Base voltages are the nominal system voltages stated in ANSI C84.1-2011, Table 1.

Fig. 4-18. LVRT requirement in IEEE Std 1547-2014.

The Si- and SiC-based setup for LVRT simulation is listed in Table 4-15. The simulation results are shown in Fig.4-19. The operation steps during the LVRT period are as follows: 1) PV system supplies rated active power and zero reactive power ($I_d$=1 p.u., $I_q$=0) until the PCC voltage drop occurs (0.6 s); 2) The PCC voltage drop (45% of base voltage) is detected. PV system and BESS system begin to supply zero active power and rated reactive power ($I_d$=0, $I_q$=1 p.u.); 3) After 160 ms, the PCC voltage returns to the rated voltage. PV and BESS system recover to normal operation. The LVRT can be achieved with either a Si-based interface converter or a SiC-based one. But due to the higher control bandwidth, the dynamic performance with the SiC-based converter is better (lower grid and converter peak current and shorter response time).

Table 4-15. Simulation Condition Setup of LVRT

| | **Case 1: Si-based** | **Case 2: SiC-based** |
|---|---|---|
| **Converter type** | Si-based (BESS, PV) | SiC-based (BESS, PV) |
| **Switching frequency** | 3 kHz (BESS, PV) | 10 kHz (BESS, PV) |
| **Current control bandwidth** | 300 Hz (BESS, PV) | 1 kHz (BESS, PV) |
| **Load** | 80% active rectifier, 20% resistive | 80% active rectifier, 20% resistive |




(a) PCC voltage, Si based

(b) PCC voltage, SiC based

(c) Grid current, Si-based

(d) Grid current, SiC-based

(e) DQ transformation of grid current, Si-based

(f) DQ transformation of grid current, SiC-based

Fig. 4-19. LVRT simulation.

## 4.4 CONCLUSION

The benefits of using HV SiC in DER converters in a conventional MV AC microgrid are benchmarked both at the converter level and the system level. At the converter level, the SiC-based DER converter will have significant weight and size advantages compared with the Si counterpart, e.g. an 82.9% weight reduction and 73.2% size reduction can be achieved for a 1 MW, 13.8 kV PV interface converter using HV SiC devices. The SiC-based DER converters can work with a higher switching frequency (e.g. 3 times that of Si-based), and therefore have a higher control bandwidth. At the system level, the high control bandwidth results in power quality improvement (e.g. saving the need for a dedicated APF which can be 14% of the total converter rating in the example study), system stability enhancement (keeping stability even in weak grid conditions) and better LVRT dynamic performance.

# 5. BENCHMARK OF HV SIC BENEFITS IN ASYNCHRONOUS MICROGRIDS

## 5.1 INTRODUCTION

An asynchronous microgrid connects to an AC distribution grid through a microgrid power conditioning system (PCS). As shown in Fig. 5-1, the microgrid PCS can be made up of two back-to-back AC/DC converters, similar to back-to-back high voltage DC (HVDC) converters in connecting two asynchronous AC transmission grids. Compared with a conventional AC synchronous microgrid benchmarked in the last chapter, the asynchronous microgrid has decoupled dynamics with the distribution grid. Consequently, it can result in numerous system-level benefits: a) easier integration of renewable energy sources (RES) into microgrids without the need to consider RES and distribution grid interactions; b) better low-voltage/frequency ride-through capability; c) easier transition between grid-connected and islanded modes and elimination of the need for resynchronization control; d) isolation of unbalance and faults, for easier microgrid protection coordination and control. Furthermore, the PCS converters can provide independent var support to micro- and macro-grids, and even allow integration of energy storage and other distributed energy resources on the DC link.

On the other hand, the microgrid PCS can add cost, size, and power loss to the system, especially given that today's PCS is based on lossy and slow Si technology. As a result, there are very few real applications for asynchronous AC microgrids. With the introduction of SiC devices, esp. HV SiC devices that will potentially enable more efficient MV microgrid PCS converters, the MV asynchronous microgrids as shown in Fig. 5-1 may be enabled. This could become a "killer" application for HV SiC devices in distribution grids.

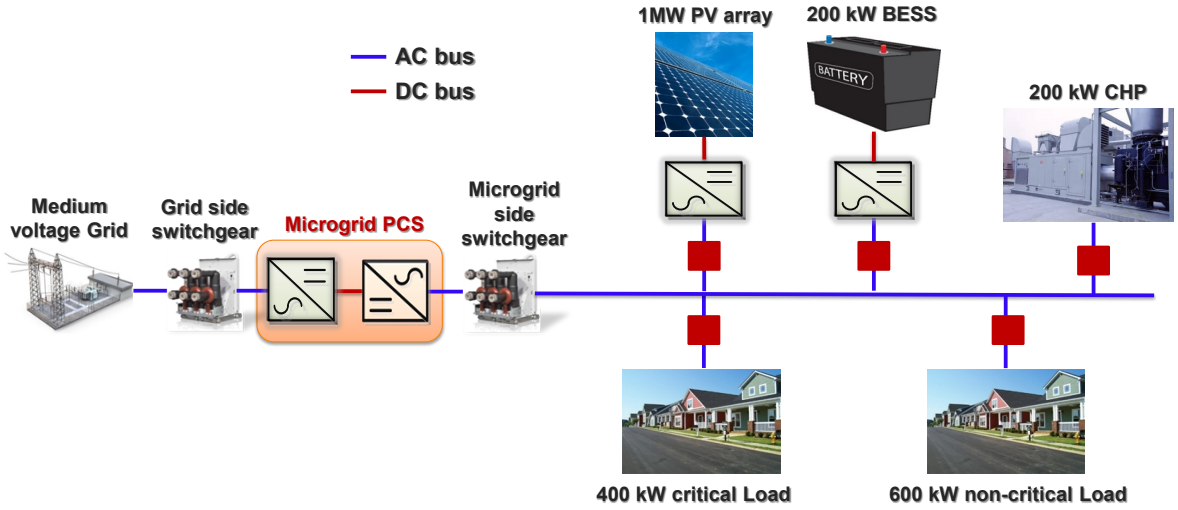



Fig.5-1. Configuration of MV asynchronous microgrid.

The main objective of this chapter is to assess the potential benefits of HV SiC device-based PCS converters both at the converter level and system level. For converter level assessment, 13.8 kV transformer-less HV SiC converters using both three-level NPC and MMC topologies are designed and compared with a 3.3 kV Si three-level NPC converter with a low-frequency transformer. At the system level, the benefits are analyzed both in grid-connected mode and islanded mode. Specifically, the enhanced performances on power quality, system stability, LVRT, transition, and black start as a result of HV SiC microgrid PCS converters are assessed using simulation.

## 5.2 CONVERTER LEVEL BENEFITS

The microgrid PCS converter connects an asynchronous microgrid with a distribution main grid. As shown in Fig. 5-1, it is a back-to-back converter with two stages: an AC-DC rectifier and a DC-AC inverter. In this section, the PCS will be designed based on HV SiC devices, as well as Si devices. The specifications of the PCS are listed in Table 5-1. The power rating of the PCS is selected as 1 MW.

Table 5-1. Specifications of the MG PCS

| Parameters | Specs | Parameters | Specs |
|---|---|---|---|
| **Power rating** | 1 MW | **Nominal AC voltage** | 13.8 kV (±10%) |
| **Nominal AC current** | 46.5 A | **THD** | < 5% |
| **Efficiency** | > 98% | **Power factor** | ±0.9 |
| **Grid function** | LVRT, HVRT, LFRT, HFRT, islanded operation, reactive power compensation, active power filtering | | |
| **Ambient temp range** | -15ºC ~ 55ºC | **Cooling** | Forced air |

The Si-based design uses the combination of a 13.8 kV/3.3 kV step-down transformer, a back-to-back converter with 3.3 kV AC input and output, and a 3.3 kV/13.8 kV step-up transformer. The configuration is similar to a Pareto Energy solution. Three-level NPC topology with HV Si IGBT is used for the back-to-back converter.

The voltage rating of a SiC device can be higher than that of a Si device. Therefore, the transformer can be eliminated in SiC-based design. The three-level NPC converter with 15 kV SiC devices is employed here. An alternative configuration using the modular multilevel converter (MMC) topology with 10 kV SiC devices is also designed and compared. To have a more complete device and topology comparison, five groups of designs are selected, including Si device-based three-level NPC converter with transformer (Group 1); SiC device-based three-level NPC converter with a switching frequency of 10 kHz (Group 2A); SiC device-based three-level NPC converter with a switching frequency which will make the converter efficiency close to that of Si-based design (Group 2B); SiC device-based MMC with switching frequency of 10 kHz (Group 3A); and SiC device-based MMC with switching frequency which will make the converter efficiency close to that of Si-based design (Group 3B). The Si-based, SiC-based three-level NPC, and SiC-based MMC PCS will be designed in Sections 5.2.1, 5.2.2, and 5.2.3 respectively. The design of the five groups will be compared in Section 5.2.4. The comparison again focuses on power loss and efficiency, weight, and size.

### 5.2.1 Si-Based Microgrid PCS Design

The topology of the Si-based PCS consists of a three-level NPC back-to-back converter (3.3 kV AC input and output) and 13.8 kV / 3.3 kV low-frequency transformers, as shown in Fig.5-2.

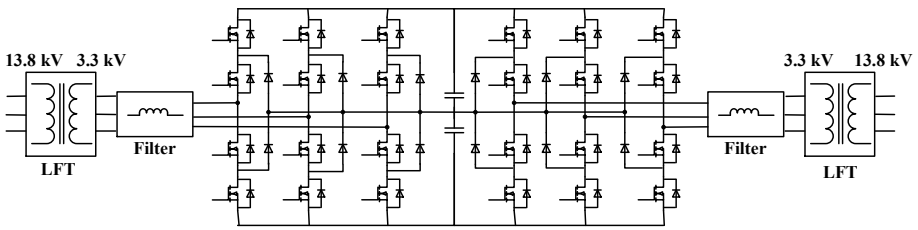



Fig.5-2. Si-based PCS.

#### 5.2.1.1 Main circuit

The main circuit is two three-level NPC converters with HV Si IGBT. The parameters are listed in Table 5-2. DC-link voltage is selected considering maximum modulation index, 10% of AC voltage variation, and 0.9 power factor. The power rating is 1.1 MVA due to the power factor requirement. The peak current reaches 305 A. Therefore, 4.5 kV/ 610 A IGBT is used here, and a switching frequency of 1.08 kHz is selected. DC-link capacitance is selected as 2.4 mF and SVPWM is applied. L filter is designed to make sure the THD is lower than 5%. The THD simulation with a 7.2 mH filter inductor is shown in Fig.5-3.

Table 5-2. Parameters of the main circuit

| Parameters | Value |
|---|---|
| **DC-link voltage** | 5.3 kV |
| **AC output voltage** | 3.3 kV |
| **Power rating** | 1.1 MVA (PF=0.9) |
| **Peak current** | 305 A |
| **Power electronics device** | 4.5 kV/610 A Si IGBT |
| **Switching frequency** | 1.08 kHz |
| **DC-link capacitor** | 2.4 mF |
| **Modulation** | SVPWM |
| **L filter** | 7.2 mH (0.25 p.u.) |

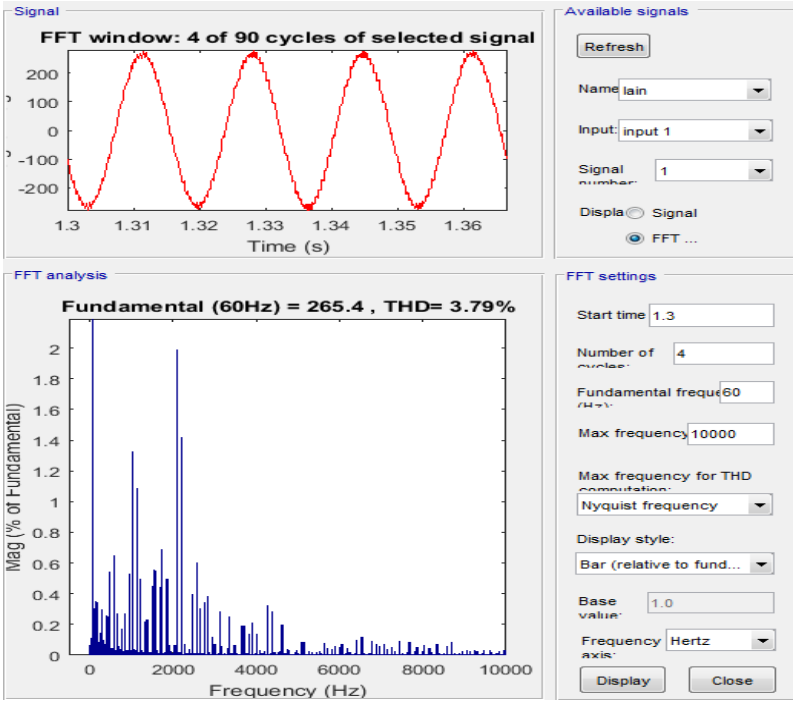



Fig.5-3. THD simulation.

Based on the main circuit parameters, the power loss can be calculated by simulation in the three-level NPC converter at the junction temperatures of 25°C and 125°C. The power loss is calculated both for the rectifier mode and inverter mode. The output characteristics and switching loss of the devices are from the datasheet of commercial Si IGBT (CM600HB-90H). The total loss, which is the sum of the rectifier and the inverter, is 12.9 kW@25°C and 18.37 kW@125°C. The cooling system and operation conditions are the same as those in Chapter 4. Considering each converter may operate in rectifier or inverter mode, the heatsink should be designed based on the worst-case scenario. The total weight of the heatsink is 134 kg (double the weight of the rectifier mode). The power loss calculation and heatsink design parameters are listed in Table 5-3. The total weight and size of the overall power electronics devices here are 30 kg and 0.032 $m^3$.

Table 5-3. Power loss calculation and heatsink design

| **Power loss calculation** | | |
|---|---|---|
| | **Rectifier mode** | **Inverter mode** |
| **T1 conduction** | 64W@25°C/72W@125°C | 68W@25°C/89W@125°C |
| **T1 switching** | 125W@25°C/251W@125°C | 633W@25°C/803W@125°C |
| **T2 conduction** | 87W@25°C/102W@125°C | 88W@25°C/115W@125°C |
| **T2 switching** | 774W@25°C/1,073W@125°C | 6W@25°C/7W@125°C |
| **D1 conduction** | 23W@25°C/18W@125°C | 20W@25°C/16W@125°C |
| **D1 recovery** | 138W@25°C/276W@125°C | 125W@25°C/250W@125°C |
| **Total** | 7.26kW@25°C/10.7kW@125°C | 5.64kW@25°C/7.67kW@125°C |
| **Heat sink design** | | |
| **Cooling** | Forced air | |
| **Rj-c** | 12.5 K/kW | 12.5 K/kW |
| **Airflow** | 4.3 m/s | |
| **Rc-a** | 5.2 K/kW | 7.7 K/kW |
| **Material** | 6063-T5 Aluminum Extrusion Alloy | |
| **Weight** | 67 kg | 45 kg |
| **Size** | 0.054 $m^3$ | 0.036 $m^3$ |

The L filter is designed using silicon steel and the results are listed in Table 5-4. The total loss consumption is 1.92 kW, and the total weight is 2,700 kg for two inductors.

Table 5-4. L filter design

| **Parameter** | **Value** |
|---|---|
| **Copper weight** | 84 kg (7.2 mH) |
| **Core weight** | 890 kg (7.2 mH) |
| **Accessories** | 376 kg (7.2 mH) |
| **Weight** | 1,350 kg (7.2 mH) |
| **Power loss** | 960 W (7.2 mH) |
| **Size** | 1.16 $m^3$(7.2 mH) |

#### 5.2.1.2 Low-frequency transformer

Two transformers are required, one on the grid side and the other on the microgrid side. A commercial 13.8 kV /3.3 kV 60 Hz transformer is selected here, and the data is listed in Table 5-5. Considering a 1 MW rated power and a 0.9 power factor, the capacity is selected as 1.1 MVA. For one transformer, the weight is 2,800 kg with a 99.5% efficiency.

Table 5-5. Low-frequency transformer design

| | |
|---|---|
| **Electrical parameters** | |
| **Capacity** | 1.1 MVA |
| **Ratio** | 13.8 kV/3.3 kV |
| **Frequency** | 60 Hz |
| **Physical parameters** | |
| **Core material** | Silicon steel |
| **Weight** | 2,800 kg |
| **Power loss** | 5 kW |
| **Size** | 4.12 $m^3$ |

### 5.2.2 SiC-Based Three-Level Microgrid PCS Design

Due to the higher voltage rating of the SiC device, the transformer can be eliminated. The three-level NPC back-to-back converter with 13.8 kV AC input and output, as shown in Fig. 5-4, is used in the SiC-based design.

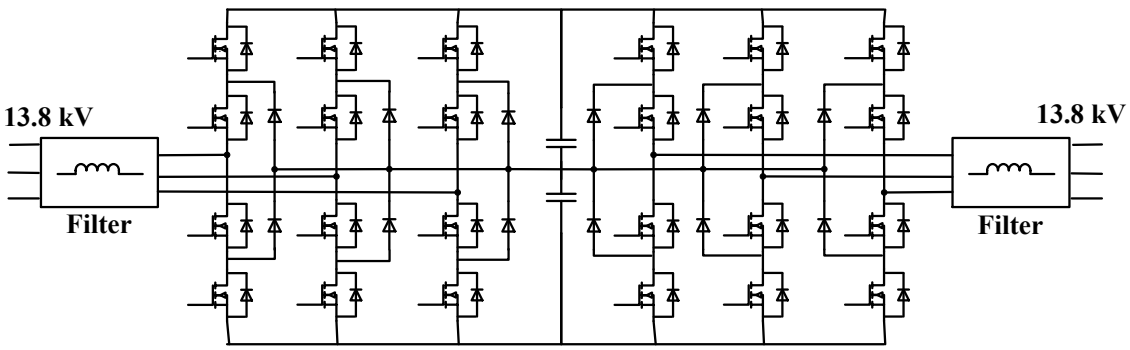
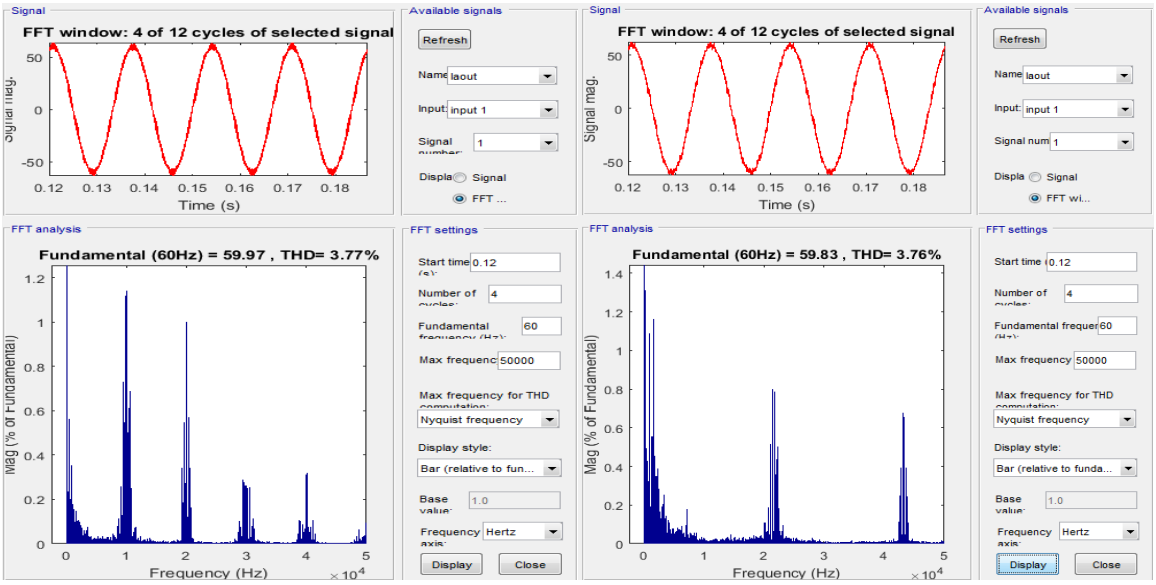



Fig.5-4. SiC-based three-level PCS.

The DC-link voltage is selected as 21 kV considering maximum modulation index, 10% of AC voltage variation, and 0.9 power factor. The power rating is 1.1 MVA due to the power factor requirement. The peak current reaches 73 A. Therefore, 15 kV/ 146 A SiC MOSFET is used here. The switching frequency is selected as 10 kHz (Group 2A). Because the efficiency of the SiC-based three-level converter at a switching frequency of 20 kHz is close to that of the Si-based, the converter with a switching frequency of 20 kHz is designed as well (Group 2B). DC-link capacitance and L filter are designed based on the corresponding switching frequency. The parameters are listed in Table 5-6. The simulation in Fig. 5-5 shows that THD is lower than 5% in both cases.

Table 5-6. Main circuit design

| Parameters | Value |
|---|---|
| **DC-link voltage** | 21 kV |
| **AC output voltage** | 13.8 kV |
| **Power rating** | 1.1 MVA (PF=0.9) |
| **Peak current** | 73 A |
| **Power electronics device** | 15 kV/146 A SiC MOSFET |
| **Switching frequency** | 10 kHz (Group 2A)/20 kHz (Group 2B) |
| **DC-link capacitance** | 28 μF (Group 2A)/14 μF (Group 2B) |
| **Modulation** | SVPWM |
| **L filter** | Group 2A: 15 mH (0.03 p.u.)<br>Group 2B: 11 mH (0.02.p.u.) |




(a) Group 2A (b) Group 2B

Fig.5-5. THD simulation.

Based on the main circuit parameters, the power loss can be calculated by simulation for both 25°C and 125°C junction temperatures. The power loss is calculated both for the rectifier mode and inverter mode and for Group 2A and Group 2B. The output characteristics and switching loss of the device are from the datasheet of the demo chip of 15 kV SiC MOSFET. The total loss is 7.3 kW@25 °C and 8.6 kW@125 °C in Group 2A and 13.9 kW@25 °C and 14.8 kW@125 °C in Group 2B. The heatsink is designed based on the worst case. The total weight of the heatsink is 56 kg for Group 2A and 136 kg for Group 2B. The power loss calculation and heatsink design results are summarized in Table 5-7. The total weight and size of the overall power electronics devices are 24.6 kg and 0.027 $m^3$.

Table 5-7. Power loss calculation and heatsink design

| **Power loss calculation** |
|---|

| | Group 2A | | Group 2B | |
|---|---|---|---|---|
| | **Rectifier mode** | **Inverter mode** | **Rectifier mode** | **Inverter mode** |
| **MOSFET 1 conduction** | 26W@25°C<br>48W@125°C | 41W@25°C<br>83W@125°C | 29W@25°C<br>50W@125°C | 42W@25°C<br>85W@125°C |
| **MOSFET 1 switching** | 38W@25°C<br>40W@125°C | 486W@25°C<br>482W@125°C | 79W@25°C<br>85W@125°C | 986W@25°C<br>975W@125°C |
| **MOSFET 2 conduction** | 36W@25°C<br>66W@125°C | 50W@25°C<br>101W@125°C | 38W@25°C<br>68W@125°C | 50W@25°C<br>101W@125°C |
| **MOSFET 2 switching** | 492W@25°C<br>486W@125°C | 38W@25°C<br>41W@125°C | 990W@25°C<br>977W@125°C | 76W@25°C<br>81W@125°C |
| **Clamping diode conduction** | 8W@25°C<br>16W@125°C | 8W@25°C<br>14W@125°C | 8W@25°C<br>16W@125°C | 8W@25°C<br>15W@125°C |
| **Total** | 3.6kW@25°C<br>4.0kW@125°C | 3.7kW@25°C<br>4.3kW@125°C | 6.9kW@25°C<br>7.2kW@125°C | 7.0kW@25°C<br>7.6kW@125°C |
| **Heatsink design** | | | | |
| **Cooling** | Forced air | | | |
| **Rj-c** | 29 K/kW | | | |
| **Airflow** | 4.3 m/s | | | |
| **Rc-a** | 13.5 K/kW | 12.5 K/kW | 5.5 K/kW | 5.1 K/kW |
| **Material** | 6063-T5 Aluminum Extrusion Alloy | | | |
| **Weight** | 26 kg | 28 kg | 62 kg | 68 kg |
| **Size** | 0.021 $m^3$ | 0.023 $m^3$ | 0.05 $m^3$ | 0.055 $m^3$ |

The line inductor filter is designed using silicon steel and the results are in Table 5-8. The total loss consumption is 590 W in Group 2A and 428 W in Group 2B. The total weight is 366 kg for Group 2A and 268 kg for Group 2B.

Table 5-8. Line filter design

| Parameter | Value |
|---|---|
| **Copper weight** | 17 kg (15 mH)/12.4 kg (11 mH) |
| **Core weight** | 115 kg (15 mH)/84.4 kg (11 mH) |
| **Accessories** | 51 kg (15 mH)/37.4 kg (11 mH) |
| **Weight** | 183 kg (15 mH)/134 kg (11 mH) |
| **Power loss** | 295 W (15mH)/214 W (11 mH) |
| **Size** | 0.135 $m^3$(15 mH)/0.1 $m^3$ (11 mH) |

### 5.2.3 SiC-Based MMC Microgrid PCS Design

The 10 kV SiC devices are relatively more available than the 15 kV devices. To use 10 kV devices to achieve 21 kV DC link voltage, MMC, as a very popular topology in high voltage applications, is selected, as shown in Fig.5-6.

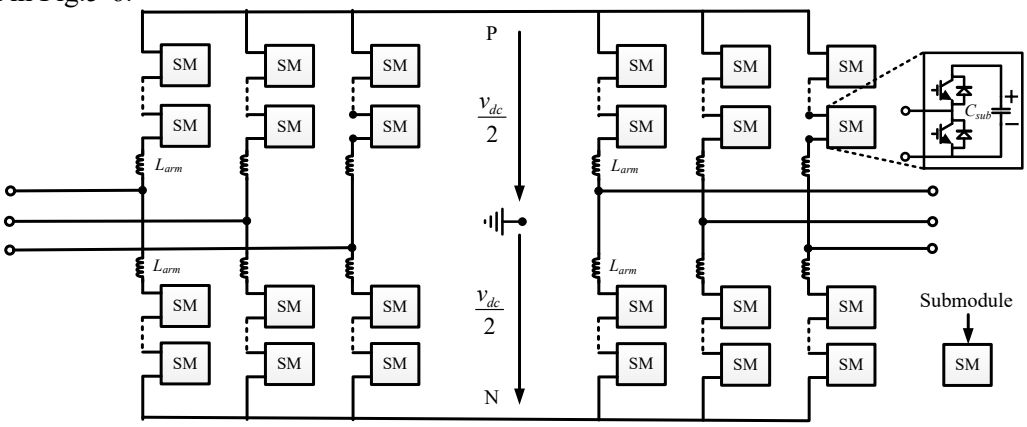
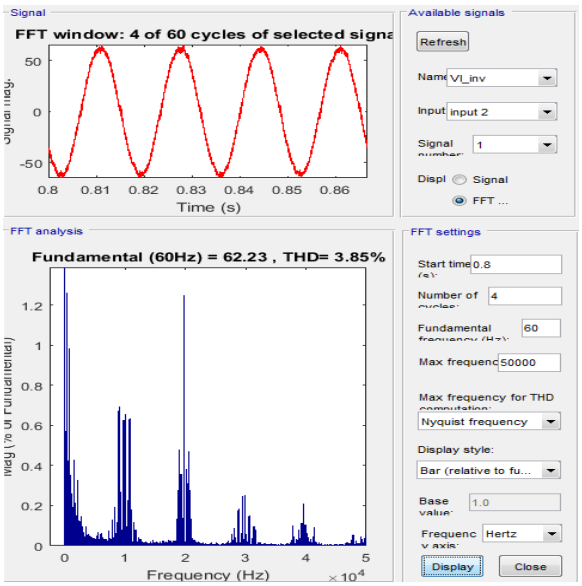



Fig.5-6. SiC-based MMC PCS.

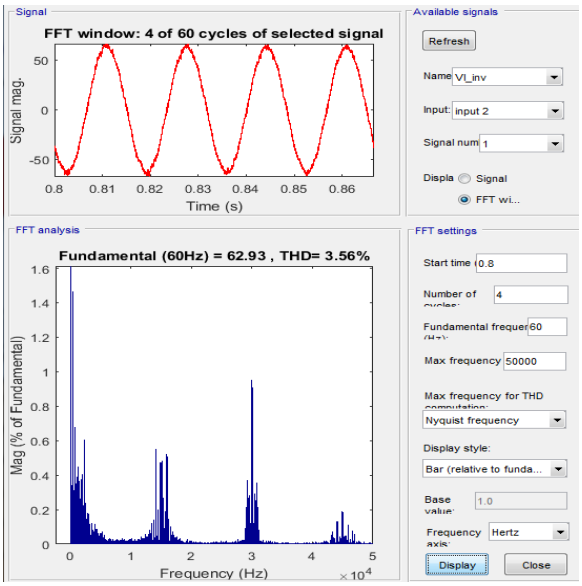
DC-link voltage is 21 kV which is the same as that of the SiC-based three-level NPC converter. Three submodules (SMs) are required for each arm and the DC voltage of the submodule is 7 kV. The max current in the arm is 50 A which approximately equals the sum of half of the AC output current and 1/3 of the DC-link current. Therefore, 10 kV / 100 A SiC MOSFET is used here. The switching frequency is selected as 10 kHz (Group 3A). Because the efficiency of the SiC-based MMC at a switching frequency of 15 kHz is close to the efficiency of the Si-based one, the MMC with a 15 kHz switching frequency is designed as well (Group 3B). To suppress the voltage ripple of the submodule to 10%, the capacitance of the submodule is selected as 70 μF. The DC-link capacitance is selected as 1 μF to maintain the DC-link voltage variation of less than 3%. The inductance is designed based on the corresponding switching frequency. The electrical design results are summarized in Table 5-9. Simulation in Fig.5-7 shows that THD is lower than 5% in both cases.

Table 5-9. Main circuit design

| Parameters | Value |
|---|---|
| **DC-link voltage** | 21 kV |
| **AC output voltage** | 13.8 kV |
| **Power rating** | 1.1 MVA (PF=0.9) |
| **Peak current** | 50 A |
| **SM number per arm** | 3 |
| **SM voltage** | 7 kV |
| **Power electronics device** | 10 kV/100 A SiC MOSFET |
| **SM capacitance** | 70 μF |
| **Switching frequency** | 10 kHz (Group 3A)/15 kHz (Group 3B) |
| **DC-link capacitance** | 1 μF |
| **Arm inductance** | Group 3A: 20 mH (0.04 p.u.)<br>Group 3B: 17 mH (0.034.p.u.) |




(a) Group 3A




(b) Group 3B

Fig.5-7. THD simulation.

Based on the main circuit parameters, the power loss can be calculated by simulation for 25°C and 125°C junction temperatures. The power loss is calculated both for the rectifier mode and inverter mode and for Group 3A and Group 3B. The output characteristics and switching loss of the device are from the datasheet of the 10 kV SiC MOSFET samples. The total loss is 9.1 kW@25 °C and 11.1 kW@125 °C for Group 3A, 12.8 kW@25 °C and 14.9 kW@125 °C for Group 3B. The heatsink is designed based on the worst case. The total weight of the heatsink is 66 kg in Group 3A and 94 kg in Group 3B. The power loss calculation and heatsink design parameters are summarized in Table 5-10. The total weight and size of the overall power electronics devices are 41.8 kg and 0.042 $m^3$.

Table 5-10. Power loss calculation and heatsink design

| **Power loss calculation** | | | | |
|---|---|---|---|---|
| | **Group 3A** | | **Group 3B** | |
| | **Rectifier mode** | **Inverter mode** | **Rectifier mode** | **Inverter mode** |
| **Upper arm conduction** | 166W@25°C<br>335W@125°C | 161W@25°C<br>315W@125°C | 169W@25°C<br>338W@125°C | 159W@25°C<br>310W@125°C |
| **Upper arm switching** | 625W@25°C<br>627W@125°C | 606W@25°C<br>606W@125°C | 946W@25°C/<br>947W@125°C | 951W@25°C<br>949W@125°C |
| **Lower arm conduction** | 169W@25°C<br>344W@125°C | 162W@25°C<br>317W@125°C | 173W@25°C<br>346W@125°C | 159W@25°C<br>312W@125°C |
| **Lower arm switching** | 556W@25°C<br>566W@125°C | 569W@25°C<br>577W@125°C | 844W@25°C<br>857W@125°C | 872W@25°C<br>884W@125°C |
| **Max device loss** | 217W@25°C<br>262W@125°C | 210W@25°C<br>271W@125°C | 313W@25°C<br>358W@125°C | 324W@25°C<br>391W@125°C |
| **Total** | 4.6kW@25°C<br>5.6kW@125°C | 4.5kW@25°C<br>5.5kW@125°C | 6.4kW@25°C<br>7.5kW@125°C | 6.4kW@25°C<br>7.4kW@125°C |

| Heatsink design (considering max device loss) | | | | |
|---|---|---|---|---|
| **Cooling** | Forced air | | | |
| **Rj-c** | 40 K/kW | | | |
| **Airflow** | 4.3 m/s | | | |
| **Rc-a** | 10.7 K/kW | 10.7 K/kW | 7.4 K/kW | 7.4 K/kW |
| **Material** | 6063-T5 Aluminum Extrusion Alloy | | | |
| **Weight** | 33 kg | 33 kg | 47 kg | 47 kg |
| **Size** | 0.027 $m^3$ | 0.027 $m^3$ | 0.038 $m^3$ | 0.038 $m^3$ |

The arm inductor is designed using silicon steel, and the results are shown in Table 5-11. The total loss consumption is 958 W for Group 3A design and 814 W for Group 3B design. The total weight is 580 kg in Group 3A and 476 kg in Group 3B.

Table 5-11. Arm inductor design

| Parameter | Value |
|---|---|
| **Copper weight** | 29 kg (20 mH)/24 kg (17 mH) |
| **Core weight** | 181 kg (20 mH)/153 kg (17 mH) |
| **Accessories** | 81 kg (20 mH)/69 kg (17 mH) |
| **Weight** | 290 kg (20 mH)/238 kg (17 mH) |
| **Power loss** | 479 W (20 mH)/407 W (17 mH) |
| **Size** | 0.215 $m^3$ (20 mH)/0.175 $m^3$ (17 mH) |

### 5.2.4 Comparison

Figs. 5-8 through 5-10 display the power loss, weight, and size comparison and the corresponding breakdown. The values are listed in Table 5-12 through Table 5-14. Due to the lower switching loss, the power losses of SiC-based three-level NPC with a switching frequency of 20 kHz (i.e. Group 2B) and SiC-based MMC with a switching frequency of 15 kHz (i.e. Group 3B) are close to the power loss of Si-based three-level NPC with switching frequency of 1 kHz (i.e. Group 1), even without including the power loss of the transformer. With a switching frequency of 10 kHz, the power losses of SiC-based three-level NPC (i.e. Group 2A) and SiC-based MMC (i.e. Group 3A) are 53.4% and 68.2% of that of the Si-based design (i.e. Group 1), respectively.

For SiC-based three-level NPC, the weights of Group 2A and Group 2B are only 17% and 15.6% of Group 1 Si-based three-level NPC. The specific powers of Group 2A and Group 2B are 15.7 times and 17.1 times of that of Group 1. And the sizes of Group 2A and Group 2B are 18.8% and 16.2% of that of Group 1. The power densities in Group 2A and Group 2B are 9.6 times and 11.1 times of that of Group 1. By comparing the results of Group 2A and Group 2B, the weight and size decrease with the increase of the switching frequency.

For SiC-based MMC, due to a large number of submodule capacitors and more devices, the benefit in weight and size is not as much as SiC-based three-level NPC. But it still shows impressive benefits compared to the Si-based design. The weights of Group 3A and Group 3B converters are still 39.8% and 37.4% of that of Group 1. The specific powers are 6.7 times and 7.1 times of that of Group 1. The size of Group 3A and Group 3B converters are 33.2% and 31.3% of that of Group 1. Their power densities are 5.4 times and 5.8 times of that of Group 1.

Table 5-12. Power loss comparison

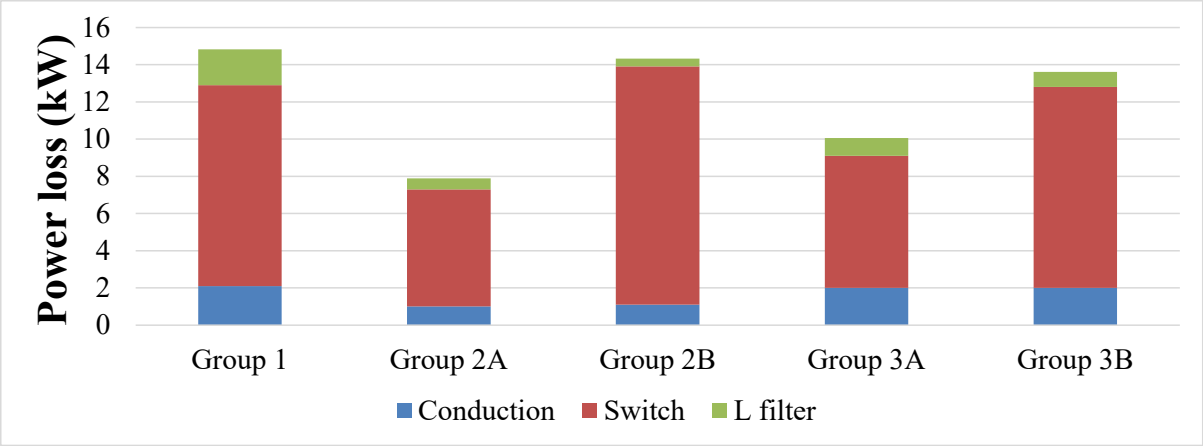
| | Group 1 | Group 2A | Group 2B | Group 3A | Group 3B |
|---|---|---|---|---|---|
| **Active device with heatsink** | 12.9 kW | 7.3 kW | 13.9 kW | 9.1 kW | 12.8 kW |
| **Output filter** | 1.92 kW | 590 W | 428 W | 958 W | 814 W |
| **Transformer** | 10 kW | - | - | - | - |
| **w/o transformer** | 14.8 kW | 7.9 kW | 14.3 kW | 10.1 kW | 13.6 kW |
| **Efficiency** | 98.52% | 99.21% | 98.57% | 98.99% | 98.64% |
| **Ratio** | 1.0 | 0.534 | 0.966 | 0.682 | 0.919 |

Table 5-13. Weight comparison

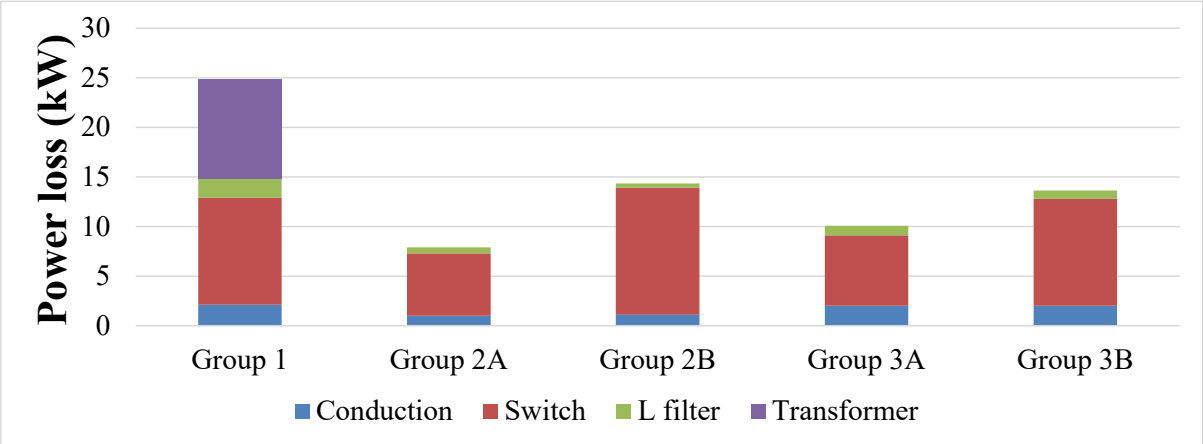
| | Group 1 | Group 2A | Group 2B | Group 3A | Group 3B |
|---|---|---|---|---|---|
| **Active device with heatsink** | 164 kg | 80.6 kg | 160.6 kg | 107.8 kg | 135.8 kg |
| **Output filter** | 2,700 kg | 366 kg | 268 kg | 580 kg | 476 kg |
| **Capacitor** | 158 kg | 72 kg | 36 kg | 532 kg | 532 kg |
| **Bus bar** | 73 kg | 9.2 kg | 18.2 kg | 12 kg | 15.2 kg |
| **Housing** | 344 kg | 59 kg | 54 kg | 137 kg | 129 kg |
| **Transformer** | 5,600 kg | - | - | - | - |
| **w/o transformer** | 3,439 kg | 586 kg | 536 kg | 1,369 kg | 1,288 kg |
| **Ratio** | 1.0 | 0.170 | 0.156 | 0.398 | 0.374 |
| **Specific power** | 0.12 MW/ton | 1.88 MW/ton | 2.05 MW/ton | 0.80 MW/ton | 0.85 MW/ton |

Table 5-14. Size comparison

| | Group 1 | Group 2A | Group 2B | Group 3A | Group 3B |
|---|---|---|---|---|---|
| **Active device with heatsink** | 0.14 $m^3$ | 0.07 $m^3$ | 0.14 $m^3$ | 0.09 $m^3$ | 0.12 $m^3$ |
| **Output filter** | 2.32 $m^3$ | 0.27 $m^3$ | 0.20 $m^3$ | 0.43 $m^3$ | 0.35 $m^3$ |
| **Capacitor** | 0.1 $m^3$ | 0.14 $m^3$ | 0.07 $m^3$ | 0.33 $m^3$ | 0.33 $m^3$ |
| **Bus bar** | 0.008 $m^3$ | 0.001 $m^3$ | 0.002 $m^3$ | 0.001 $m^3$ | 0.002 $m^3$ |
| **Transformer** | 4.12 $m^3$ | - | - | - | - |
| **w/o transformer** | 5.12 $m^3$ | 0.96 $m^3$ | 0.83 $m^3$ | 1.70 $m^3$ | 1.60 $m^3$ |
| **Ratio** | 1.0 | 0.188 | 0.162 | 0.332 | 0.313 |
| **Power density** | 0.12 MW/$m^3$ | 1.15 MW/$m^3$ | 1.33 MW/$m^3$ | 0.65 MW/$m^3$ | 0.69 MW/$m^3$ |

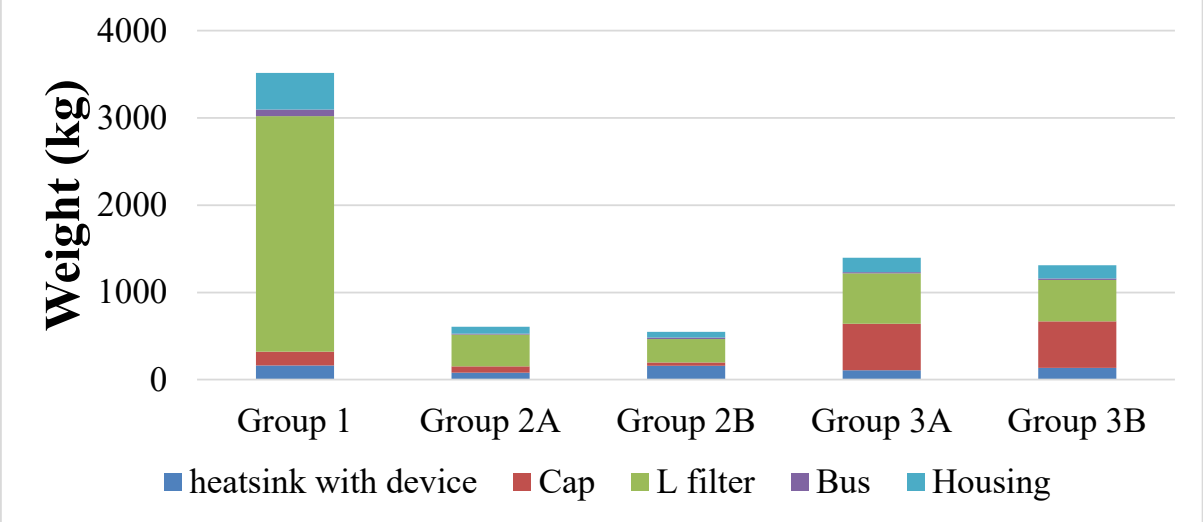



(a) w/o transformer

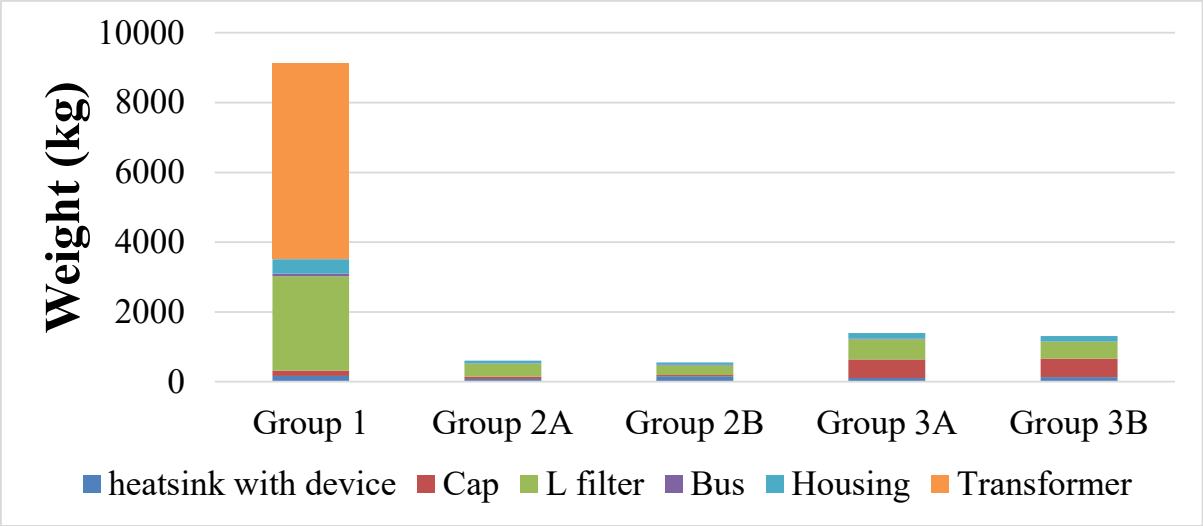



(b) w/ transformer

Fig.5-8. Power loss comparison.

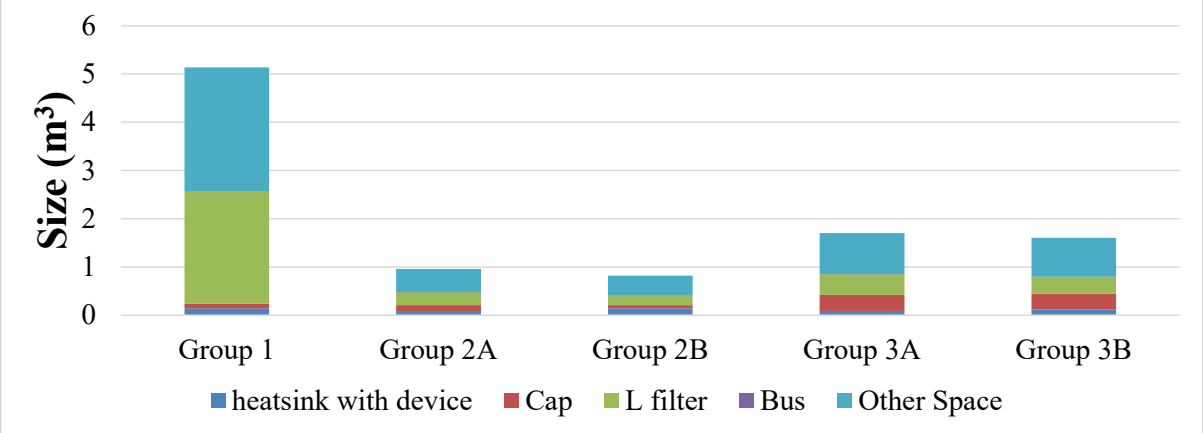



(a) w/o transformer

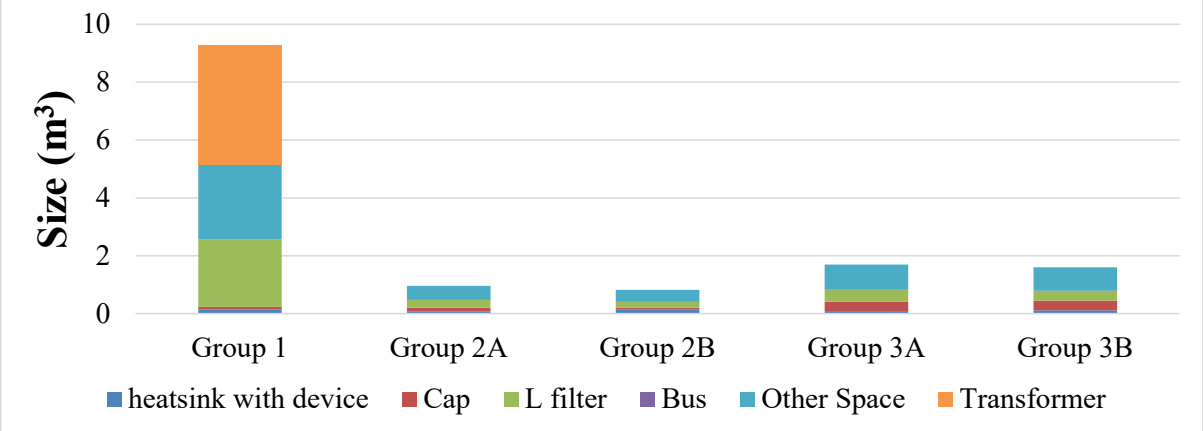



(b) w/ transformer

Fig.5-9. Weight Comparison.




(a) w/o transformer




(b) w/ transformer

Fig.5-10. Size comparison.

Based on the above design comparison, it can be concluded that: 1) Compared to the Si-based system, even without including a transformer, the improvement of SiC-based microgrid PCS is significant (83% weight reduction and 81% size reduction with three-level NPC, 60% weight reduction and 67% size reduction with MMC); 2) for the same efficiency, the switching frequency of SiC-based microgrid PCS converter can be much higher (nearly 10 to 20 times of that of Si-based converter). The much-increased switching capability and high switching frequency can lead to many system-level benefits. These benefits will be discussed in the next section.

## 5.3 SYSTEM LEVEL BENEFITS

The benefits of the asynchronous microgrid over a conventional microgrid will be discussed first by comparing the performance of the microgrid with and without the PCS. Furthermore, the benefits of the SiC-based PCS will be benchmarked against the Si-based solution. The benefits are shown for both the grid-connected mode and islanded mode, including normal and abnormal operating conditions.

The potential system-level benefits of asynchronous microgrids with PCS as well as SiC-based PCS are summarized in Table 5-15.

Table 5-15. Potential system-level benefits of the SiC-based microgrid PCS

| **Grid-connected mode** | | |
|---|---|---|
| **Use case** | **Benefits of microgrid PCS** | **Benefits of SiC** |
| **Frequency & voltage control** | Easy for a) reactive power support, for both sides independently; b) power transfer control | Not obvious (smaller filter for more var), dynamic response |
| **Stability** | *Isolation* – Can isolate stability issue of microgrid, enabling easy integration of high renewable microgrid with the existing ac grid.<br>*small-signal stability* – Will generally simplify the design for stability. A microgrid stable in the islanded case can be more easily integrated with the ac grid.<br>*Oscillation damping & voltage stability* - Easier inertia emulation & var support | *small-signal stability* - Faster SiC can help control and impedance forming<br>*Oscillation damping* Faster SiC can help with inertia emulation & var support |
| **Power quality** | Interface converters can provide active power filtering (APF) functions for both ac grid and microgrid. Can save dedicated filters | APF function only effective with SiC |
| **LVRT** | No voltage drop in microgrid, load voltage maintained | Better dynamic response |
| **Multi-feeder microgrid** | Easy to achieve microgrid with multiple feeders: a) No need for information on voltage amplitude and phase of feeders; 2) Easy to isolate from the faulted feeder and maintain the connection with other feeders; easy power flow | Not obvious |
| **Short circuit current** | Short circuit current will be reduced with the asynchronous microgrid, as the interface converters will isolate/limit fault current contributions | Not obvious |
| **Efficiency** | Will incur additional loss during normal operation – a drawback of the microgrid PCS | SiC can have lower power loss than Si |
| **Islanded mode** | | |

| | | |
|---|---|---|
| **Transition** | Seamless transition between grid-connected and islanded modes, no voltage drop in microgrid | Better dynamic response |
| **Frequency & voltage control** | Microgrid side PCS provides var support | Not obvious |
| **Stability** | Microgrid PCS could be a stabilizer | Faster SiC can help control and impedance forming |
| **Power quality** | Microgrid side interface converter can provide APF function when SiC is applied for MG, reducing or eliminating the need for dedicated filters | APF function only effective with SiC |
| **Black start** | Black start is easy with Microgrid PCS, but no obvious benefit over traditional islanded microgrid | Not obvious |
| **Other benefits: The interface converters can integrate energy storage, CHP/local generation, and fault current limiting/protection functions.** | | |

The asynchronous microgrids can lead to many system-level benefits; however, not all of these benefits can utilize the fast switching capabilities enabled by SiC. This section focuses on the system-level issues that can potentially benefit from SiC solutions, including power quality, stability, LVRT, the transition between grid-connected mode and islanded mode, and black start. The simulation will be carried out to benchmark these benefits. Note that microgrid PCS converters can integrate energy storage, CHP, and other local generation through the DC link. They can also integrate fault current limiting and protection functions. However, these advanced functionalities will not be in the scope of this benchmark study.

The configuration of the microgrid simulated in this section is shown in Fig.5-1. In the case that CHP, BESS, and PV do not supply any power, the 1 MW load can be supplied by the utility grid through the PCS. In the case that PV has a full power output, but all the loads are off, the output power of PV can be supplied to the utility through the PCS. Therefore, the PCS should be capable of working in both of these cases, supplying full PV power to the utility or transferring full power from the utility to loads. Therefore, the power rating of the PCS is selected as 1 MW. The performance on power quality, system stability, LVRT, mode transition, and black start is assessed using simulation for three cases: without the PCS, with Si and SiC-based PCS. In the simulation of this section, the SiC-based PCS is assumed to switch at 10 kHz considering that the improvement in control bandwidth with 10 kHz is high enough to show the system benefits. With a switching frequency of 10 kHz, the SiC-based PCS still has significant efficiency benefits based on the design in the last section. Noted also that the DER interface converters (i.e. interface converters for PV and BESS systems) in this section are assumed to be Si-based converters. In other words, with SiC-based microgrid PCS, no other converters in the microgrid need to be high bandwidth SiC based for enhanced system performance.

### 5.3.1 Power Quality Improvement

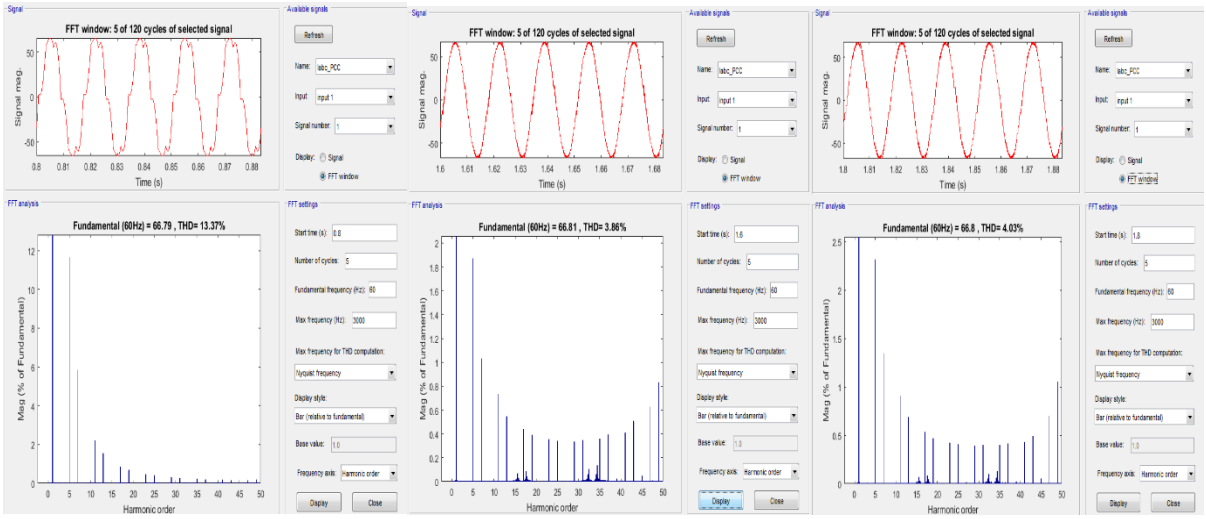
The PCS for an asynchronous microgrid can isolate harmonics issues between the microgrid and the grid. Therefore, the harmonics on the microgrid side will not impact the grid side and vice versa. If the load in the microgrid generates harmonic currents, it will not cause harmonic components in the grid side with PCS. If the PCS converters are Si-based, due to the low switching frequency (i.e. 1 kHz) of these high power converters, the PCS converters cannot help filter the microgrid harmonic components, and a dedicated Si APF is needed as described in the last chapter. On the other hand, by using SiC-based PCS with a switching frequency of 10 kHz, the APF function can be integrated into the PCS. The harmonic components can be compensated by the PCS and will not impact other equipment in the microgrid. Therefore, two solutions are compared in this section: 1) Si-based solution, a Si-based PCS with 1 kHz

switching frequency plus a Si-based APF with 10 kHz switching frequency; 2) SiC-based solution, only a SiC-based PCS with 10 kHz switching frequency. The setups of the two solutions are listed in Table 5-16. The target is to maintain the TDD of the current which flows through the other equipment in the microgrid (i.e. the sum of the current in BESS, PV, and CHP in this case) to be lower than 5%. The two solutions are compared in terms of the converter rating requirement.

The performance can be functions of operating conditions. In the case when the output power of the PCS is zero, The TDD simulation results of the total current in BESS, PV, and CHP are shown in Fig.5-11. Without harmonics compensation, 15% harmonic current, which is from the non-linear six-pulse uncontrolled rectifier load, is injected into the equipment. TDD becomes less than 5% both with additional Si-based APF and SiC-based PCS.

Table 5-16. Solutions of harmonics compensation

| | **Solution 1: Si-based** | **Solution 2: SiC-based** |
|---|---|---|
| Converter type | Si-based (PCS, BESS, PV, APF) | SiC-based (PCS)<br>Si-based (BESS, PV) |
| Switching frequency | 1 kHz (PCS)<br>3 kHz (BESS, PV)<br>10 kHz (APF) | 10 kHz (PCS)<br>3 kHz (BESS, PV) |
| Current control bandwidth | 200 Hz (PCS)<br>600 Hz (BESS, PV)<br>2 kHz (APF) | 2 kHz (PCS)<br>600 Hz (BESS, PV) |
| Load | six-pulse uncontrolled rectifier | six-pulse uncontrolled rectifier |




(a) without harmonic compensation (b) Si-based solution (c) SiC-based solution

Fig.5-11. TDD simulation.

Because the grid impedance is isolated by the PCS, the TDD only varies with the output power of the PCS. The TDD simulation results are shown in Fig.5-12. TDD is lower than 5% when output power varies from -1 MW to 1 MW. For the Si-based solution, the converter rating is the sum of the converter ratings of the Si-based PCS and the Si-based APF. For the SiC-based solution, it is just the converter rating of the

SiC-based PCS. The relationship between the output power of the PCS and total current rating (i.e. sum of PCS and APF current) is shown in Fig.5-13.

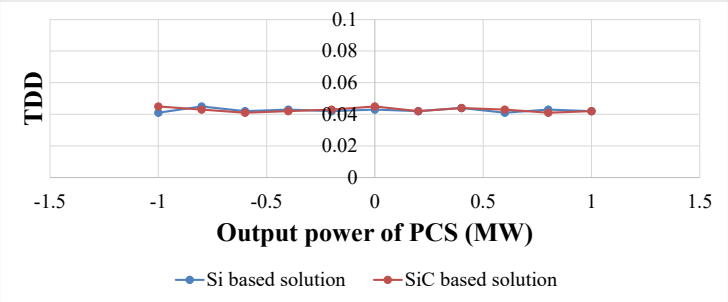



Fig.5-12. TDD variation with output power.

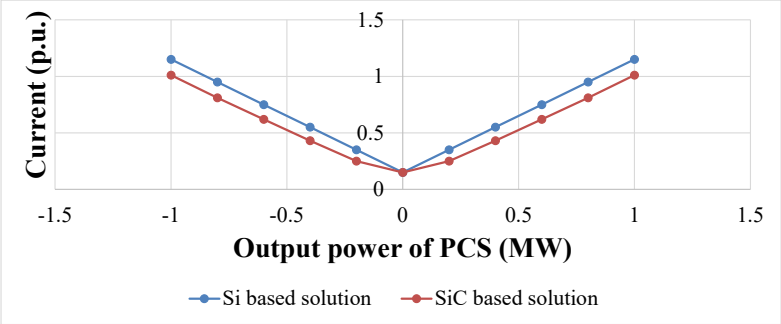



Fig.5-13. Current rating comparison.

It can be concluded that the Si-based solution needs an extra 150 kVA (15% more) converter for Si-based APF while the impact on SiC-based converter rating is minimal (~1%). By eliminating the dedicated active filters, the SiC-based solution saves a 14% converter rating.

### 5.3.2 System Stability Enhancement

The benefits of the HV SiC PCS module on the stability of the asynchronous microgrid are investigated in both the grid-connected mode and the islanded mode.

#### 5.3.2.1 Grid-connected mode

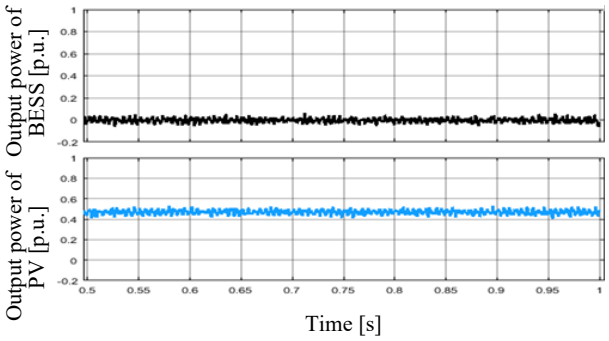
Three cases are compared. Case 1: without the PCS. Case 2: with Si-based PCS. Case 3: with SiC-based PCS. The detailed parameters of these three cases are listed in Table 5-17.

Table 5-17. Case setups for stability study of the microgrid in the grid-connected mode.

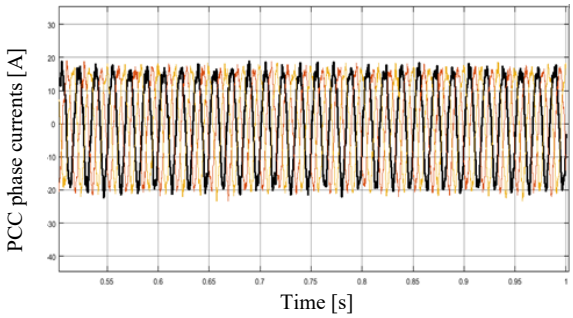
| | Case 1 | Case 2 | Case 3 |
|---|---|---|---|
| **Converter type** | Si-based (BESS, PV) | Si-based (BESS, PV, PCS) | Si-based (BESS, PV)<br>SiC-based (PCS) |
| **Switching frequency** | 3 kHz (BESS, PV) | 3 kHz (BESS, PV)<br>1 kHz (PCS) | 3kHz (BESS, PV)<br>10 kHz (PCS) |

| | | | |
|---|---|---|---|
| **Control bandwidth** | 300 Hz (BESS, PV) | 300 Hz (BESS, PV)<br>100 Hz (PCS) | 300 Hz (BESS, PV)<br>1 kHz (PCS) |
| **Load** | 1 MW, 80% active rectifier load, 20% resistive and capacitive load | | |

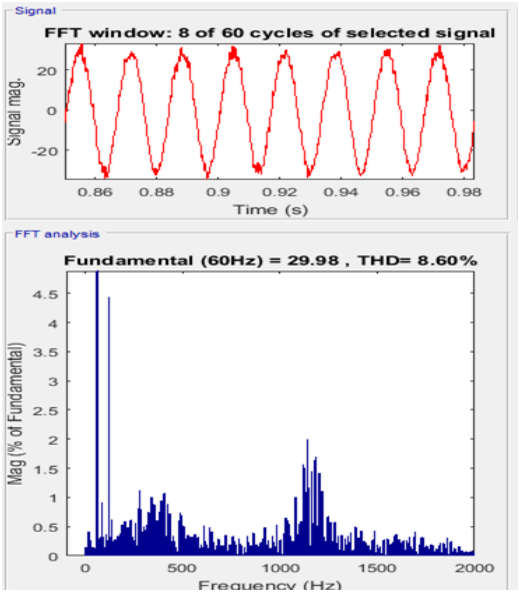
Several simulations of each case are conducted in MATLAB/Simulink to study the stability of the microgrid. For Case 1, two different grid conditions are considered, namely, 1) the grid impedance is 0.05 p.u., and 2) the grid impedance is 0.1 p.u.. Fig.5-14(a) depicts the power outputs of the BESS and the PV in the microgrid, Fig.5-14(b) illustrates the waveforms of the PCC phase currents, and Fig. Fig.5-14(c) shows the FFT analysis results of the PCC current when the grid impedance is 0.05 p.u.. In addition, the simulation results with the grid impedance of 0.1 p.u. are shown in Fig.5-15. It shows that the microgrid without the interface PCS converter is stable with a strong grid but becomes unstable in a weak grid.




(a) active power outputs of BESS and PV

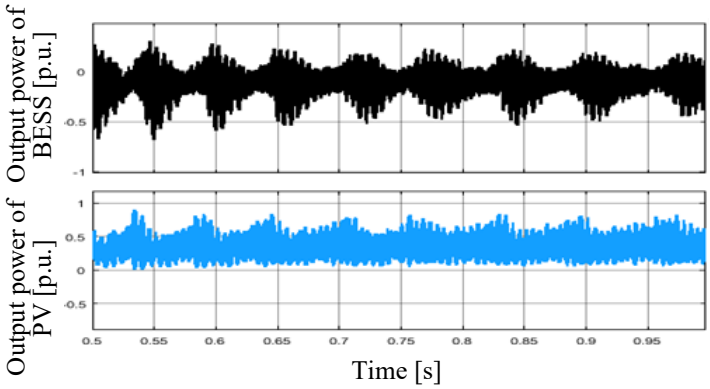



(b) PCC phase current

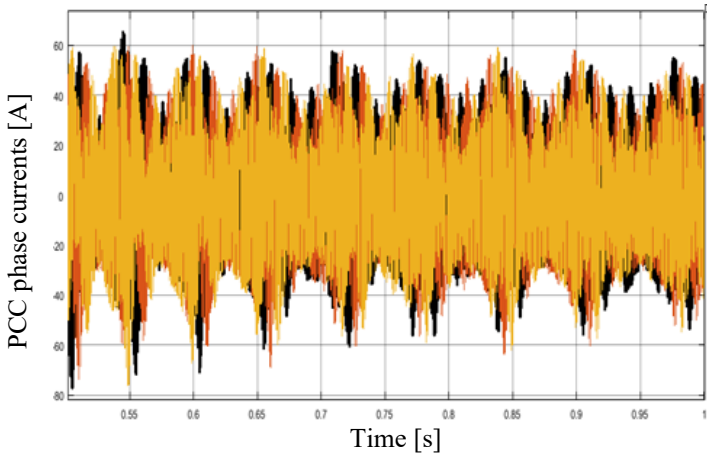



(c) FFT analysis of PCC current

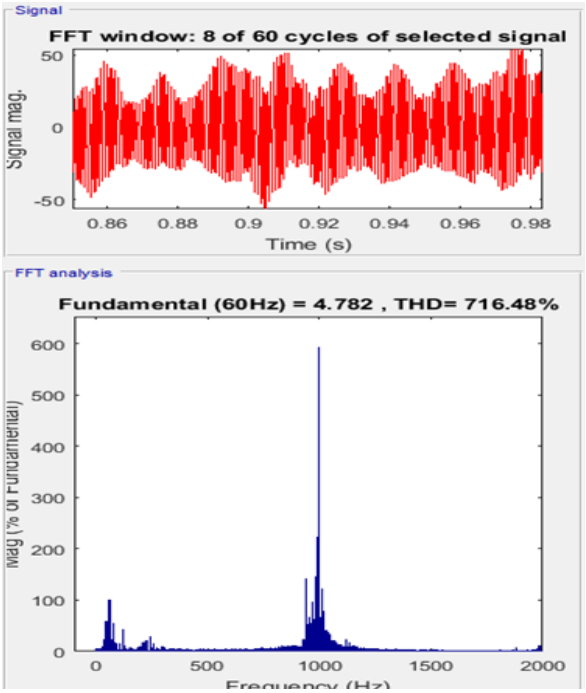
Fig.5-14. Simulation results of Case 1 when the grid impedance is 0.05 p.u..




(a) active power outputs of BESS and PV



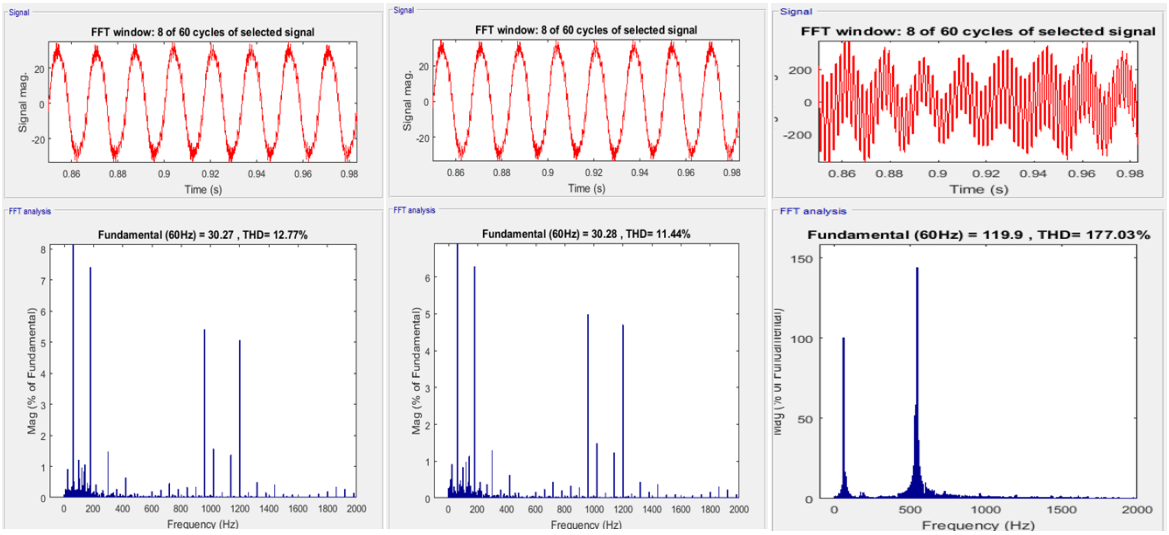

(b) PCC phase current




(c) FFT analysis of PCC current

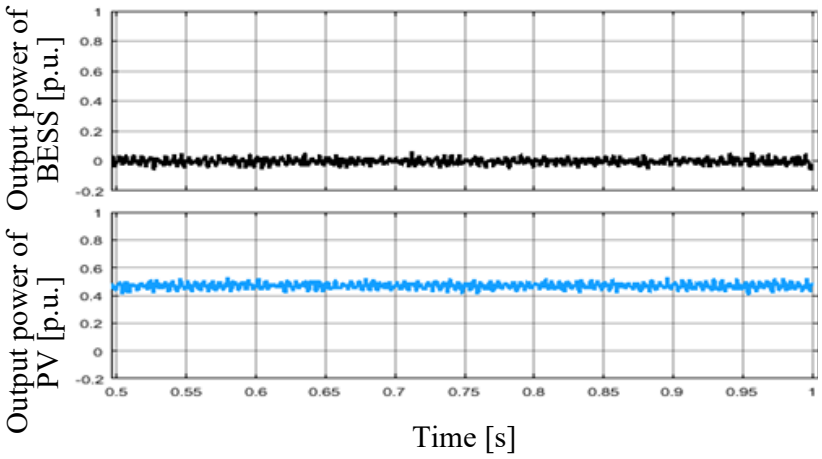
Fig.5-15. Simulation results of Case 1 when the grid impedance is 0.1 p.u..

For Case 2 with Si-based microgrid PCS, three grid conditions are evaluated, namely, 1) the grid impedance is 0.05 p.u., 2) the grid impedance is 0.1 p.u., and 3) the grid impedance is 0.1 p.u. and an additional PFC capacitor with 0.163 p.u. capacitance is installed at the grid side of the PCC. Fig.5-16 shows the time-domain waveforms and FFT analysis of PCC phase currents under the aforementioned three grid conditions. The stable system operation in Fig.5-16(a) and Fig.5-16(b) indicates that the Si-based PCS can facilitate the stable integration of a microgrid into a weak grid. However, the unstable resonance with a frequency of about 600 Hz in Fig.5-16(c) shows that the grid-side of the Si-based microgrid PCS could still suffer from instability issues if there are high capacitive components present in the weak grid. The resonance is caused by the interaction between the weak grid and the non-passive admittance of the grid-side converter of the PCS. Since the switching frequency and control bandwidth of the Si-based converter are limited, the grid-side unstable resonance is not damped.

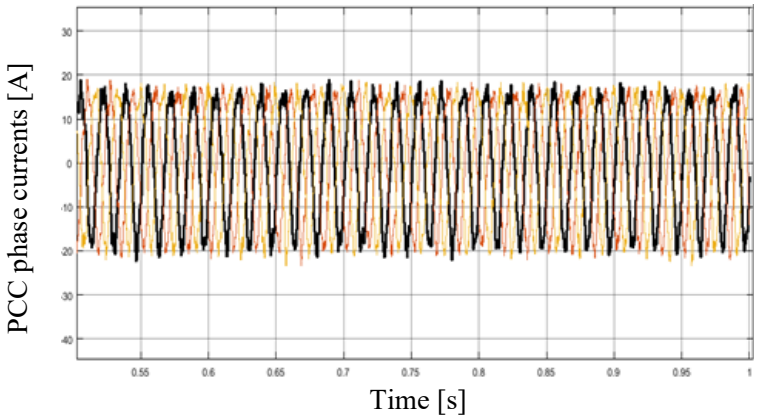



(a) grid impedance is 0.05p.u. (b) grid impedance is 0.1p.u. (c) grid impedance is 0.1p.u., PFC capacitor at the grid side is 0.163p.u.

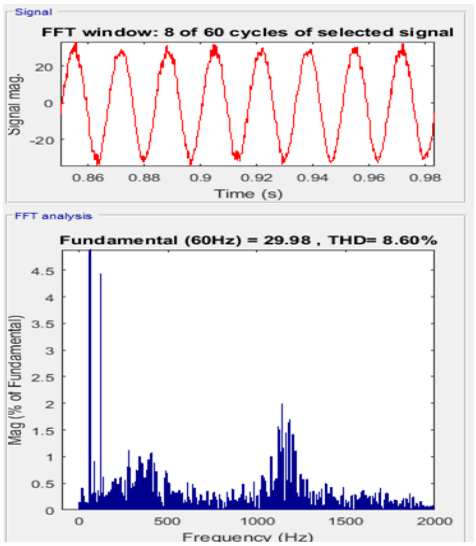
Fig.5-16. Simulation results of PCC phase currents in Case 2.




(a) active power outputs of BESS and PV




(b) PCC phase current

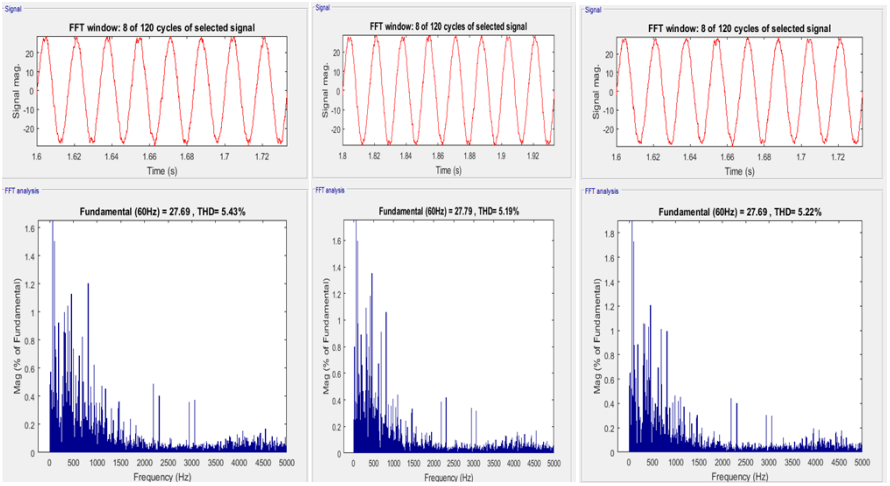



(c) FFT analysis of PCC current

Fig.5-17. Simulation results of the microgrid in Case 2.

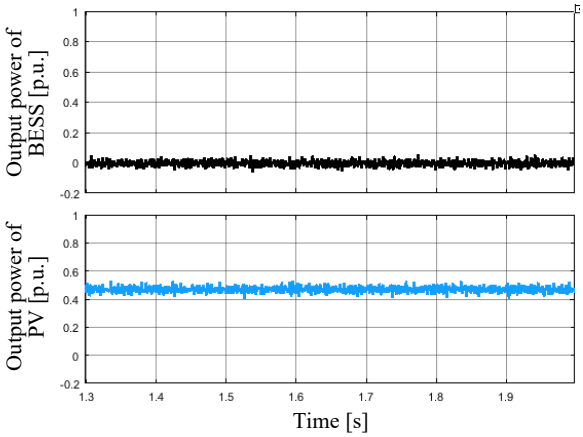
Nevertheless, the microgrid PCS has the benefit of isolating the stability issues of the microgrid from the stability issues of the weak grid. Fig.5-17(a) depicts the active power output of the BESS and the PV, while Fig.5-17 (b) and (c) show the time-domain waveform and FFT analysis of the PCC phase currents, under the aforementioned three grid conditions. Obviously, due to the isolation effect of the PCS, the microgrid is stable under all three grid conditions.

The aforementioned three grid conditions are also considered for Case 3 with SiC-based microgrid PCS. Fig.5-18 illustrates the time-domain waveforms and FFT analysis of PCC phase currents under these three grid conditions. The system is stable under all three grid conditions, thanks to the high switching frequency and high control bandwidth of the SiC-based converters. In addition, the stability of the microgrid itself is also preserved, as shown in Fig.5-19.

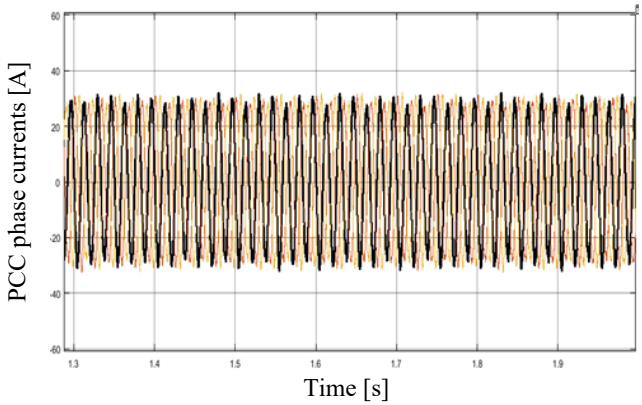



(a) grid impedance is 0.05p.u. (b) grid impedance is 0.1p.u. (c) grid impedance is 0.1p.u., PFC capacitor at the grid side is 0.163p.u.

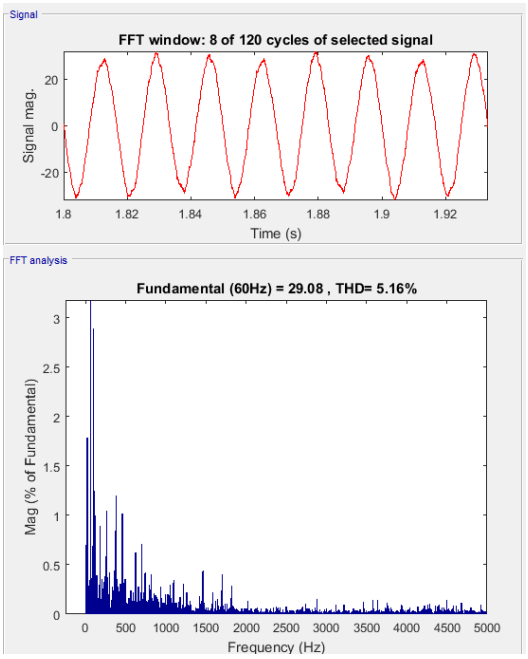
Fig.5-18. Simulation results of PCC phase currents in Case 3.




(a) Active power outputs of BESS and PV




(b) PCC phase current




(c) FFT analysis of PCC current

Fig.5-19. Simulation results of the microgrid in Case 3.

#### 5.3.2.2 Islanded mode

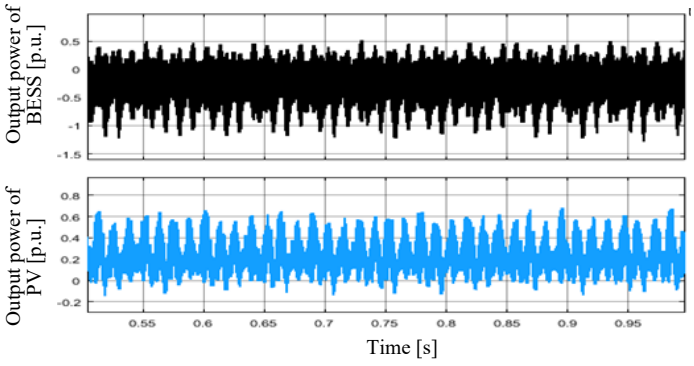
Two cases are studied to investigate the benefits of the microgrid PCS on the stability of the microgrid in the islanded mode. Case 1: without SiC-based PCS. Case 2: with SiC-based PCS. The detailed parameters of the two cases are presented in Table 5-18.

Table 5-18. Case setups for stability study of the microgrid in the grid-connected mode.

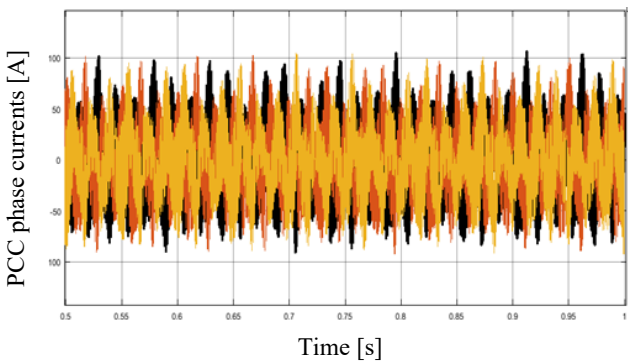
| | Case 1 | Case 2 |
|---|---|---|
| **Converter type** | Si-based (BESS, PV) | Si-based (BESS, PV)<br>SiC-based (PCS) |
| **Switching frequency** | 3 kHz (BESS, PV) | 3 kHz (BESS, PV)<br>10 kHz (PCS) |
| **Control bandwidth** | 300 Hz (BESS, PV) | 300 Hz (BESS, PV)<br>1 kHz (microgrid PCS) |
| **Load** | 1MW, 80% is active rectifier load, 20% is resistive and capacitive loads | |

In Case 1, the microgrid with Si-based converters is unstable under the specific load condition. Fig.5-20(a) shows the active power output of the BESS and the PV, while the time-domain waveform and FFT analysis of the PCC phase currents are given in Fig.5-20 (b) and (c). Due to the interaction between the non-passive output admittance of the Si-based converter and the capacitive load within the microgrid, there is an unstable resonance with a frequency near 1000 Hz. However, when the SiC-based microgrid PCS is adopted in Case 2, the microgrid-side SiC-based converter with a high control bandwidth can work as a stabilizer to actively damp the unstable resonance and enhance the stability of the microgrid. Fig.5-21 shows the stable operation of the microgrid with the SiC-based microgrid PCS.

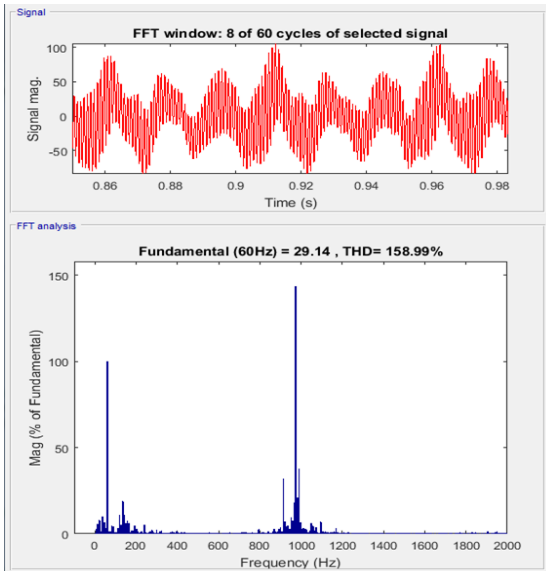
In summary, the SiC-based microgrid PCS can enhance the stability of the microgrid in both the grid-connected mode and the islanded mode. Specifically, in the grid-connected mode, SiC-based microgrid PCS can help stabilize both the grid side and microgrid side. It can stably work with a) a weak grid, which could introduce instability issues for conventional microgrids, and b) unfavorable grid-side loads, which could cause unstable problems for Si-based microgrid PCS. In the islanded mode, the SiC-based microgrid PCS can behave as a stabilizer to damp the resonance within the microgrid.




(a) Active power outputs of BESS and PV

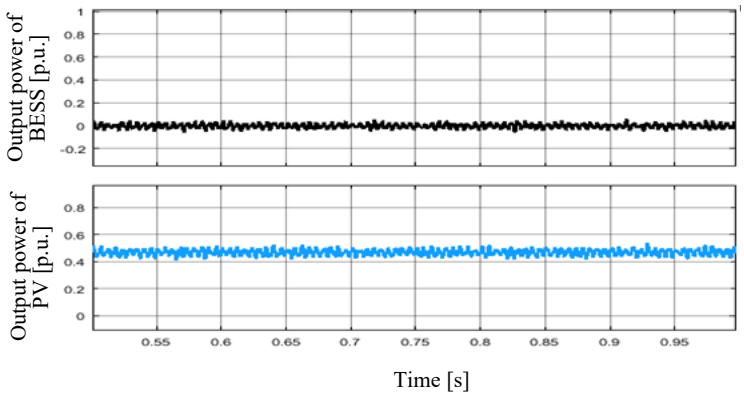



(b) PCC phase current

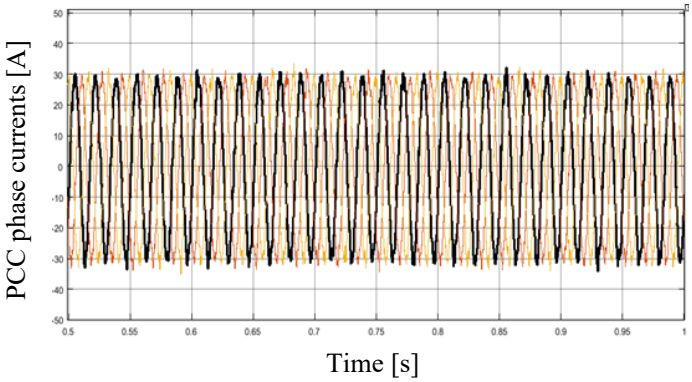



(c) FFT analysis of PCC current

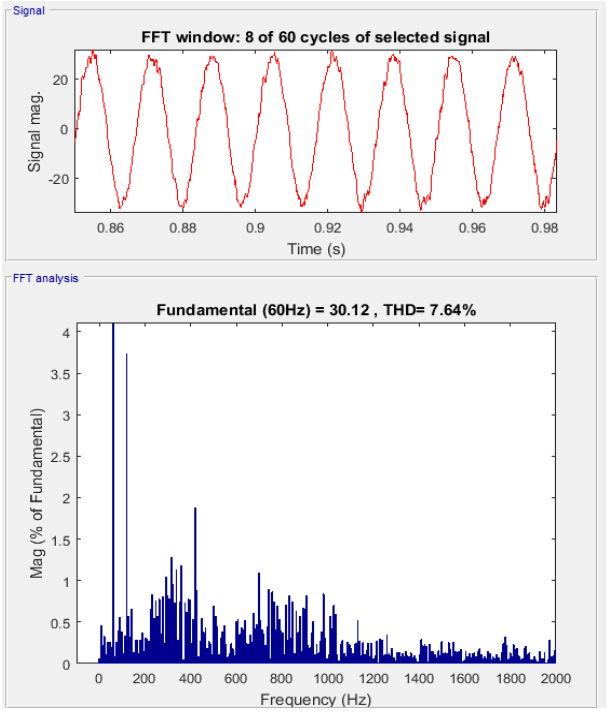
Fig.5-20. Simulation results of the microgrid in Case 1.




(a) Active power outputs of BESS and PV




(b) PCC phase current




(c) FFT analysis of PCC current

Fig.5-21. Simulation results of the microgrid in Case 2.

### 5.3.3 Low Voltage Ride Through

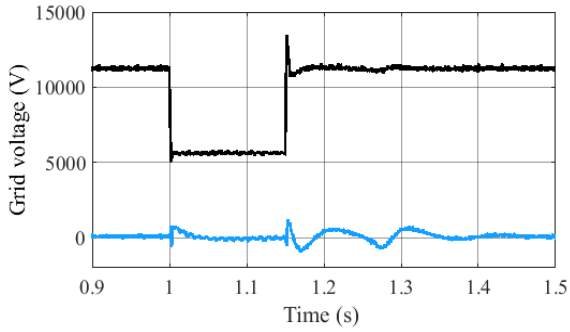
The LVRT in conventional AC microgrids has been studied in Chapter 4. In the conventional AC microgrid, the DER converters have LVRT capability. However, due to the voltage drop in the PCC, the load has to operate abnormally. By using the asynchronous microgrid PCS, there is no voltage drop in the PCC of the microgrid side and the load voltage is maintained. The LVRT performance using Si- and SiC-based microgrid PCS is simulated in this subsection. The setup of Si- and SiC-based LVRT simulation is in Table 5-19. The IEEE Std 1547-2014 is again followed.

Table 5-19. Setup for LVRT simulation

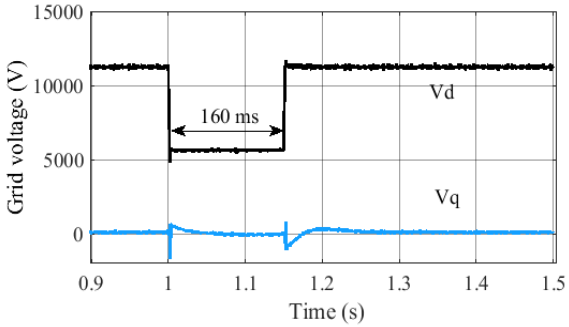
| | **Setup 1: Si-based** | **Setup 2: SiC-based** |
|---|---|---|
| Converter type | Si-based (PCS, BESS, PV) | SiC-based (PCS) |

| | | Si-based (BESS, PV) |
|---|---|---|
| Switching frequency | 1 kHz (PCS)<br>3 kHz (BESS, PV) | 10 kHz (PCS)<br>3 kHz (BESS, PV) |
| Current control bandwidth | 100 Hz (PCS)<br>300 Hz (BESS, PV) | 1 kHz (PCS)<br>300 Hz (BESS, PV) |
| Load | 80% active rectifier, 20% resistor | |

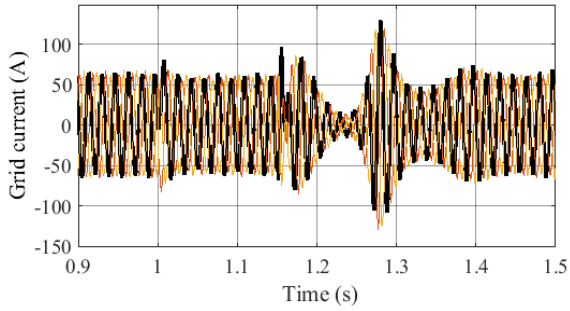
The simulation results are shown in Fig.5-22. The operation steps during the LVRT period are as follows: 1) The grid supplies the power to the load until the grid voltage drop starts (1.0 s); 2) The grid voltage drop (45% of the rated voltage) is detected. The converter of microgrid PCS on grid side VSC1 operates in LVRT mode and supplied 1.0 p.u. reactive current. The converter on the microgrid side VSC2 transitions to rectifier mode such that the DC-link voltage of microgrid PCS can be maintained. 3) After 160 ms, the grid voltage returns to the rated voltage. The microgrid recovers to the operation before Step 1. The PCC voltage on the microgrid side which is also the load voltage can be maintained both with Si- and SiC- based microgrid PCS. But due to the higher control bandwidth, the dynamic performance with the SiC-based converter is better (lower peak current and shorter response time).



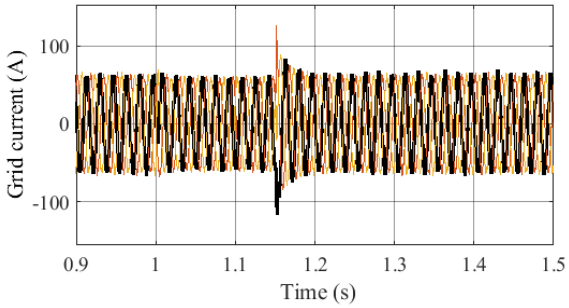

(a) Grid voltage, Si-based



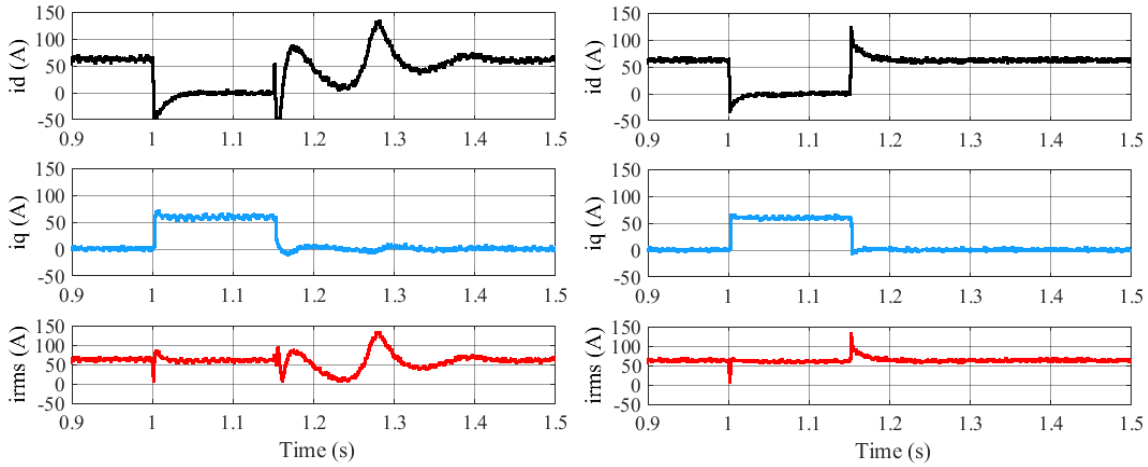

(b) Grid voltage, SiC-based



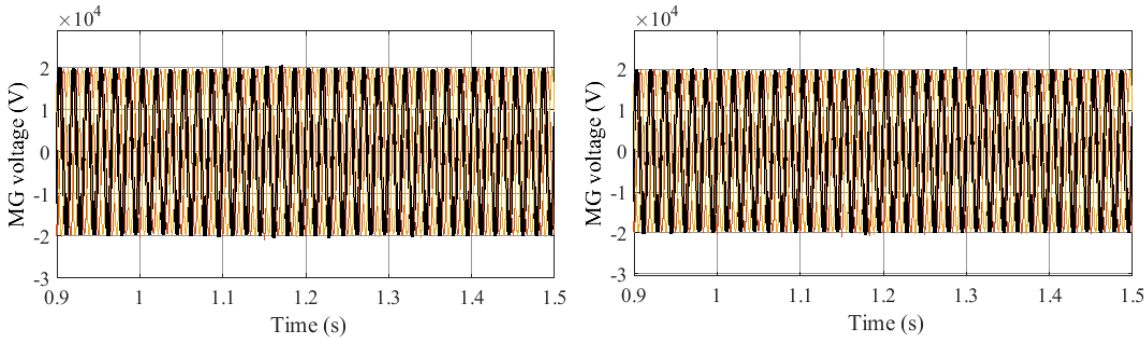

(c) Grid current, Si-based



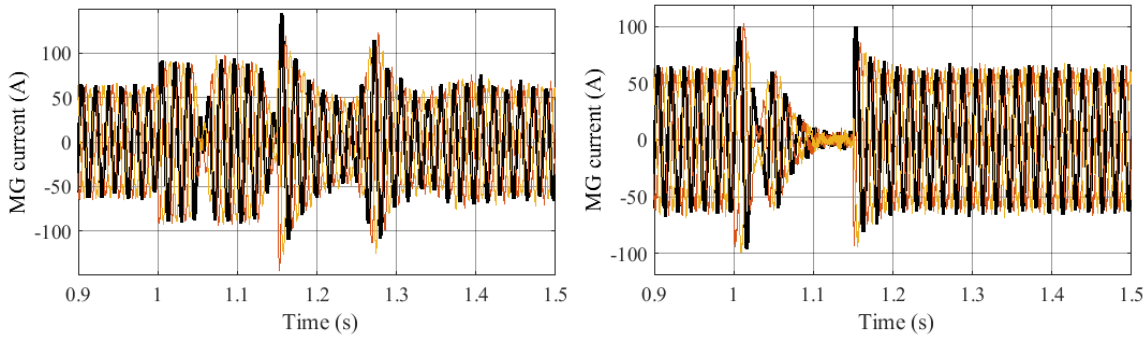

(d) Grid current, SiC-based



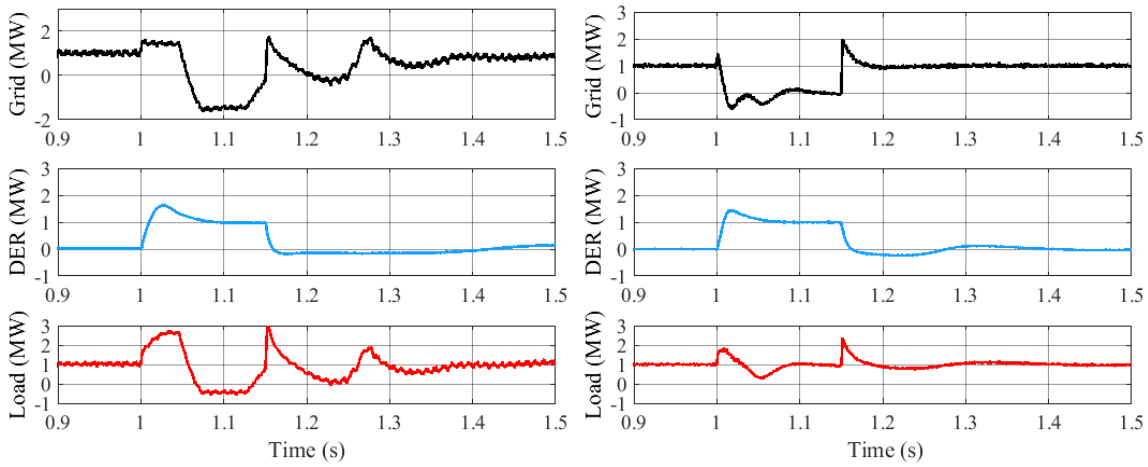

(e) Grid current in DQ coordinates, Si-based (f) Grid current in DQ coordinates, SiC-based




(g) Microgrid PCC voltage, Si-based (h) Microgrid PCC voltage, SiC-based




(i) PCS current on microgrid side, Si-based (j) PCS current on microgrid side, SiC-based




(k) Power sharing, Si-based (l) Power sharing, SiC-based

Fig.5-22. LVRT simulation.

### 5.3.4 Transition Between Islanded Mode and Grid-Connected Mode

The transition between islanded mode and grid-connected mode is evaluated in this section. Sometimes the transition occurs on purpose (i.e. intentional islanding) but most of the time, the transition takes place when a utility fault occurs, such as the grid voltage drop as a result of short-circuit fault. With a conventional AC microgrid, when the grid voltage drop is detected, the DER interface converter will attempt LVRT first based on the IEEE Std 1547-2014. After the LVRT period, the microgrid can be disconnected and operates in islanded mode if the fault is not cleared. There is one obvious drawback with the conventional AC microgrid during mode transition: The load operates abnormally due to the voltage drop during the LVRT period. In the asynchronous microgrid with PCS, during the transition period, the microgrid is isolated from the utility and the load voltage can be maintained.

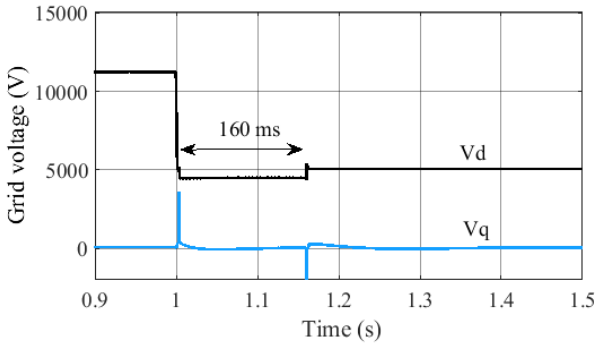
To assess the above-mentioned benefit for the asynchronous microgrid with SiC-based PCS, simulation is carried out for three cases: 1) without the asynchronous MG PCS; 2) with the Si-based PCS; 3) with SiC-based PCS. The simulation parameters are listed in Table 5-20.

Table 5-20. Simulation cases for mode transition

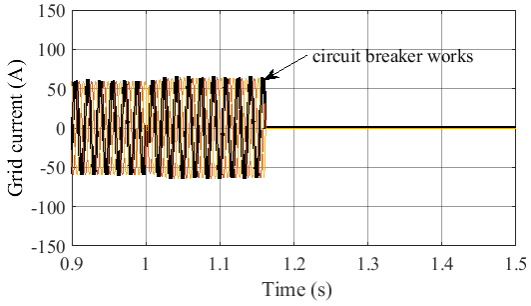
| | **Case 1: without PCS** | **Case 2: Si-based PCS** | **Case 3: SiC-based PCS** |
|---|---|---|---|
| Converter type | Si-based (BESS, PV) | Si-based (PCS, BESS, PV) | SiC-based (PCS)<br>Si-based (BESS, PV) |
| Switching frequency | 3 kHz (BESS, PV) | 1 kHz (PCS)<br>3 kHz (BESS, PV) | 10 kHz (PCS)<br>3 kHz (BESS, PV) |
| Current control bandwidth | 300 Hz (BESS, PV) | 100 Hz (PCS)<br>300 Hz (BESS, PV) | 1 kHz (PCS)<br>300 Hz (BESS, PV) |
| Load | 50% active rectifier, 50% resistive | | |

The simulation results with PCS and without PCS are shown in Fig.5-23 and Fig.5-24. The operation steps with the PCS during the transition period are, as follows: 1) Operation in grid-connected mode until

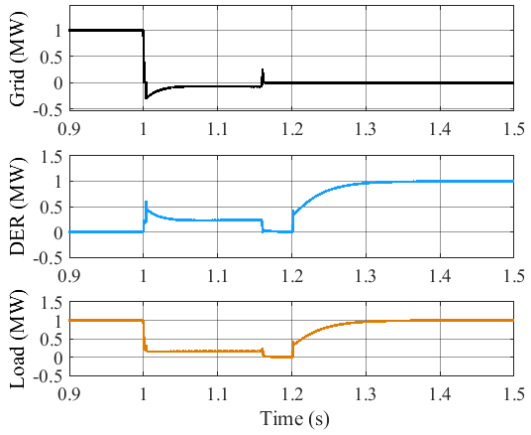
the grid voltage starts to drop (1.0 s); 2) The grid voltage drop (45% of rated voltage) is detected. The microgrid PCS converter on grid side VSC1 transitions from rectifier mode to LVRT mode and supplies 1.0 p.u. reactive current. The converter on the microgrid side VSC2 transitions from droop control to rectifier mode such that the DC-link voltage of microgrid PCS can be maintained; 3) After 160 ms, if the grid voltage is not recovered, VSC1 is shut down and the microgrid is disconnected. Without the PCS, all the DER interface converters in the microgrid have to transition from droop control to LVRT mode and the load will withstand low voltage in step 2. With the PCS, a seamless transition between grid-connected mode and islanded mode can be achieved. The PCC voltage in the microgrid can be maintained and the load is supplied normally. The dynamic performance of SiC-based PCS is better than the Si-based counterpart due to the high control bandwidth (lower peak current and shorter response time).




(a) Grid voltage

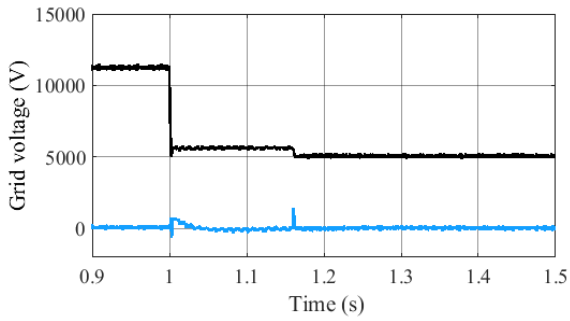



(b) Grid current

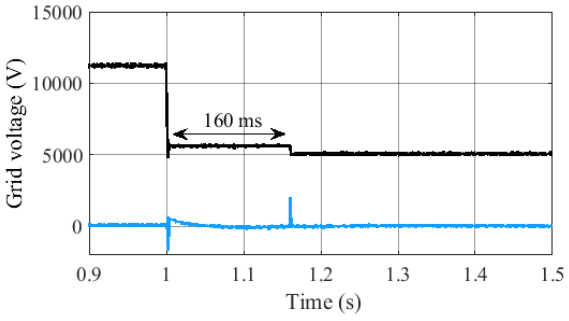



(c) Active power sharing

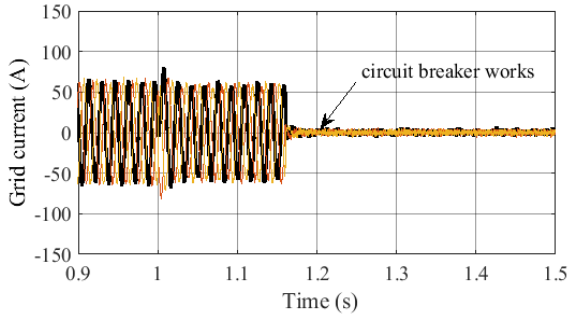
Fig.5-23. Transition simulation without PCS.



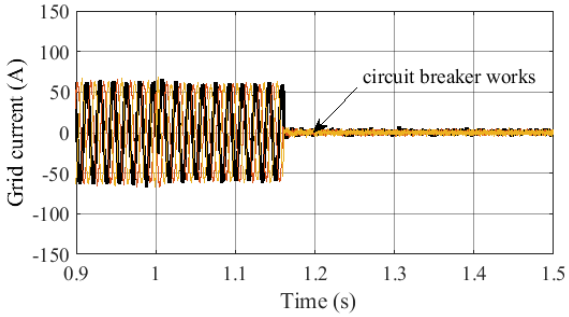

(a) Grid voltage, Si-based



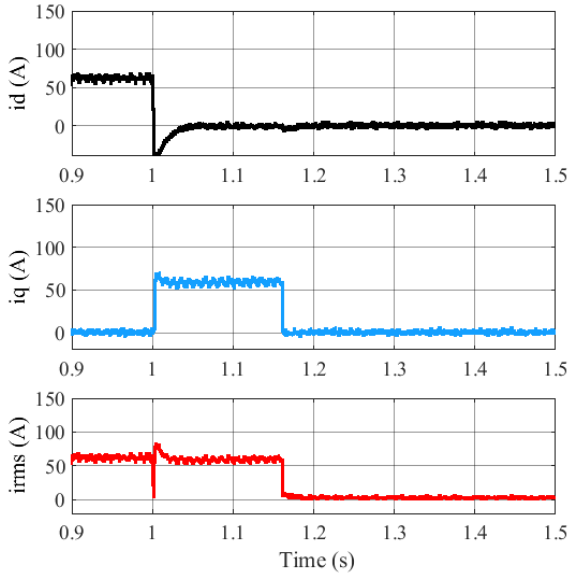

(b) Grid voltage, SiC-based

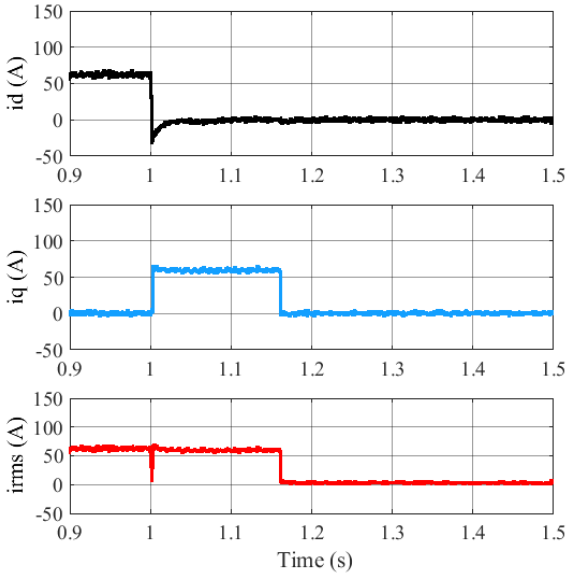



(c) Grid current, Si-based

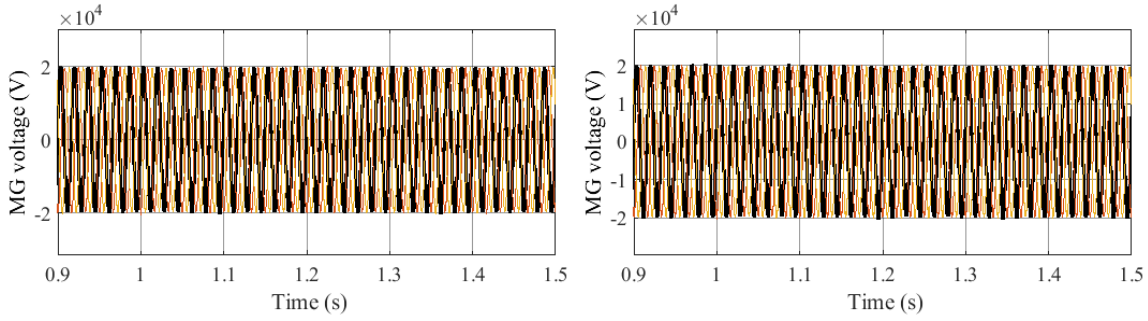



(d) Grid current, SiC-based

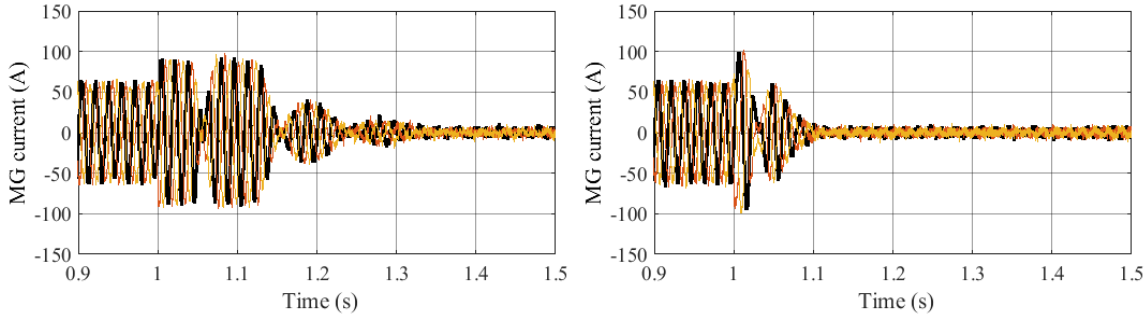


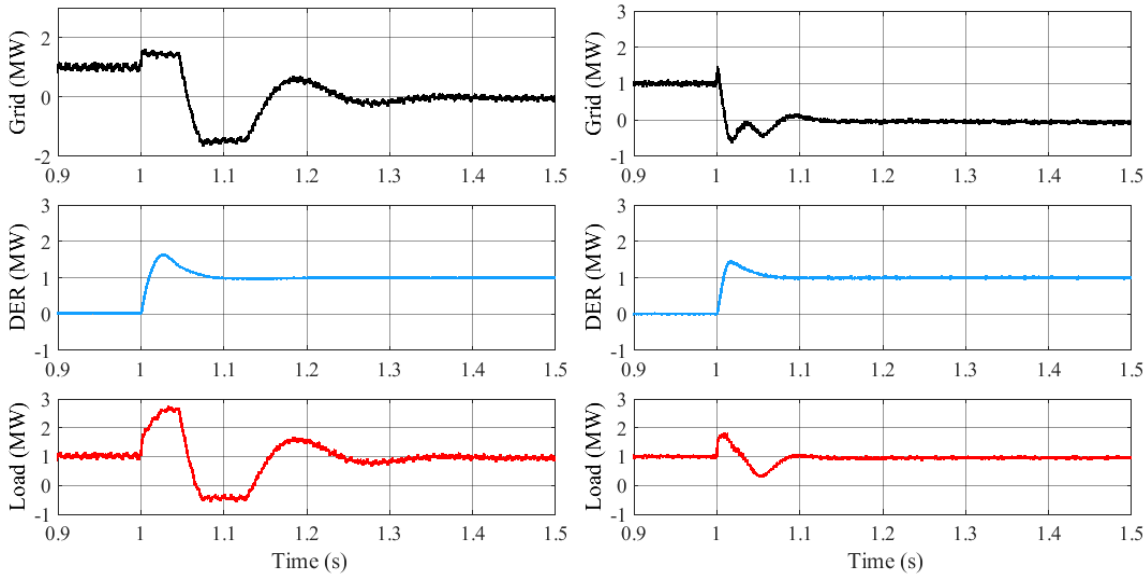

(e) Grid current in DQ coordinates, Si-based (f) Grid current in DQ coordinates, SiC-based




(g) Microgrid PCC voltage, Si-based (h) Mirogrid PCC voltage, SiC-based




(i) PCS current on microgrid side, Si-based (j) PCS current on microgrid side, SiC-based




(k) Power sharing, Si-based (l) Power sharing, SiC-based

Fig.5-24. Transition simulation with PCS.

### 5.3.5 Black Start

The black start is the procedure of restoring an electric power station or a part of an electric grid to operation without relying on an external network. With or without the asynchronous microgrid PCS, the microgrid is required to have black start capability based on IEEE Std 1547. First, the microgrid should

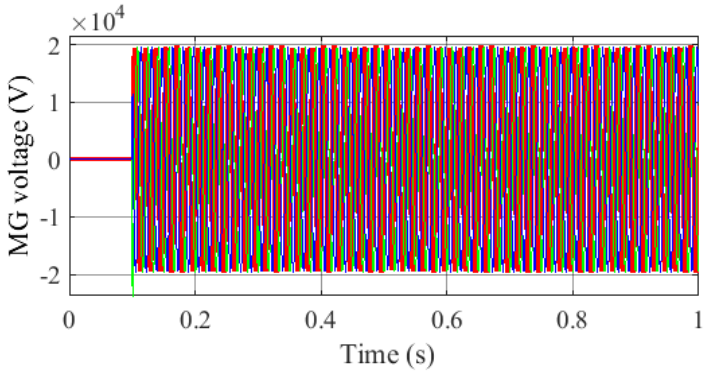
perform a black start internally during islanded operation for local service restoration. Then the microgrid can reconnect to the utility grid.

To evaluate the black start performance, three cases are simulated: 1) Case 1: without the asynchronous microgrid PCS; 2) with the Si-based PCS; 3) with SiC-based PCS. The case parameters are in Table 5-21.

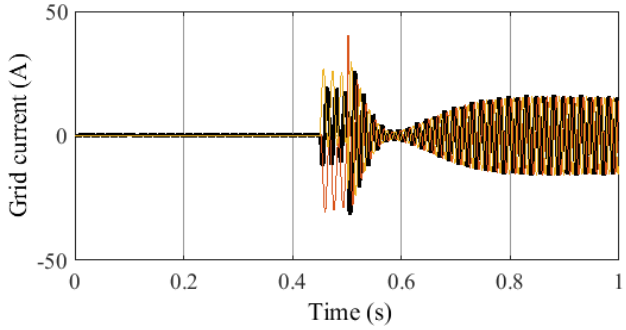
Table 5-21. Simulation cases for black start

| | **Case 1: without PCS** | **Case 2: Si-based** | **Case 3: SiC-based** |
|---|---|---|---|
| Converter type | Si-based (BESS, PV) | Si-based (PCS, BESS, PV) | SiC-based (PCS)<br>Si-based (BESS, PV) |
| Switching frequency | 3 kHz (BESS, PV) | 1 kHz (PCS)<br>3 kHz (BESS, PV) | 10 kHz (PCS)<br>3 kHz (BESS, PV) |
| Current control bandwidth | 300 Hz (BESS, PV) | 100 Hz (PCS)<br>300 Hz (BESS, PV) | 1 kHz (PCS)<br>300 Hz (BESS, PV) |
| Load | 50% active rectifier, 50% resistive | | |

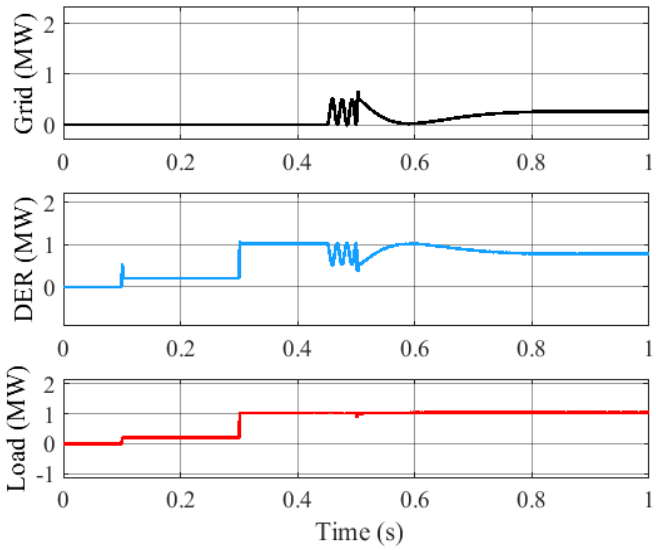
The simulation results of black start with and without the PCS are shown in Fig. 5-25 and Fig. 5-26. The black start steps without microgrid PCS are as follows: 1) Build up the PCC voltage in the microgrid by BESS (0.1s); 2) PV system is put into operation and the load in the microgrid is powered (0.3s); 3) Synchronize the voltage and phase of the microgrid with the utility and connect them (0.45s); 4) Transition to grid-connected mode (0.5s). With the microgrid PCS, the black start steps are: 1) Build up the PCC voltage in the microgrid by BESS (0.1s). The PCS DC-link voltage is established by microgrid side converter VSC2; 2) PV system is put into operation and the load in the microgrid is powered (0.3s); 3) Synchronize (from 0.2s to 0.45s) with the utility using grid side PCS converter VSC1; 4) Transition to grid-connected mode (0.5s). The black start with microgrid PCS is easier because the resynchronization can be completed only with VSC1. The dynamic performance with SiC-based MG PCS is better than Si-based due to the higher control bandwidth (lower peak current and shorter response time).




(a) PCC voltage in microgrid

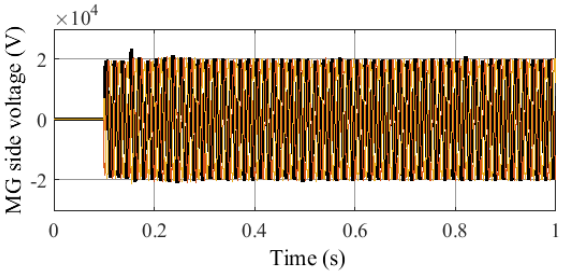



(b) Grid current

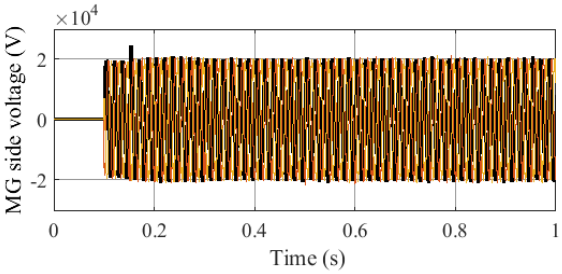



(c) Active power sharing

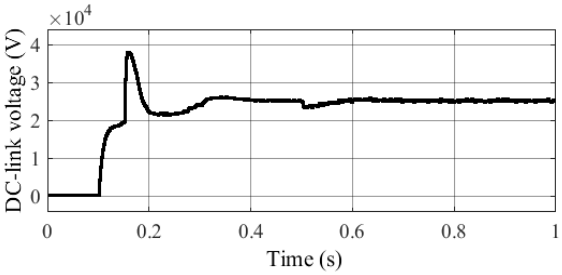
Fig.5-25. Black start simulation without PCS.



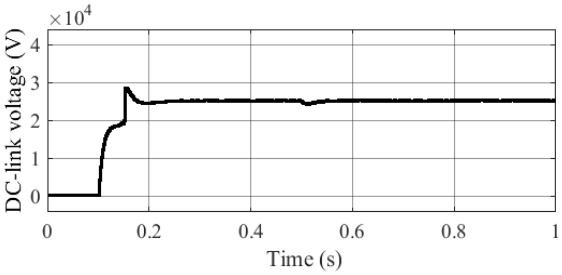

(a) PCC voltage in microgrid, Si-based



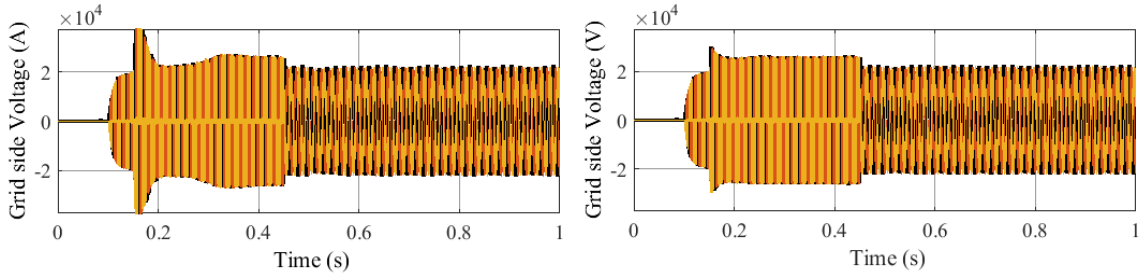

(b) PCC voltage in microgrid, SiC-based




(c) DC-link voltage of PCS, Si-based



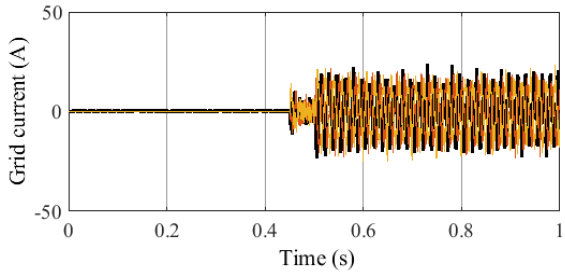

(d) DC-link voltage of PCS, SiC-based



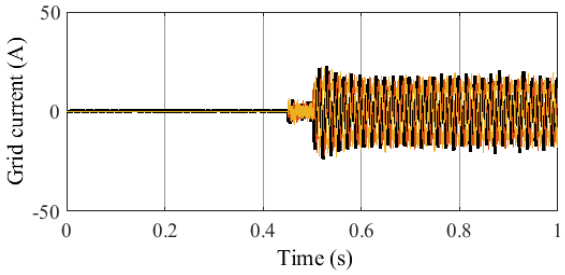

(e) Grid side voltage, Si-based



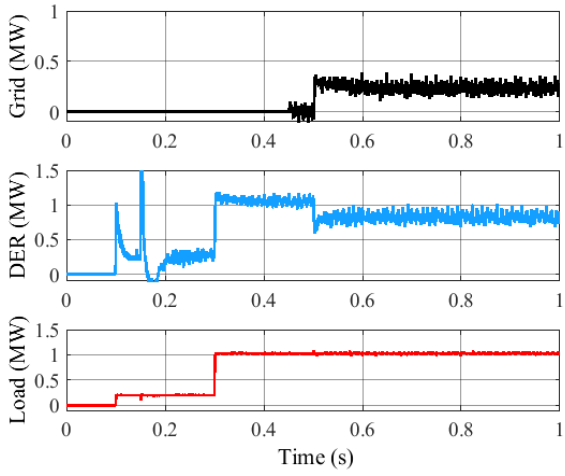

(f) Grid side voltage, SiC-based



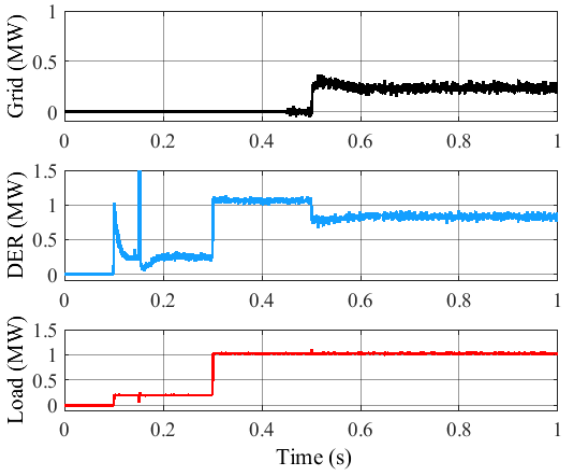

(g) Grid side current, Si-based




(h) Grid side current, SiC-based




(i) Active power sharing, Si-based




(j) Active power sharing, SiC-based

Fig.5-26. Black start simulation with PCS.

## 5.4 CONCLUSION

The benefits of using HV SiC in asynchronous microgrid PCS are evaluated and benchmarked both at the converter level and system level. At the converter level, the SiC-based PCS has significant benefits in weight and size (83% weight reduction and 81% size reduction with SiC-based three-level NPC, 60% weight reduction and 67% size reduction with SiC-based MMC, compared with a Si three-level NPC, even without considering low-frequency transformers), and even in efficiency if 10 kHz switching frequency is selected (46.6% loss reduction with SiC-based three-level NPC and 31.8% reduction with SiC-based MMC).

The SiC-based PCS converters can work with a higher switching frequency (around 10 to 20 times higher than Si-based PCS converters), and therefore have a higher control bandwidth. At the system level, the benefits in enhanced power quality, enhanced system stability, LVRT, transition between islanded mode and grid-connected mode, and black start are evaluated through simulation. On power quality, SiC-based

PCS can have integrated harmonic filtering capability and therefore eliminate the need for additional harmonic filters (e.g. saving an APF that can be 14% of the PCS converter or load rating). On stability, the SiC PCS can isolate the impact of the grid impedance and enhance the system stability in grid-connected mode, and operates as a stabilizer to enhance the stability in islanded mode. On LVRT, mode transition between grid-connected and islanded modes and black start, with the PCS, the load in the microgrid can be supplied normally even in LVRT and mode transition periods and the black start can be easier. With the SiC-based PCS with much higher control bandwidth, better dynamic performance during LVRT, mode transition, and black start can be achieved, compared with the Si-based PCS.

# 6. HV SIC-BASED PCS CONVERTER DESIGN CONSIDERING GRID REQUIREMENTS

In previous sections, converters are benchmark designed without considering grid requirements. However, to increase the system's reliability and provide better grid support services, considering grid requirements in the converter design is necessary. Although some grid requirements have been considered in Si-based converters, there are still some differences between the Si and SiC-based converters, especially HV SiC-based converters. In this chapter, the HV SiC-based PCS converter design considering grid requirements is conducted. By comparing to the baseline design, the impact of grid requirements on the converter design is evaluated. The design approach can also be extended to other converter topologies and applications.

## 6.1 INTRODUCTION

### 6.1.1 System Configuration

The configuration of the flexible combined heat and power (F-CHP) system is shown in Fig. 6-1, and the PCS converter is designed to connect the 850 V LV DC bus to the 13.8 kV AC grid. The PCS converter needs to work in both grid-connected mode and islanded mode. In the grid-connected mode, the PCS converter needs to realize the four-quadrant operation. Also, to increase the system's reliability, it needs to keep operating during grid transients. Therefore, grid requirements need to be considered in the converter design. In the islanded mode, since the MV AC grid is unavailable, the PCS converter could be required by the grid manager to form the MV AC voltage and frequency, supporting the external balanced or unbalanced AC loads.

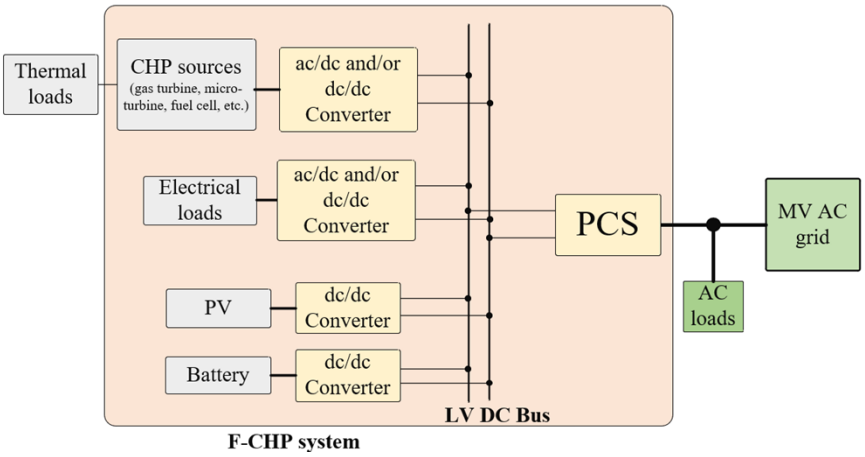



Fig. 6-1. The system configuration for the F-CHP system.

### 6.1.2 Converter Design Requirements

The PCS converter topology is shown in Fig. 6-2. It is a SiC-based, modular, transformer-less (i.e. no 60 Hz transformers), three-phase four-wire DC/AC PCS converter. It consists of a DC/DC stage and a DC/AC stage. The DC/DC stage boosts the LV DC to MV DC and realizes galvanic isolation, and the DC/AC stage converts the MV DC to MV AC and interfaces with the MV AC grid. The rated voltage for the LV DC bus is 850 V, and 1.7 kV SiC MOSFETs are used. The MV DC voltage is determined by the design, and 10 kV SiC MOSFETs are used.

Design specifications and requirements of the PCS converter are shown in Table 6-1. The converter power rating is 1 MW, and the efficiency needs to be 98%. The LV DC voltage needs to consider 5% voltage variation, and the MV AC grid voltage needs to consider -12% and +10% variation based on the normal 13.8 kV grid voltage range. The PCS converter needs to achieve the four-quadrant operation. The control bandwidths of the AC voltage and current are required to be 300 Hz and 1 kHz, respectively.

Many grid requirements need to be met. Based on IEEE Std 1547-2018, the PCS converter needs to meet the power quality, voltage ride-through, and frequency ride-through requirements. Besides, to increase the system stability and realize the system functions, some other requirements, such as grid faults, unbalance operation, and transient operation, need to be achieved.

The scope of this work is the DC/AC stage of the PCS converter. Since grid requirements mainly impact the DC/AC stage design, and the MV DC-link decoupled the DC/DC stage from the DC/AC stage, the DC/DC stage will not be discussed in the work except for some impact also transferred to the DC/DC stage.

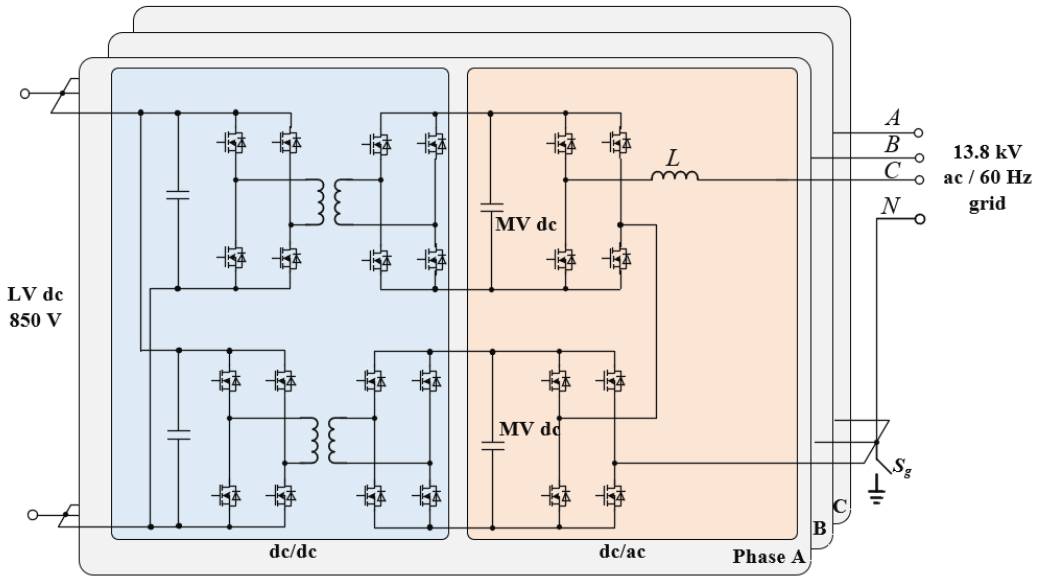



Fig. 6-2. The PCS converter topology.

Table 6-1. The PCS converter design specifications and requirements.

| | | |
|---|---|---|
| Converter design parameters | Power rating | 1 MW |
| | LVDC voltage rating | 850 V (±5%) |
| | MVAC grid voltage rating | 13.8 kV (-12% ~ 10%) |
| | MVAC grid frequency | 60 Hz (±1.2 Hz) |
| | Efficiency | 98 % |
| | Power factor | Four-quadrant operation |
| | Ambient temperature | -25 ºC ~ 35 ºC |
| | Cooling | Water cooling/Forced air |
| | Voltage control bandwidth | >300 Hz |
| | Current control bandwidth | >1 kHz |

| | | |
|---|---|---|
| Grid requirements | IEEE Std 1547 | ▪ 5% TDD in MVAC-side current<br>▪ Low/high voltage ride through<br>▪ Low/high frequency ride through |
| | Other system requirements | ▪ MVAC grid faults<br>▪ MVAC grid unbalance operation<br>▪ 33% unbalance load support in the islanded mode<br>▪ Lightning and switching transient |

## 6.2 BASELINE DESIGN

To understand the impact of grid requirements on the converter design, a converter baseline design is conducted first. In the baseline design, only the grid-side current harmonic requirement (TDD<5%) is considered, and other grid requirements in Table 6-1 are not considered.

### 6.2.1 Device

Considering the converter control bandwidth requirements, the switching frequency is selected at 10 kHz. To meet the overall converter efficiency requirement, i.e. 98%, the DC/AC stage is designed to have an efficiency of 99%. Then, three 10 kV/300 mΩ SiC MOSFET dies are paralleled at each position to get a 10 kV/100 mΩ half-bridge power module. The total loss of each device position is 370 W, of which 190 W is the switching loss and 180 W is the conduction loss. Based on the 10 kV SiC half-bridge MOSFET in [180], the scaled 10 kV power module has a junction to the case thermal resistance of 0.13 ºC/W per switch position, dimension of 6.5 cm × 12.5 cm × 2.4 cm, and weight of 0.2 kg. Therefore, for each H-bridge, the device size is 390 $cm^3$, and the weight is 0.4 kg.

### 6.2.2 Device Cooling

Water cooling is used in this 1 MW converter. The thermal resistance of the thermal interface is calculated first. Thermal grease TG-S606C, which has a thermal conductivity of 5 W/(m·ºC), is used. The thickness is assumed to be 100 μm, resulting in thermal resistance of 0.00246 ºC/W. Then, the cold plate surface maximum temperature, considering each H-bridge uses one cold plate, is calculated to be 43 ºC. The ATS-CP-1004 cold plate is used to accommodate two half-bridge modules of each H-bridge. Based on the cold plate capability, the coolant flow rate is determined at 1 GPM. The inlet coolant temperature is calculated to be 33 ºC, and the outlet coolant temperature of each cold plate is 39 ºC. The dimensions of the cold plate are 16.2 cm × 17.2 cm × 2.0 cm, and its weight is 1.1 kg. Therefore, the cold plate size for each H-bridge is 557 $cm^3$, and the weight is 1.1 kg.

### 6.2.3 DC-link Capacitor

Assume the DC-link front source, which is the DC/DC stage in this PCS converter, has high impedance for the $2^{nd}$-order frequency, which can be realized through control if necessary. As a result, all the $2^{nd}$-order

power variation needs to be provided by the DC-link capacitor. Then, the relationship between the DC-link capacitance and the 2nd-order voltage ripple can be derived as

$$C_{dc} = \frac{S}{3N\omega\varepsilon U_{dc}^2} \tag{6-1}$$

where $S$ is the three-phase converter power rating, $N$ is the H-bridge number in each phase; $C_{dc}$ is the DC-link capacitance; $\varepsilon$ is the DC-link peak-to-peak voltage ripple in the percentage of the rated DC-link voltage; $V_{dc}$ is the rated DC-link voltage.

Considering the MV AC grid normal voltage range (-12% ~ +10%), the DC-link voltage of each H-bridge is determined at 6.3 kV. To limit the DC-link voltage ripple at ±5%, the DC-link capacitance is calculated to be 114 μF. The DC-link capacitor RMS current is also calculated based on the converter operation parameters. When the power factor is 0, the DC-link capacitor RMS current has the maximum value of 26 A. Also, the dominant part of the RMS current is the 2nd-order component.

Then, the 2 kV/440 μF film capacitor B25620B1447K983 from TDK is selected. Four capacitors are connected in series to withstand the 6.3 kV DC-link voltage and achieve a total capacitance of 110 μF. It has a current capability of 80 A, and the power loss and temperature rise of each capacitor is calculated to be 1.7 W and 3.1 ºC, respectively, based on the ESR and thermal resistance provide in the capacitor datasheet. Therefore, this capacitor can withstand the current. The overall capacitor size in each H-bridge module is 11,412 cm$^3$, and the total weight is 11.4 kg.

### 6.2.4 Filter Inductor

The filter inductor is sized based on the MV AC grid-side current harmonic requirements. According to the simulation result, 4.4 mH (0.009 p.u.) inductance is needed, and the current RMS and peak values are 44 A and 66 A, respectively. Considering the core loss caused by high-frequency current ripples, an amorphous core is used. The inductor electrical design results are shown in Table 6-2. As used in the 13.8 kV grid, based on IEC 60071-1, the inductor insulation requirement needs to consider several conditions, as shown in Table 6-3.

Table 6-2. The inductor basic design results.

| | |
|---|---|
| Inductance | 4.4 mH |
| Current RMS value | 44 A |
| Current peak | 66 A |
| Core material | Amorphous |
| Core size | AMCC1000 × 2 |
| Winding turn number | 60 |
| Wire gauge | AWG #5 |
| Air gap | 4.8 mm |
| Wire loss | 52 W |
| Core loss | 48 W |

Table 6-3. The inductor insulation requirements.

| Condition | Voltage |
|---|---|
| Steady-state operation | 12.6 kV |

| | |
|---|---|
| Low-frequency short-term insulation capability | 31 kV |
| Lightning surge | 95 kV |

As shown in Fig. 6-3, the inductor winding is wound on a bobbin, and 60 turns are divided into 4 layers with 15 turns in each layer. The insulation between winding layers is based on Dupont Nomex 410 paper. The core is set in an aluminum container, so they have the same voltage potential. Then the whole inductor is potted with epoxy in the container, and the container is grounded. Therefore, the insulation between the winding and the core/container is realized by epoxy. To determine the thickness of the Dupont paper and the distance between the winding and the core/container, the voltage stress, and the material electrical strength have to be understood first. As shown in Table 6-4, the turn-to-turn and the layer-to-layer insulations mainly consider the steady-state operation, while the winding-to-core insulation needs to consider all conditions. The dielectric strength of insulation materials is shown in Table 6-5. Although Dupont paper has a much higher dielectric strength for the lightning surge, the continuous operation value is only 1.6 kV/mm to avoid partial discharge. Epoxy has a 6 kV/mm dielectric strength for continuous operation, and a time factor of 0.45 can be considered for lightning surge, so it is 13.33 kV/mm. Therefore, considering the worst case, the Dupont paper thickness between winding layers needs to be 1.31 mm, and the distance between the winding and the core/container needs to be 7.13 mm.

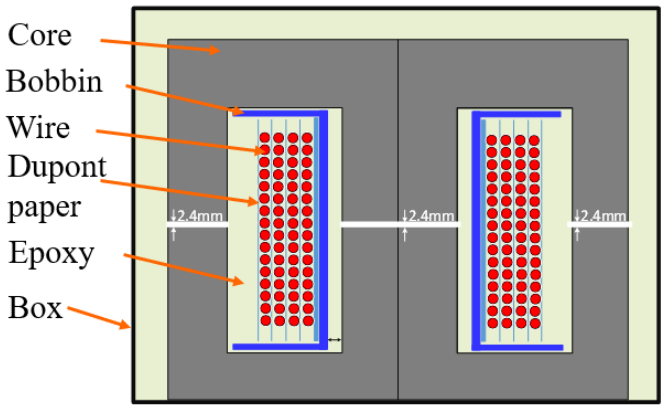



Fig. 6-3. Inductor insulation design.

Table 6-4. The inductor voltage stresses.

| Conditions | Voltage stress between adjacent turns in the same layer | Voltage stress between adjacent turns in different layers | Voltage stress between winding and core/container |
|---|---|---|---|
| Lightning | / | / | 95 kV |
| Short term | / | / | 31 kV |
| Steady state | 110 V | 2.1 kV | 12.6 kV |

Table 6-5. Dielectric strength of insulation materials.

| Conditions | Dupont Nomex 410 paper | Epoxy |
|---|---|---|
| Lightning | 50 kV/mm | 13.33 kV/mm |
| Short-term | 30 kV/mm | 6 kV/mm |
| Long-term | 1.6 kV/mm | 6 kV/mm |

Then, the thermal simulation was conducted through Ansys/Icepak, and the temperature distribution is shown in Fig. 6-4. The hot spot is located in the winding, and it has a temperature of 104 ºC. Since the ambient temperature in the simulation is 20 ºC, the temperature rise is 84 ºC. The core, which is capable to operate at a maximum working temperature of 155 ºC, is the maximum temperature limitation of the inductor materials. Considering the maximum ambient temperature of 35 ºC, the maximum allowed temperature rise could be up to 120 ºC. Considering at least a 20 ºC margin for uneven loss distribution and loss estimation discrepancy, the inductor temperature rise in simulation needs to be limited to 100 ºC. Therefore, the designed inductor can meet the thermal requirement. Although there is still some thermal margin, further reducing the wire size or core size cannot shrink the inductor size too much since the insulation space cannot be reduced. Therefore, each inductor has a size of 6,447 $cm^3$ and a weight of 23.2 kg.

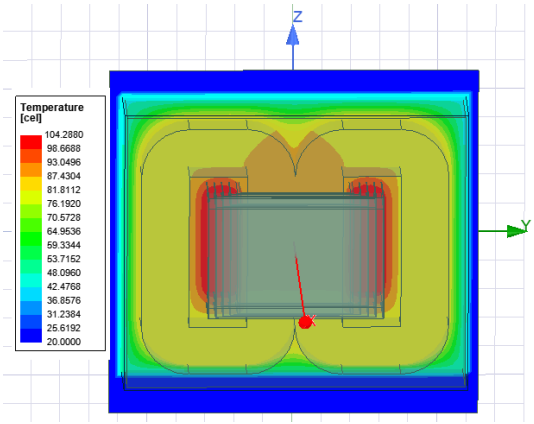


Fig. 6-4. Baseline inductor thermal simulation result.

### 6.2.5 Pre-charge Circuit

A larger pre-charge resistance can achieve a smaller pre-charge current but a longer pre-charge process. Neglecting the power loss on the DC-link voltage balancing and voltage sampling resistors, the total energy transferred through the resistor to the DC-link capacitors is constant, which equals the total energy stored in the DC-link capacitors. A smaller pre-charge resistance results in a shorter pre-charge period but a larger transient and average resistor power loss. Considering the average power rating and pre-charge time, the pre-charge resistor is selected at 10 kΩ. The pre-charge time is around 10 seconds, and the average power rating of the pre-charge resistor should be larger than 281 W. The resistor TAP600K10KE, which has a power rating of 600 W is selected. It has a continuous dielectric strength of 6 kV RMS, and a short-term (1 min) of 12 kV RMS, so it can meet the PCS converter requirement. The size and weight of the pre-charge resistor are 125 $cm^3$ and 0.5 kg, respectively. The relay used to bypass the pre-charge resistor needs to consider both the insulation capability and the current rating. A double pole single throw relay, named RL 38-h, is selected. It has an insulating voltage of 10 kV AC, and a current rating of 30 A per pole. To meet the converter current rating, the two poles can be connected in parallel, then a total of 60 A can be achieved. The size and weight of each relay are 1,250 $cm^3$ and 2 kg, respectively.

### 6.2.6 Arrester

Arresters are installed at the MV AC side terminals to protect the converter from lightning or switching transient surges. The arrester selection is commonly based on the system voltage level. the SIEMENS arrester 3EK7 120-3AC4 is selected. It has a size of 3,030 cm3 and a weight of 1.85 kg.

### 6.2.7 Gate Drive and Gate Driver Power Supply

The gate driver (GD) and gate driver power supply (GDPS) are not designed, instead, they are leveraged from [181] and [182]. Although these gate driver and gate driver power supply are designed for the 10 kV/300 mΩ SiC MOSFET, the size and weight should not change too much after modifying for the scaled 10 kV SiC MOSFET half-bridge module.

### 6.2.8 Baseline Design Summary

The component size and weight summary of the three-phase DC/AC converter baseline design are shown in Fig.6-5 and Fig.6-6, respectively. The H-bridge DC-link capacitor dominates the converter size, followed by the filter inductor. However, the filter inductor has a larger weight than the DC-link capacitor. The total size of the considered components is around 126 L, and the total weight is 173 kg.

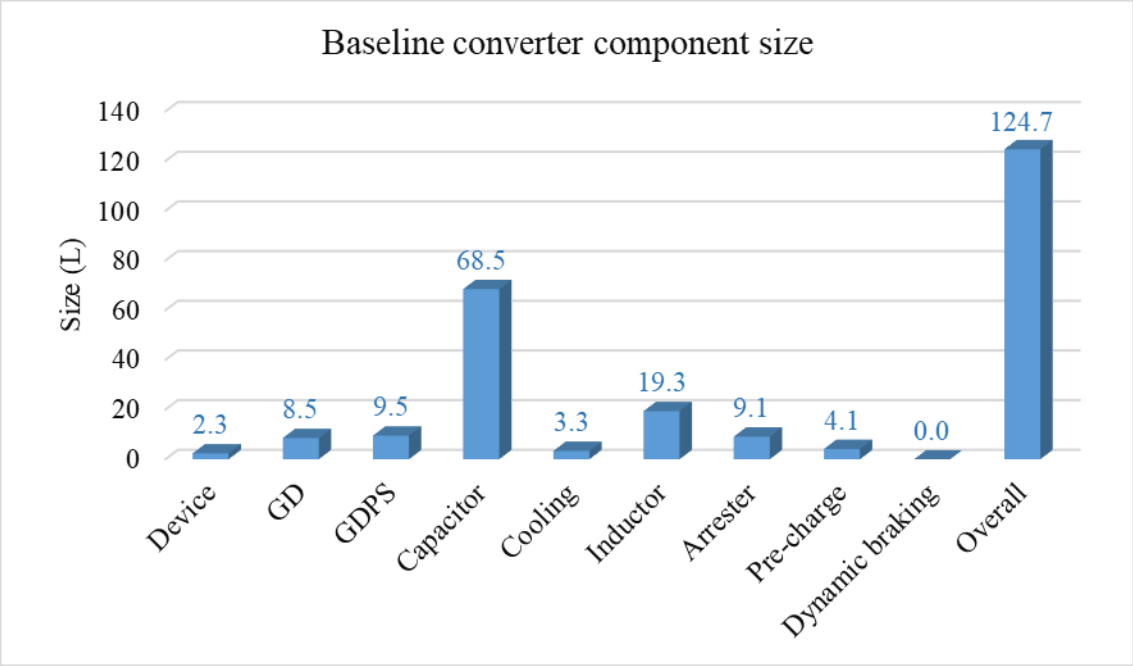



Fig. 6-5. Component size summary of the DC/AC converter baseline design.

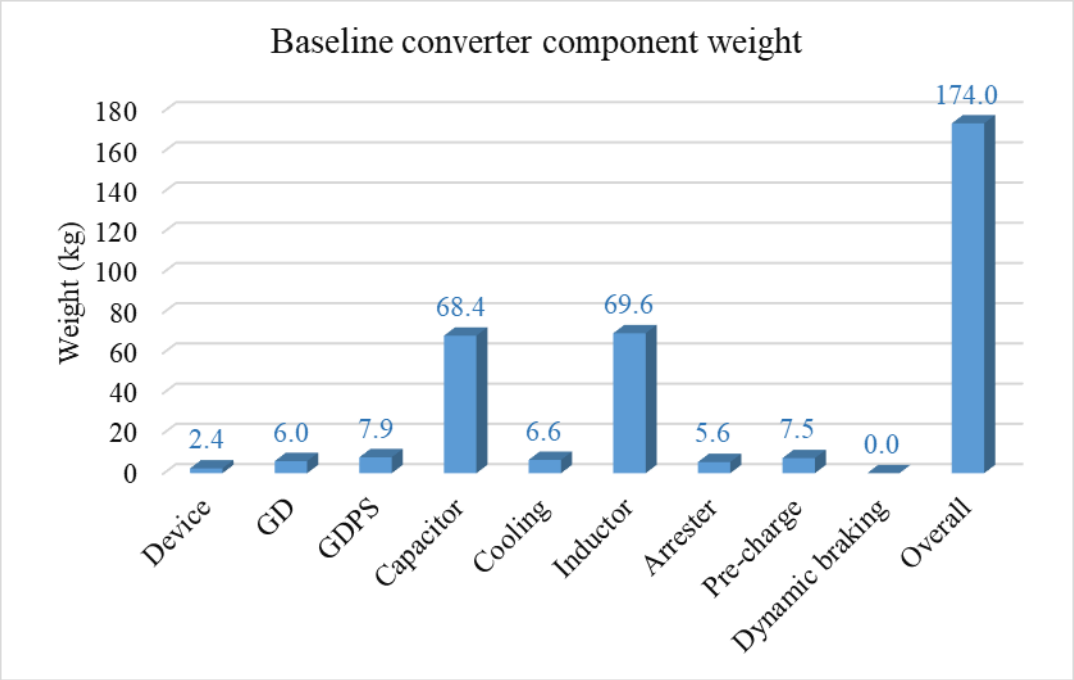


Fig. 6-6. Component weight summary of the DC/AC converter baseline design.

## 6.3 CONVERTER DESIGN CONSIDERING GRID REQUIREMENTS

### 6.3.1 Voltage Ride Through

IEEE Std 1547-2018 requires the low voltage ride-through (LVRT) and high voltage ride-through (HVRT) capability of distributed energy resources. This work also refers to this standard. There are three operation performance categories, and their LVRT and HVRT range and duration are different. Category III has the widest voltage ride-through range and longest time duration, while category I has the narrowest range and the shortest duration. In category III. The continuous operation range is [0.88 p.u., 1.1 p.u.]. It requires the DER to keep operating at the voltage range of [0.5 p.u., 0.88 p.u.] for 21 seconds. For voltage lower than 0.5 p.u. or higher than 1.1 p.u., it is not mandatory to ride through. The PCS converter, however, is designed to keep working in the continuous range, ride through the whole low voltage range, i.e., [0, 0.88 p.u.], and ride through the high voltage range of [1.1 p.u., 1.2 p.u.]. In the following, the impact of the LVRT and HVRT will be analyzed first, and then design or control methods will be used to make sure the converter can ride through the low or high voltage ranges.

#### 6.3.1.1 The 1st Impact: Inrush Current

As shown in Fig. 6-7, the grid-connected voltage source converter (VSC) has the control process of sampling, calculation, and PWM generation. The converter output power is controlled through the filter inductor current control, and the differential equation of the filter inductor $L$ is

$$v_L = L\frac{di_L}{dt} = v_{PWM} - v_{grid} \tag{6-2}$$

Through sampling the grid voltage, $v_{grid}$, and PLL, the controller obtains the grid amplitude and angle. A voltage reference, $v_{ref}$, is generated by the controller and output through the PWM generation and device switching, to control the inductor current, $i_L$, following the reference. Therefore, knowing the grid voltage information, i.e., amplitude and angle, is critical for the grid-connected converter control.

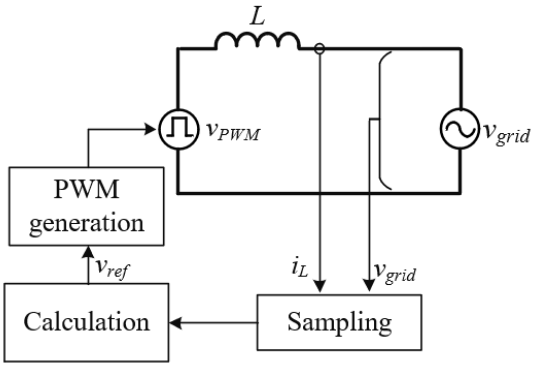



Fig. 6-7. General voltage source converter.

In the steady-state operation, since the inductor is small, the averaged value of the PWM voltage is close to the grid voltage. However, when the grid voltage, $v_{grid}$, has a sudden change, the converter cannot immediately update its output voltage to follow the grid voltage and maintain the inductor current, due to the delays. Then, the voltage difference between the inductor terminals suddenly increases, depending on how large the grid voltage changes. The inductor current will also increase, and an inrush current will occur, which can be estimated as

$$\Delta i_L \approx \frac{v_{grid0} - v_{grid1}}{L} T_d \tag{6-3}$$

where $v_{grid0}$ and $v_{grid1}$ are the grid voltages before the sudden change and after the sudden change, respectively, and $T_d$ is the total delay time, which consists of all the delays in the converter control loop including sampling, calculation, PWM modulation, and device switching.

From (6-3), it can be found that the inrush current is almost proportional to the total delay time, $T_d$, and it is inversely proportional to the filter inductance. Therefore, a larger filter inductance results in a smaller inrush current, and a larger delay time leads to a large inrush current. Increasing the inductance also increases the converter size, weight, as well as cost. Some control methods, such as grid voltage feed-forward control, can speed up the response of the converter to the grid voltage disturbance, but some delays cannot be eliminated.

Assume the grid voltage suddenly changed from 1 p.u. to 0.4 p.u., and the minimum total control delay of $2.5T_s$ is considered. Based on (6-3) the inrush current is

$$\Delta i_L = \frac{\frac{13.8\,\text{kV}}{\sqrt{3}} \times \sqrt{2} \times (1.0 - 0.4)}{4.4\,mH} \times 250\,us = 390\text{A} \tag{6-4}$$

and its per-unit value is

$$\Delta i_{L\_pu} = \frac{\Delta i_L}{I_{base}} = \frac{39\text{A}}{59A} = 6.5\ p.u. \tag{6-5}$$

The simulation has been conducted with Simulink, and the waveforms are shown in Fig. 6-8. When the grid voltage suddenly drops from 1.0 p.u. to 0.4 p.u., an inrush current up to 6.8 p.u. is induced.

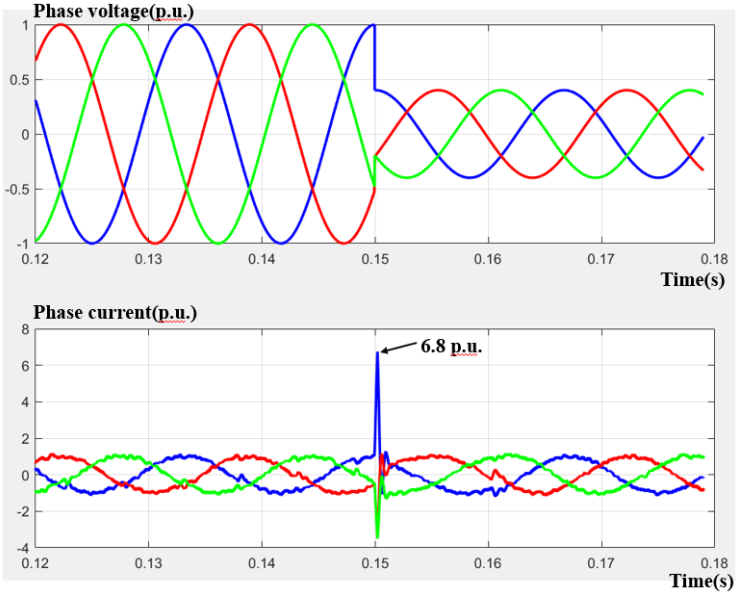



Fig. 6-8. Inrush current caused by grid voltage sudden change without any control.

#### 6.3.1.2 Solution for the Inrush Current: PWM Mask Approach

Increasing the filter inductance could reduce the inrush current, but it also increases the size and cost of the converter. Therefore, a control-based solution is proposed in [183], which is called PWM masked approach. When the phase current is larger than the preset threshold value, the PWM signals in that phase will be temporarily masked. Then, the inrush current flows through the body diodes of the 10 kV SiC MOSFETs, and the converter output voltage will be either the total positive DC-link voltage or negative DC-link voltage depending on the current direction. The polarity of the voltage applied to the inductor will be inverted, and the inductor current starts to decrease. When the current goes down to be lower than the release threshold value, the PWM signals will be released, and the converter goes back to normal control.

Experimental tests based on a small-scale prototype are conducted to verify the approach. As shown in Fig. 6-9, without the PWM mask function, when the grid voltage suddenly changes from 1 p.u. to 0.25 p.u., the inrush current reaches 50 A and 60 A at the moment of grid voltage drop and recovery, respectively. However, with the PWM mask, the inrush current is limited to the preset threshold value, i.e., 25 A. More details can be found in [183]. Therefore, the PWM mask function can effectively limit the inrush current at the trainset of grid voltage change.

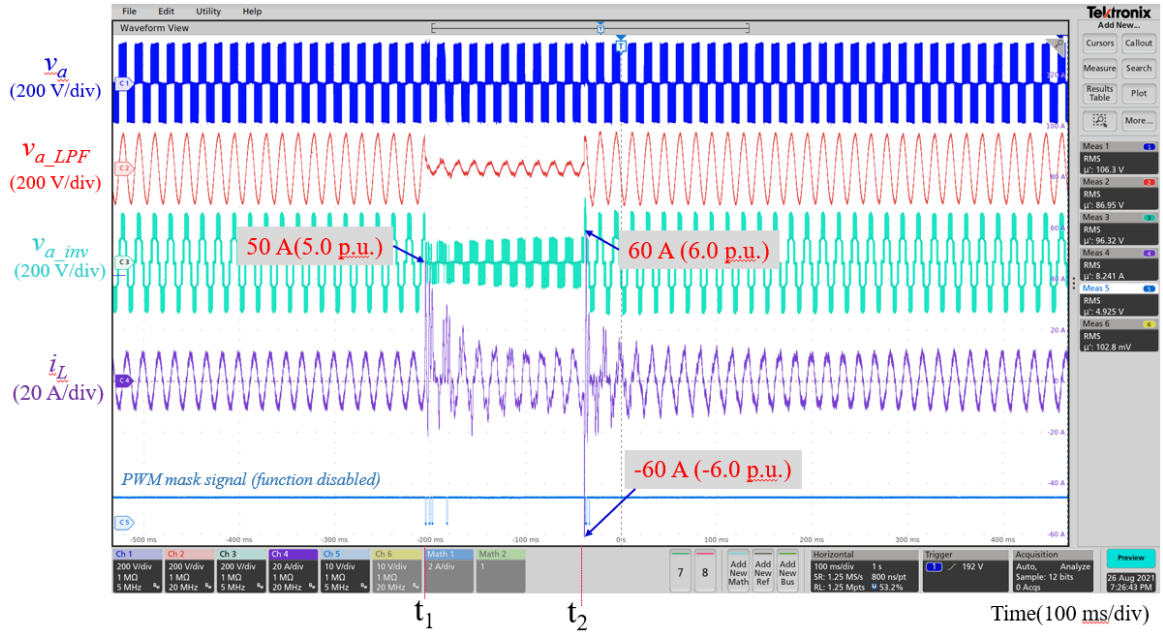



Fig. 6-9. Low voltage ride through waveforms without the PWM mask function.

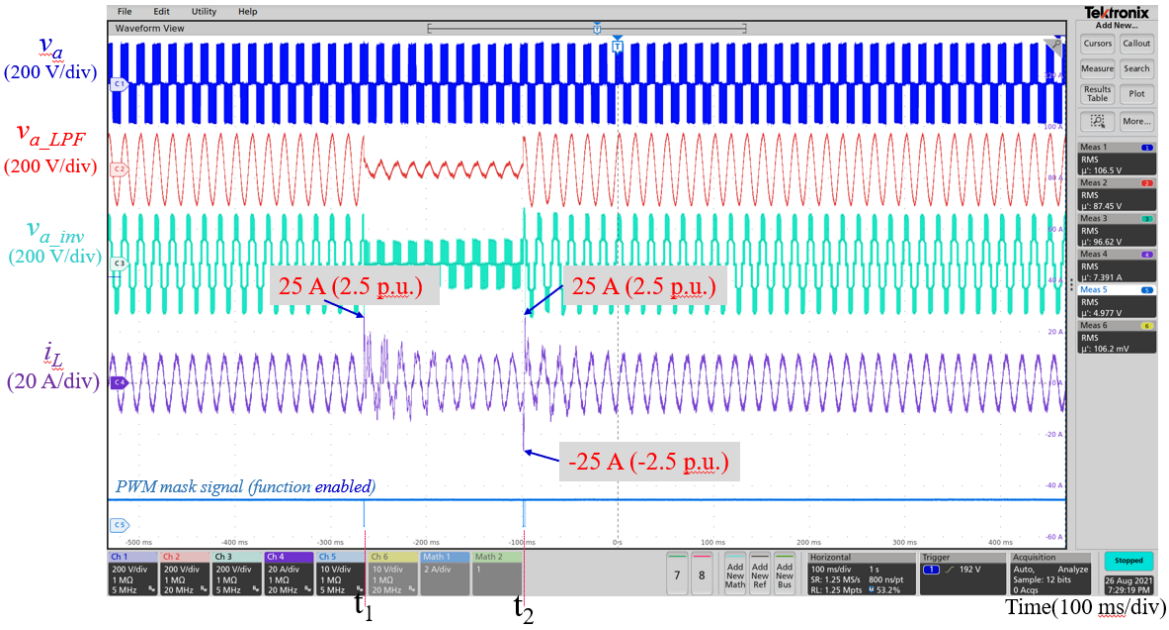



Fig. 6-10. Low voltage ride through waveforms with the PWM mask function.

### 6.3.1.3 The 2nd Impact: Higher DC-link Voltage

For the LVRT, as long as the inrush current is limited with the PWM mask approach, the DC-link voltage variation is small. Also, during the steady state, the DC-link voltage is sufficient to output the AC voltage and the modulation index is lower than one.

However, the grid voltage during HVRT is in the range of [1.1 p.u., 1.2 p.u.]. The DC-link voltage (6.3 kV) of the baseline design, which is selected based on 1.1 p.u. grid voltage, is not sufficient for the 1.2 p.u.

grid voltage. Since the AC filter inductor is small (<0.01 p.u.), the DC-link voltage needed can be estimated as

$$V_{dc} = \frac{\sqrt{2} \times 13.8\,\text{kV} \times 1.2}{\sqrt{3} \times 2} = 6.76\ kV \tag{6-6}$$

To enable the converter to ride through 1.2 p.u. grid voltage, the DC-link voltage is increased from 6.3 kV to 6.67 kV. Although 6.67 kV is lower than the value calculated in (6-6), i.e., 6.76 kV, they are close, and a little bit of modulation saturation is also acceptable especially considering the short period of the ride through. Utilizing 6.67 kV rather than a higher value is mainly considered to limit the device voltage stress. Also, 6.67 kV is the averaged value, with ±5% voltage ripple on the DC-link, the maximum DC-link voltage will be around 7 kV, which is considered to be within the safe operating region of the device.

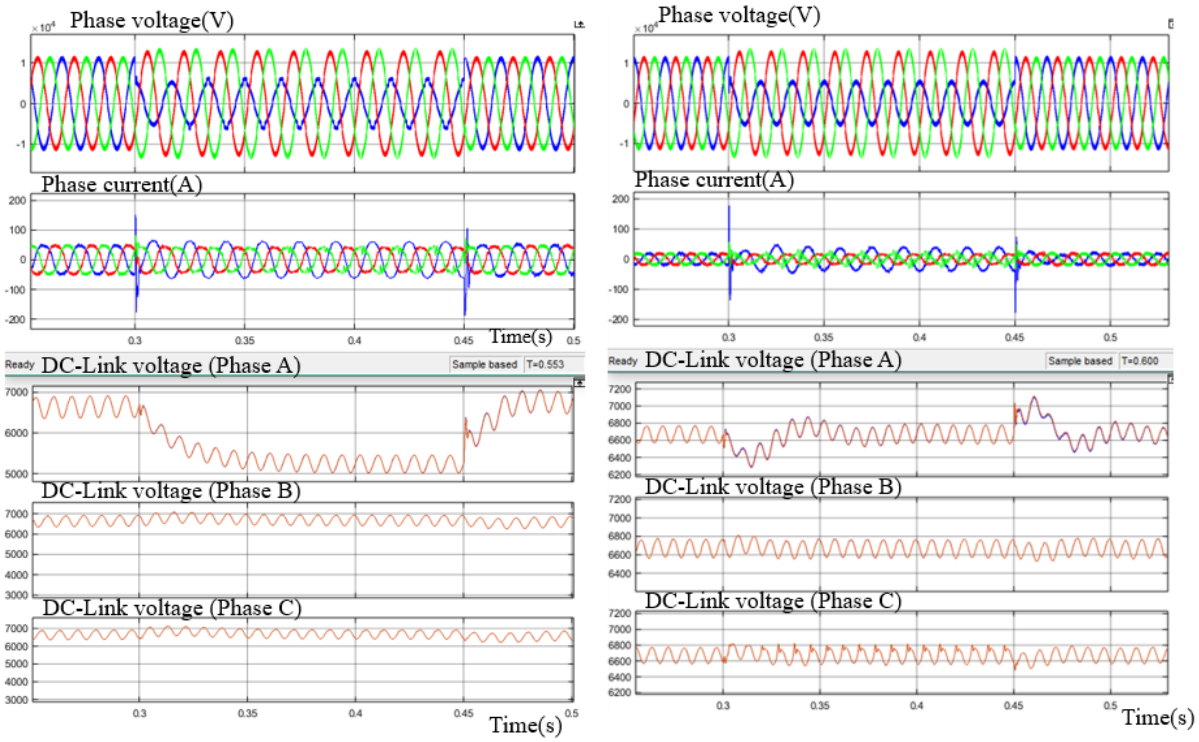
#### 6.3.1.4 The 3rd Impact: Power Delivery

Due to the current limit of the PCS converter, the maximum power that can be delivered by the converter changes with the grid voltage. If the grid voltage decreases, i.e., lower than 1 p.u., the maximum power delivery also drops. If the grid voltage increases, higher than 1 p.u., the maximum power delivery increases. When the DC/AC stage power decreases, if the DC/DC stage keeps delivering the same power during the LVRT period, the DC-link voltage may increase or decrease depending on the power flow direction.

As shown in Fig. 6-11(a), with 300 Ω on each DC-link, the DC/AC stage will deliver the rated power at the steady state. However, at time $t$=0.3 s, voltages of phases A (blue), B (red), and C (green) change from 1 p.u. to 0.5 p.u., 1.15 p.u, and 2 p.u., respectively. The DC-link voltage of phase A decreases at the beginning of the LVRT, and then stays at ~5.2 kV, at where the phase A converter hit its current limit. As a comparison, DC-link voltages of phases B and C do not change since their currents do not reach the limit.

When the resistor on the DC-link changes from 300 Ω to 800 Ω, the power rating before the grid voltage change decreases from 1 p.u. to 0.33 p.u. Then, as shown in Fig. 6-11(b), when the phase A voltage (blue) drops from 1 p.u. to 0.5 p.u., DC-link voltages can still be maintained at the steady state of the LVRT since the maximum power delivery capability of phase A is larger than the power consumption on the DC-link. However, a transient at the beginning of the voltage change is inevitable due to the response time of the converter.

On the contrary, if the DC/DC stage also decreases its power delivery, the LV DC bus voltage will be impacted depending on the power flow direction. If the PCS converter is providing power to the LV DC bus before the LVRT, then during the LVRT period, the LV DC bus voltage may decrease when the PCS converter power delivery decreases. On the other hand, if the PCS converter is absorbing power from the LV DC bus before the LVRT, then the LV DC bus voltage may increase during the LVRT period. If there are other sources, such as large LV DC capacitors or batteries, which can quickly compensate for the LV DC voltage, the LV DC bus can be stabilized within a certain range. Therefore, through control coordination between the DC/DC stage and the DC/AC stage and between the PCS converter and other energy storage/resources, the impact of the LVRT on the power delivery can be reduced.




(a) 300 Ω on the DC-link (b) 800 Ω on the DC-link

Fig. 6-11. Simulation results of the impact of LVRT on power delivery.

#### 6.3.1.5 Impact on the Hardware Design

Based on the above study, the LVRT and HVRT do have some impacts on the converter. Although the inrush current can be effectively limited by the PWM mask method, the inductor design and 10 kV SiC MOSFETs selection still need to consider the limited inrush current, which will be introduced later in this chapter.

The power impact can be reduced through power control coordination, but the higher DC-link voltage requires a higher DC-link capacitor rating. Through (6-1), the capacitance needed to limit the 2nd-order voltage ripple within ±5% is 99 μF. The capacitor voltage rating needs to be higher than 7 kV, considering the voltage ripple. The capacitors used in the baseline design are still used here due to the available product limitation.

### 6.3.2 Grid Faults

#### 6.3.2.1 Design Requirements

Compared to the LVRT and HVRT, the main concern of grid faults is the temporary overvoltage. In the HVRT, the maximum overvoltage considered is 1.2 p.u. When a grid fault happens, however, the overvoltage could be more than 1.2 p.u. The overvoltage induced by grid faults is related to the system grounding. The temporary overvoltage induced by faults in an ungrounded system can be as high as 1.82 p.u., and the overvoltage of a three-phase four-wire system, depending on the grounding configuration and wire configuration, could be between 1.25 p.u. and 1.5 p.u [184].

The temporary overvoltage (>1.2 p.u.) ride through is not required in standards for the grid-connected converter. However, it would be better to keep the converter in operation considering both the converter side and grid side reliability and resilience. Therefore, converter design requirements in terms of faults are:

1) Ride through faults with overvoltage lower than 1.2 p.u. This is similar to HVRT.

2) For faults with overvoltage higher than 1.2 p.u., the converter can temporarily stop operation, but once the grid voltage goes below 1.2 p.u., the converter needs to start operation within a certain time, e.g. 3 seconds.

#### 6.3.2.2 Impacts: Inrush Current and DC-link Overvoltage

When the grid voltage is higher than the overall DC-link voltage, even though PWMs are masked, the inrush current can still flow through the body diode of the MOSFET to charge the DC-link. The acceptable DC-link overvoltage depends on the voltage rating of the device, DC-link capacitor, and DC-link bus bar. Also, for a long-term overvoltage case, the limited inrush current, which is higher than the continuous operation range, is a threat to the device. Therefore, another method needs to be adopted to address the overvoltage issue.

As shown in Fig. 6-12, when grid voltages of phases A (blue), B (red), and C (green) are changed respectively from 1 p.u. to 0.5 p.u., 1.3 p.u., and 1.4 p.u. at time $t$=0.293 s, an inrush current of 4 p.u. occurs at phase C. The converter (both the DC/AC stage and the DC/DC stage) is shut down (PWMs are turned off) by the DC-link overvoltage protection, which is set at 7.5 kV, at the very beginning. However, even though PWMs are off, the inrush current can still flow through the body diode of the 10 kV SiC MOSFET to charge DC-link capacitors, until either the circuit breaker is opened, or DC-link capacitors are fully charged, whichever is realized first. Also, the PWM mask method, which has a threshold value of 3 p.u. does not help to reduce the inrush current of phase C. DC-link voltages in phase C are charged to around 8.9 kV, which is out of the device's safe switching voltage range. After the circuit breaker is opened, which usually takes several or tens of milliseconds, DC-link voltages gradually decrease because of the discharging introduced by voltage balancing resistors in parallel with DC-link capacitors.

A theoretical study is conducted to analyze the maximum overcurrent and the DC-link overvoltage in terms of different fault timing and different converter power factor before the fault, assuming the grid voltage suddenly changes from 1 p.u. to 1.4 p.u. As shown in Fig. 6-13, when the fault happens a little bit before the peak of the voltage waveform, the overcurrent and DC-link overvoltage are the maximum, which are 5 p.u. and 9.18 kV, respectively. The converter power factor has little impact.

Considering the voltage stress of the 10 kV SiC MOSFET, the steady-state DC-link voltage cannot be further increased, so the converter cannot ride through an overvoltage of more than 1.2 p.u. The PCS converter can temporarily stop operation during faults if the overvoltage is higher than 1.2 p.u., and when the grid voltage is recovered, the converter needs to go back to operate within 3 seconds. Then, how to protect the converter from overvoltage during the fault and get the converter back to operate after the fault is cleared is the key challenge that needs to be addressed.

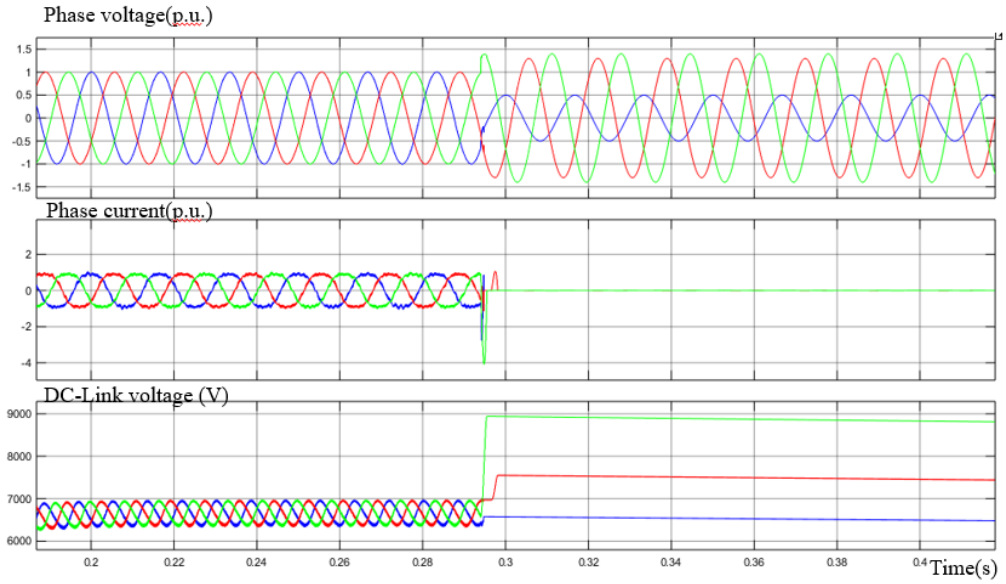



Fig. 6-12. Simulation waveform when a fault happens (voltages of phase A (blue), B (red), and C (green) are changed from 1 p.u. to 0.5 p.u., 1.3 p.u., and 1.4 p.u., respectively).

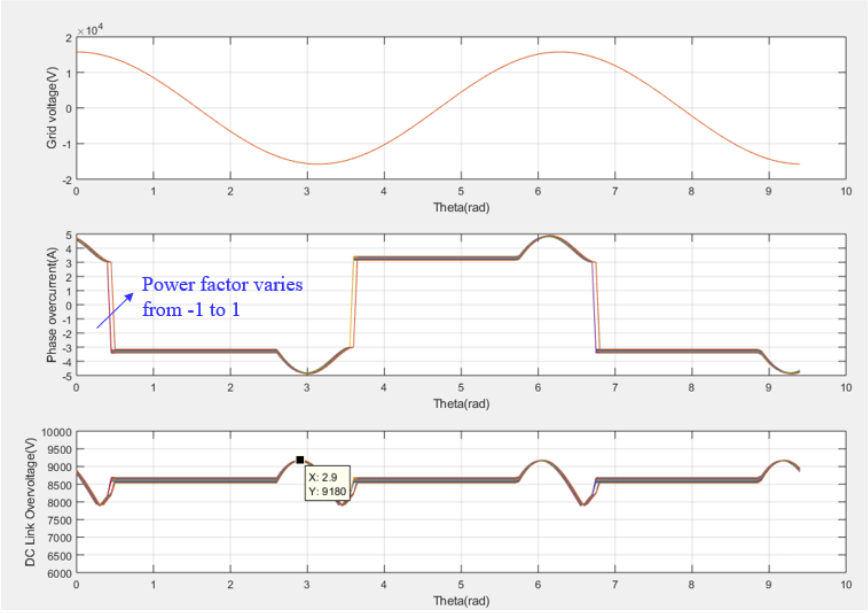



Fig. 6-13. Overcurrent and DC-link overvoltage in terms of different fault timing and converter power factor (@ grid voltage change from 1 p.u. to 1.4 p.u.).

#### 6.3.2.3 Solution: Dynamic Braking Circuit

To discharge the DC-link and limit the overvoltage, an additional dynamic braking circuit is adopted. As shown in Fig. 6-14, it consists of a braking resistor, $R_{braking}$, and a switch $T_{braking}$. The braking resistor needs to be small so that it can discharge the DC-link voltage from 9.2 kV to 7.1 kV within 3 s. The braking switch, which needs to withstand the DC-link voltage, can use either several Si or SiC devices connected in series or use MV SiC devices. Since there is no need for fast switching, the device voltage balancing can be easily realized. Also, the current rating of the braking switching can be very small. For example, selecting the braking resistance to be 10 kΩ so that the DC-link can be discharged within 0.3 s, then the maximum current flow through the braking switching is less than 1 A.

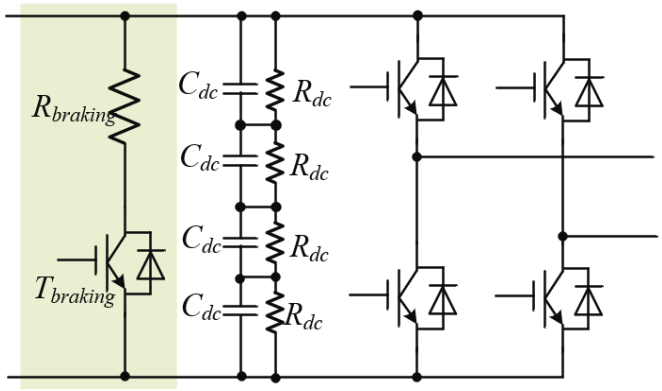



Fig. 6-14. The additional braking circuit on each MV DC-link.

A simulation has been conducted to verify the analysis. As shown in Fig. 6-15, a grid fault happens at time $t=t_1$. As a result, phase voltages of phases A (blue), B (red), and C (green) are changed from 1 p.u. to 0.5 p.u., 1.3 p.u., and 1.4 p.u., respectively. An inrush current of up to 4 p.u. occurs in phase C. To speed up the simulation, the braking resistor is 1 kΩ. Due to the filter inductor, DC-link voltages of phase C are charged to around 8.7 kV, which is higher than the grid voltage peak. The braking switch is controlled to operate when the DC-link voltage is higher than 8.2 kV and to stop operation when the DC-link voltage drops below 8 kV. This control can decrease the DC-link voltage to below 8 kV and reduce the voltage stress on the 10 kV SiC MOSFET and the DC-link capacitor. With 8 kV on each DC-link, the overall DC-link voltage in one phase, which is around 16 kV, is higher than the grid peak voltage corresponding to 1.4 p.u., which is around 15.8 kV, so the DC-link will not be charged. Instead, the DC-link voltage will gradually decrease because of DC-link voltage balancing resistors, which are sized at 5 MΩ, as shown in the period of [$t_2$, $t_3$] in Fig. 6-15.The grid fault is cleared after 5 cycles, and the converter detects that the grid voltage is recovered to normal at time $t=t_3$, then the braking switch is turned on to discharge the DC-link. At time $t=t_4$, DC-link voltages are all below 7.1 kV, the converter is restarted. Therefore, the simulation verifies the braking circuit function. With the braking circuit, the converter can quickly restart after the fault is cleared, and it does not affect the steady-state operation efficiency.

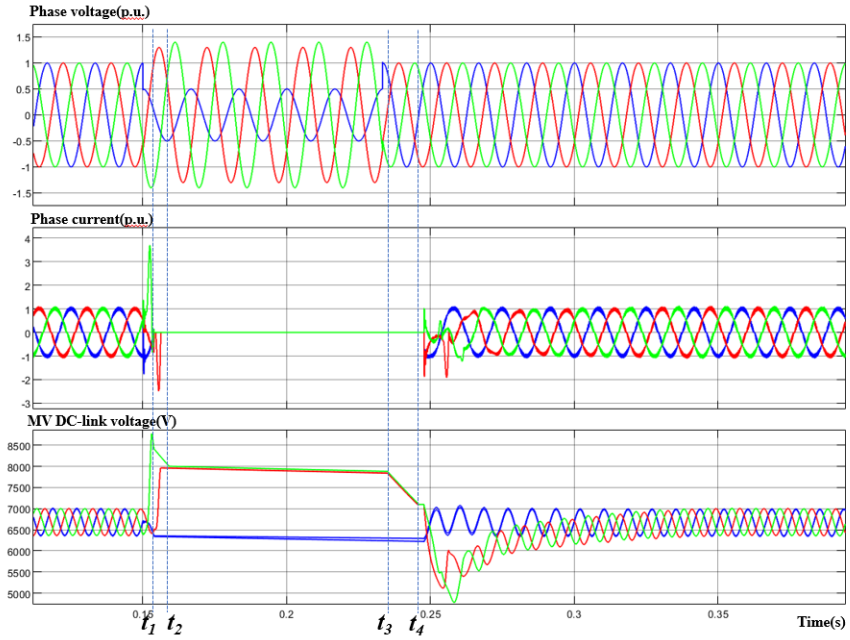



Fig. 6-15. Simulation with the additional braking circuit on each MV DC-link.

#### 6.3.2.4 Impact on the Hardware Design

Although the converter is temporarily turned off, the inrush current still flows through the filter inductor and the body diode of the SiC MOSFET. The maximum inrush current is considered to be 5 p.u. based on Fig. 6-13. The device transient current rating needs to be higher than the inrush current, and the filter inductor has to consider the inrush current to avoid saturation, which otherwise will result in an even larger inrush current. These will be introduced later in this chapter.

The hardware impact is mainly the dynamic braking circuit. Considering the discharging time and the braking switch current rating, the braking resistor is determined at 10 kΩ. So the maximum discharging current is 0.9 A, and the discharging time is around 0.3 s. Three IXYS 4.7 kV/2 A Si MOSFETs (IXTL2N470) are used in series as the braking switch, considering their lower cost and small current rating compared to the MV SiC MOSFET. In the future, they can also be replaced with a single low current MV SiC device with a sufficient voltage rating. The snubber circuit is necessary to balance the voltage, but considering the low current rating, they are neglected when estimating the component size and weight. Moreover, since these MOSFETs do not need to have a fast switching, the device loss is low, so no heat sink is used. Therefore, the overall braking device size and weight are around 12 $cm^3$ and 24 g, respectively.

Based on the DC-link capacitor energy change, the energy dissipated on the discharging resistor is

$$E_R = \frac{1}{2} \times (110uF)^2 \times \left((9.3kV)^2 - (7.1kV)^2\right) = 1.98kJ \tag{6-7}$$

Two Vishay 5 kΩ thick film chassis mount resistors (LPS0800L5001KB) are selected to be connected in series. Each resistor has a voltage rating of 5 kV dc, and a short-term energy rating of 1.5 kJ (@ 0.3 s), which can meet both the insulation and energy dissipation requirements. Also, because of the short period, no heat sink is needed for the resistor. Therefore, the overall resistor size and weight are 190 $cm^3$ and 166 g, respectively.

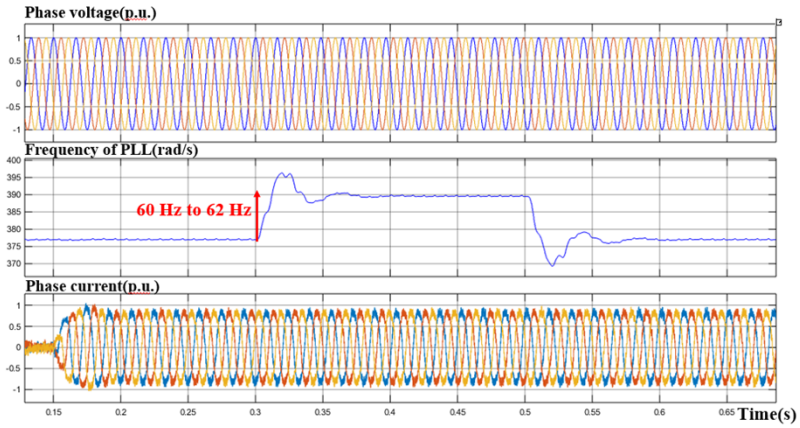
### 6.3.3 Frequency Ride Through and Grid Voltage Angle Change

The frequency ride-through (FRT) is also required in IEEE Std 1547-2018. The required FRT ranges for three different converter categories are the same. However, they have a different maximum rate of change of frequency (ROCOF) requirements, and the values for categories I, II, and III are 0.5 Hz/s, 2.0 Hz/s, and 3.0 Hz/s, respectively. The continuous operation frequency range is [58.8 Hz, 61.2 Hz], and the converter needs to ride through the low-frequency range of [50 Hz, 58.8 Hz] and the high-frequency range of [61.2 Hz, 66 Hz] with a duration of 299 s. Besides the frequency variation, IEEE Std 1547-2018 also requires the DER to ride through 20 electrical degrees of positive-sequence phase angle change within a sub-cycle-to-cycle time frame and up to 60 electrical degrees of individual phase angle change.

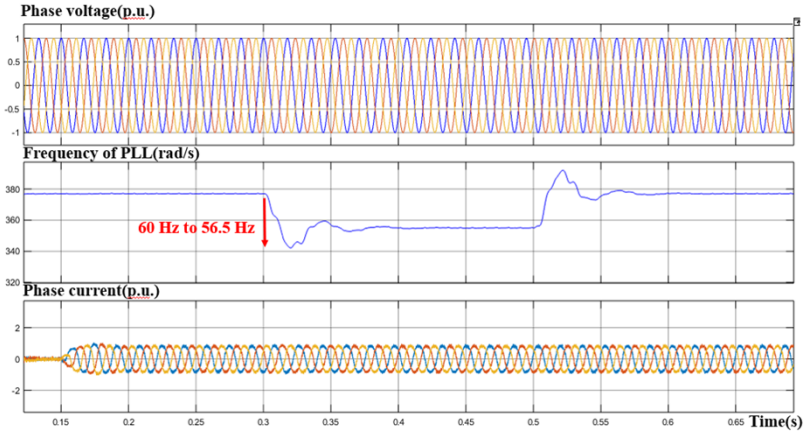
#### 6.3.3.1 Frequency Ride Through

The frequency variation in the power electric system is usually slow, and the maximum ROCOF requirement in IEEE Std 1547-2018 is 3.0 Hz/s. However, to find the worst impact from the frequency variation, a step-change is assumed in the frequency ride through simulation.

The frequency step-up and step-down simulation results are shown in Fig. 6-16 (a) and (b), respectively. From these waveforms, the frequency variation has little impact on the converter operation. Although the PLL needs a short time to catch up with the new frequency, the converter currents are not impacted since the frequency variation is still small.




(a) Frequency step up from 60 Hz to 62 Hz

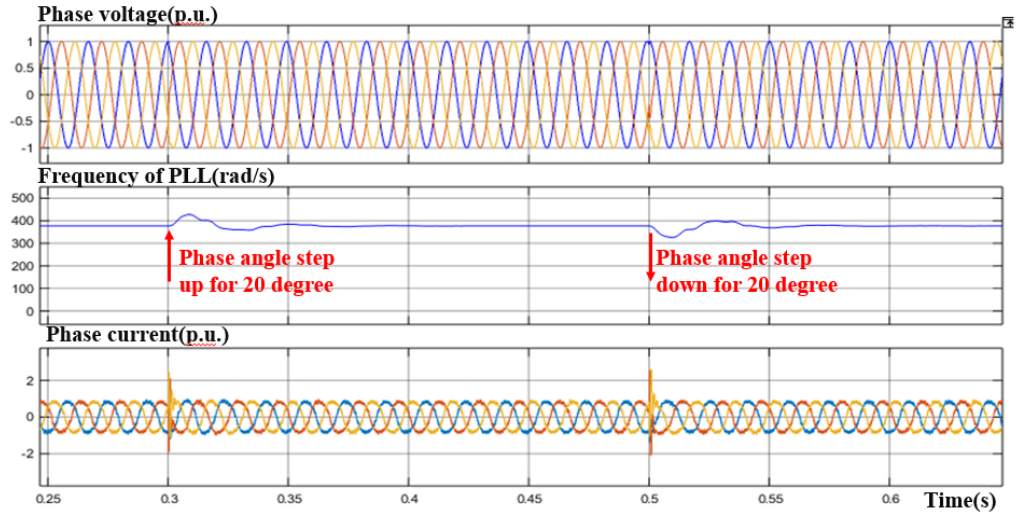



(b) Frequency step down from 60 Hz to 56.5 Hz

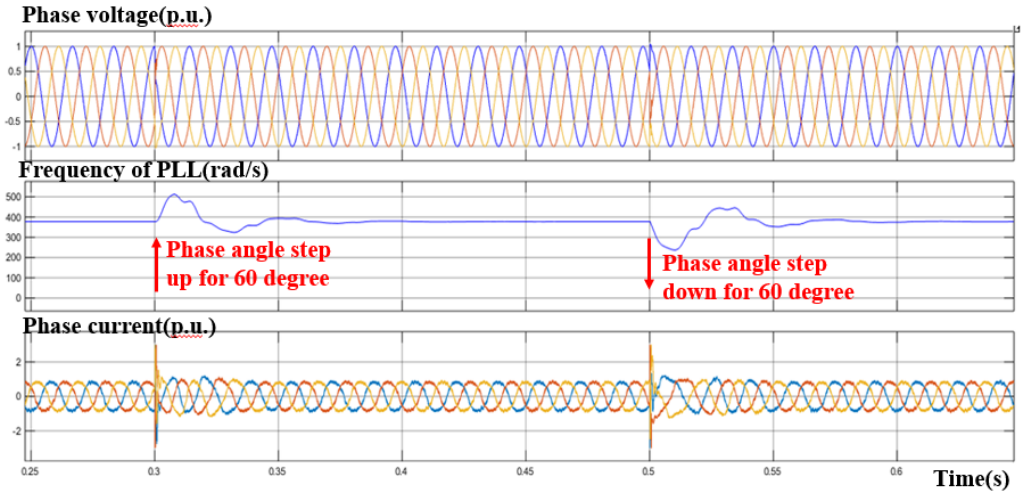
Fig. 6-16. Frequency ride through simulation.

### 6.3.3.2 Angle Variation

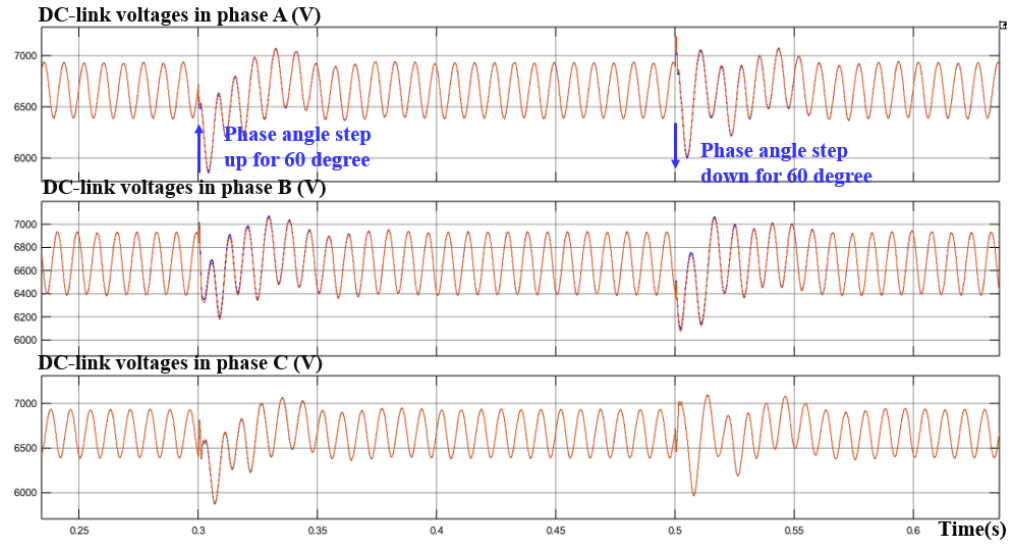
The voltage phase angle sudden change will lead to the voltage sudden change between the AC filter inductor, which results in an inrush current, similar to the discussion in section 6.3.1. The simulation is conducted to verify it. As shown in Fig. 6-17(a), when the voltage phase angle suddenly changes 20 electrical degrees, an inrush current of 2.2 p.u. occurs. A larger phase angle change results in a higher inrush current. As shown in Fig. 6-17(b), when the phase angle change becomes 60 degrees, the inrush current is around 3 p.u., which is limited by the PWM mask method. Due to the inrush current, the DC-link voltages are also impacted, as shown in Fig. 6-17 (c). With the limitation of the PWM mask method, the DC-link voltage variations are in an acceptable range. Therefore, the phase angle change leads to inrush current and DC-link voltage variations. With the PWM mask method, they both can be limited.




(a) Simulation waveforms of phase angle step change for 20 electric degrees




(b) Simulation waveforms of phase angle step change for 60 electric degrees




(c) DC-link voltage waveforms of phase angle step change for 60 electric degrees

Fig. 6-17. Phase angle change simulation.

#### 6.3.3.3 Impact on Hardware Design

Because of the PWM mask function, the inrush current can be limited, but the inductor design and 10 kV SiC MOSFETs' transient current capability need to be further considered, which will be introduced later in this chapter.

Based on (6-1), the DC-link capacitance is related to the fundamental frequency. To keep the same voltage ripple, a lower fundamental frequency results in a larger DC-link capacitance. Since the frequency variation is not short (hundreds of seconds), it needs to be treated as a steady state. Considering the minimum frequency, i.e., 50 Hz, the DC-link capacitance need to be increased from 99 μF to 119 μF. The same DC-link capacitor will be used due to the limitation of available products, since the capacitance is only 100 μF, the DC-link voltage ripple will increase from ±5% to ±5.4%, which is still acceptable.

### 6.3.4 Lightning Surge

The converter needs to be designed such that it will not be damaged or even trip when a lightning surge occurs.

#### 6.3.4.1 The 1st Impact: Inrush Current

The power loop of the converter, through which a lightning surge may pass, can be simplified as shown in Fig. 6-18. To simplify the analysis, the DC/DC stages of the PCS converter are represented by current sources and decoupled from DC/AC stages. Because of the three-phase four-wire configuration, the neutral wire can be grounded through the converter or the AC grid grounding, and an inductor $L_{ng}$ (could also be resistor or both) represents the neutral line to ground impedance.

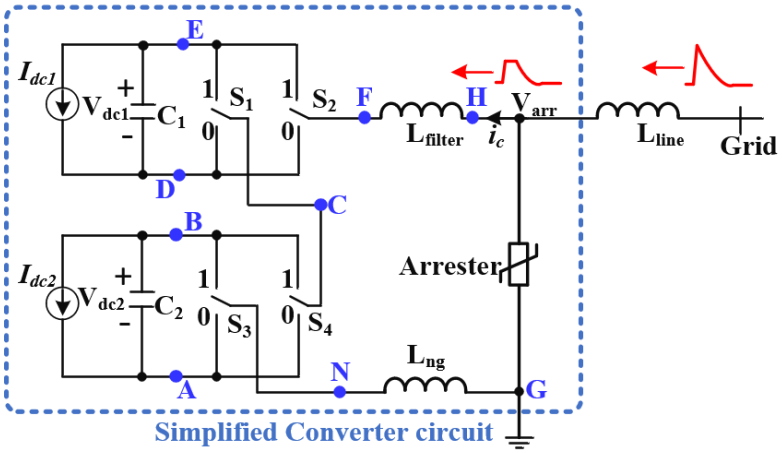



Fig. 6-18. Simplified converter power loop in terms of the transient surge.

When a lightning surge occurs, the arrester absorbs a large surge current and clamps the converter terminal voltage $V_{arr}$ at a certain level, which is dependent on the surge current, for example, 37 kV (at 10 kA). However, 37 kV is still much higher than the grid's normal operating voltage. And the maximum output voltage of the PCS converter, $V_{FN}$, is the sum of two DC-link voltages in each phase, which is 13.4 kV. Then, the filter inductor $L_{filter}$ and the neutral-to-ground impedance $L_{ng}$ share the remaining voltage and the phase current $i_c$ will increase. The inductor current increment during the lightning surge can be estimated as

$$\Delta i_L = \frac{di_c}{dt}\Delta t = \frac{V_{arr} - V_{FN}}{L_{filter} + L_{ng}} = \frac{V_{arr} - (S_2 - S_1)V_{dc1} - (S_4 - S_3)V_{dc2}}{L_{filter} + L_{ng}}\Delta t \quad (6\text{-}8)$$

where $S_k$ (k =1, 2, 3, 4) represents the state of the device in each half-bridge, and

$$S_k = \begin{cases} 1 & If\ current\ flow\ through\ the\ upper\ device \\ 0 & If\ current\ flow\ through\ the\ lower\ device \end{cases} \quad (6\text{-}9)$$

Although the lightning surge duration is quite short, the high overvoltage can still induce a large inrush current because of the large voltage and small impedance. From (6-8), the worst case happens when:

1) the neutral-to-ground impedance $L_{ng}$=0, which means the PCS converter is solidly grounded at the neutral point.

2) the converter output voltage, $V_{FN}$, has an opposite polarity to the lightning surge voltage.

Since the typical lightning surge has a time characteristic of 1.2/50 μs, it is assumed that the arrester clamps the lightning surge at 37 kV for 50 μs, which simplifies the calculation of the inrush current. Then, under a positive lightning surge, the current increment during the surge transient in the worst case could be

$$\Delta i_{L1} = \frac{37\ kV + 6.67\ kV + 6.67\ kV}{4.4\ mH + 0} \times 50\ us = 573\ A = 9.8\ p.u. \quad (6\text{-}10)$$

A better situation is when the lightning surge occurs, the converter switching state is $S_2$=$S_4$=1 and $S_1$=$S_3$=0. The converter output voltage, $V_{FN}$, becomes the same polarity as the lightning surge voltage. This could help to reduce the rising rate of the current. Assuming the PCS converter output voltage has an opposite polarity to the lightning surge, then the inrush current would be

$$\Delta i_{L2} = \frac{37\ kV - 6.67\ kV - 6.67\ kV}{4.4\ mH + 0} \times 50\ us = 268\ A = 4.5\ p.u. \quad (6\text{-}11)$$

If the PWM mask function is utilized, when the inrush current exceeds the threshold value, PWMs can be masked. Then, the inrush current will flow through the body diodes of MOSFETs, and this will change the PCS converter output voltage to be the same polarity as the lightning surge voltage and help to reduce the rising rate of the inrush current.

Then, with solid ground, the PCS converter may have an inrush current within a range of [4.5 p.u., 9.8 p.u.] depending on the switching states of the PCS converter at the moment when the lightning surge happens. Besides, the saturation characteristic of the filter inductor is neglected and the filter inductance is assumed to be constant even with a high current. However, if the inductor is not designed to have that high saturation current capability, the inductor may be saturated during the lightning transient and the inrush current will go higher than the calculation.

The inrush current will flow through the filter inductor, devices, busbar, etc. Also, the regular protection components, such as fuse and mechanical switches, cannot protect the converter from this inrush current because their response time is much longer than the period of a lightning surge. Therefore, if the inrush current induced by the lightning is not considered in the converter design, it could trip or even damage the PCS converter.

From the analysis, it can also be found that the AC grid side filter inductance and the neutral-to-ground impedance are the main impedance to limit the inrush current from a lightning surge. A smaller overall impedance results in a larger inrush current. Therefore, a larger filter inductance or a higher grounding impedance can help reduce the inrush current caused by a lightning surge.

#### 6.3.4.2 The 2nd Impact: DC-link overvoltage

As analyzed above, the inrush current will also flow through the DC-link capacitor, either through the MOSFET channel or through the body diode. If devices are switching and the inrush current flows through the device channel, it could either charge or discharge the DC-link voltage depending on the state of the switch. If the PCS converter has stopped switching as a result of overcurrent protection and the inrush current flows through body diodes of MOSFETs, the inrush current will only charge DC-link capacitors. In both cases, DC-link overvoltage may happen.

From Fig.6-18, differential equations for DC-link capacitors are

$$\begin{cases} C_1 \frac{dV_{dc1}}{dt} = (S_2 - S_1) i_c - I_{DC1} \\ C_2 \frac{dV_{dc2}}{dt} = (S_4 - S_3) i_c - I_{DC2} \end{cases} \tag{6-12}$$

Through solving equations (6-10), (6-11), and (6-12), the overvoltage and overcurrent of the converter can be obtained. However, it is difficult to do that, so simulation could be a good method to do the estimation. Since the lightning transient duration is short, increasing the DC-link capacitance can significantly reduce the voltage overshoot. Also, increasing the filter inductance can help to reduce the DC-link overvoltage because of the smaller inrush current.

#### 6.3.4.3 The 3rd Impact: Converter Insulation Considerations

Insulation is another important consideration for the MV PCS converter when facing a lightning surge. As introduced above, during a lightning surge, even with the arrester the induced voltage could be around 37 kV (referenced to ground). Therefore, high potential (referenced to ground) may also occur on the converter components, which may also stress the converter insulation.

Since the arrester is connected between the line and ground, the potential, referenced to the ground, of different components in the converter has to be considered. As shown in Fig. 6-18, different points in the converter have different potentials during the lightning surge, and they can be expressed as

$$\begin{cases} V_{NG} = \frac{L_{ng}}{L_{ng} + L_{filter}} (V_{arr} - S_{21} V_{dc1} - S_{43} V_{dc2}) \\ V_{AG} = V_{NG} - S_3 V_{dc2} \\ V_{BG} = V_{NG} + (1 - S_3) V_{dc2} \\ V_{CG} = V_{NG} + S_{43} V_{dc2} \\ V_{DG} = V_{NG} + S_{43} V_{dc2} - S_1 V_{dc1} \\ V_{EG} = V_{NG} + S_{43} V_{dc2} + (1 - S_1) V_{dc1} \\ V_{FG} = V_{NG} + S_{43} V_{dc2} + S_{21} V_{dc1} \\ V_{HG} = V_{arr} \end{cases} \tag{6-13}$$

From (6-13), the converter neutral point potential, $V_{NG}$, makes a substantial difference for the components' potential during the lightning transient. $V_{NG}$ is mainly determined by the ratio of the neutral-to-ground impedance, $L_{ng}$, to the filter inductor impedance, $L_{filter}$. A larger ratio of $L_{ng}$ to $L_{filter}$ will result in a higher neutral point potential during the lightning transient, and all the components' potential will be increased correspondingly. On the contrary, a smaller ratio of $L_{ng}$ to $L_{filter}$ will result in a smaller neutral point potential and it helps to reduce the converter component potentials during the lightning transient. In this case, the filter inductor withstands most of the clamped voltage, by the arrester.

Therefore, although the neutral-to-ground impedance can help to reduce the inrush current, it also increases the neutral point potential during the lightning transient and then increases the insulation requirements (to the ground) for the components in the converter, such as the DC bus, wires, devices, etc.

Besides, the converter or grid grounding impedance is mainly determined by the system's temporary overvoltage design, and it is hard to change for the lightning consideration.

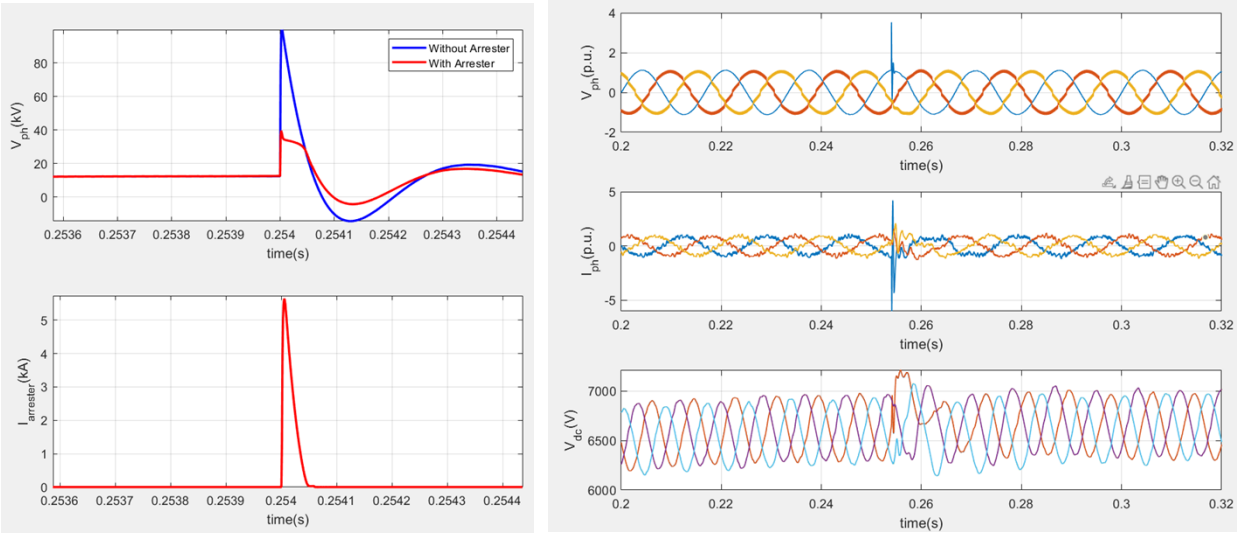
#### 6.3.4.4 Simulation Verification

A simulation model, including the grid, PCS converter, lightning emulator, as well as arrester, is used to study the impact of a lightning surge on the converter operation more accurately, and more details can be found in [185]. Fig. 6-19(a) shows the voltage clamping performance of the arrester. Without the arrester, during the lightning surge, the converter terminal voltage has a peak value of around 95 kV. However, with the arrester, the voltage peak is clamped at around 37 kV, and the surge current flowing through the arrester is around 5.5 kA. Fig. 6-19(b) shows waveforms of the phase voltage, phase current, and DC-link voltages. An inrush current up to 6 p.u. is induced during the lightning transient, and DC-link voltages of phase C (lightning surge phase) have a voltage overshoot of around 500 V. This verifies the inrush current and DC-link voltage overshoot analysis.

To evaluate the impact of a lightning surge on the PCS converter insulation. Instead of solid grounding, different neutral-to-ground impedances are used in the simulation. In Fig. 6-20(a), the neutral-to-ground impedance is 0.5 mH, and during the lightning surge, the neutral point potential is around 0.2 p.u. The inrush current is around 4.7 p.u., which is smaller than the value, 6 p.u. in Fig. 12, in the case where the neutral point is solidly grounded. With a larger neutral-to-ground impedance, as shown in Fig. 6-20(b), the neutral point potential increases to around 0.55 p.u. while the inrush current is reduced to 4.0 p.u.

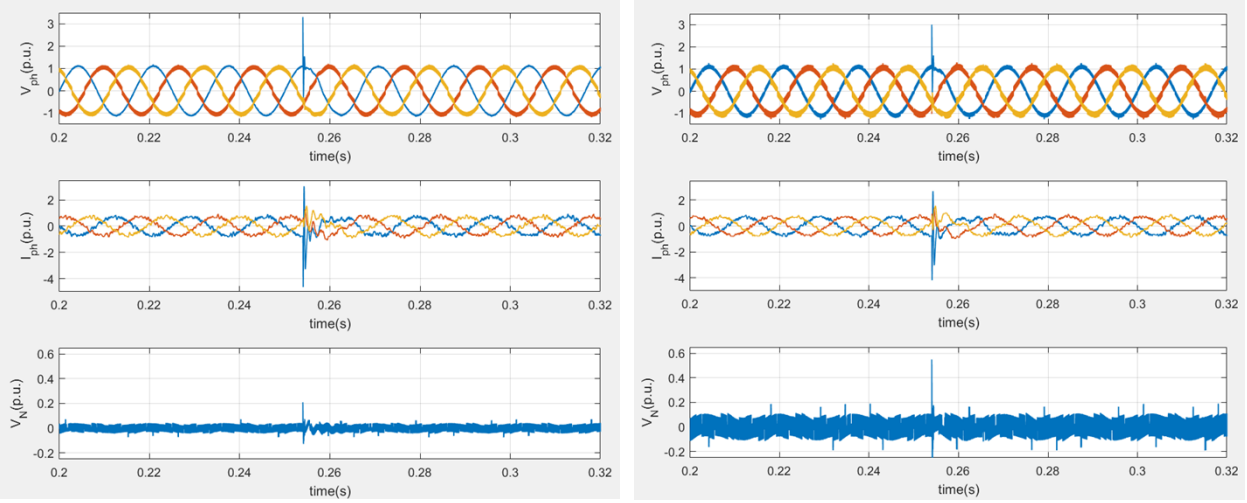
Therefore, as shown in Table 6-6, a larger neutral-to-ground impedance results in a smaller inrush current but leads to a higher neutral point potential, which increases the potential of other components in the converter. This verifies the theoretical analysis in Section II.

Although the PWM mask function cannot limit the inrush current induced by the lightning surge, it can still help to reduce the inrush current. As shown in Fig. 6-21, with the help of the PWM mask function, the inrush current drops from 6 p.u. in Fig. 6-19 to around 5 p.u.




(a) Phase voltage and arrester current (b) converter waveforms

Fig. 6-19. Waveforms of phase voltage, arrester current, phase current, and DC-link voltage with $L_{ng}$=0.




(a) $L_{ng}$=0.5 mH (b) $L_{ng}$=1.5 mH

Fig. 6-20. Waveforms of phase voltage, phase current, and the neutral point voltage with different $L_{ng}$.

Table 6-6. PCS converter lightning surge simulation summary.

| Neutral-to-ground impedance | Inrush current | Neutral point potential |
|---|---|---|
| 0 | 6 p.u. | 0 |
| 0.5 mH | 4.7 p.u. | 0.2 p.u. |
| 1.5 mH | 4.0 p.u. | 0.55 p.u. |

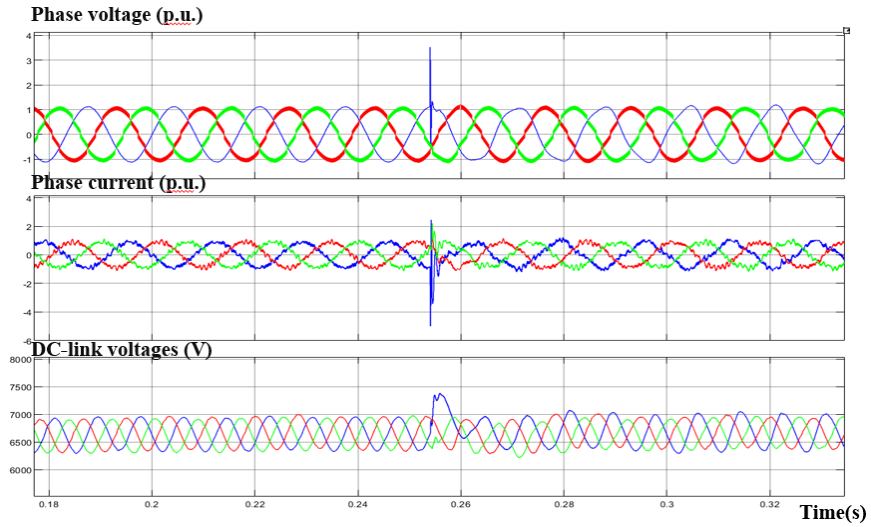



Fig. 6-21. Waveforms of lightning surge simulation with PWM mask function and $L_{ng}$=0 mH.

### 6.3.4.5 Impact on the Hardware Design

The inrush current also needs to be considered in the filter inductor design and 10 kV SiC MOSFETs selection, which will be discussed later in this chapter. The DC-link voltage overvoltage is still within the capability of the device and the DC-link capacitor, so no hardware needs to be redesigned.

## 6.4 DESIGN COMPARISON

### 6.4.1 Summary of the Impact of Grid Requirements on the Converter Design

The impacts of grid requirements on the converter design discussed in this chapter are summarized in Table 6-7.

Table 6-7. Summary of the grid requirements impact on the converter design.

| Grid/design requirements | Requirement details | Impact on converter design |
|---|---|---|
| Voltage ride through | ▪ The converter needs to ride through the low voltage range of [0, 0.88 p.u.], and ride through the high voltage range of [1.1 p.u., 1.2 p.u.] | ▪ Inrush current, which can be effectively limited by the PWM mask function, e.g., 2 p.u.<br>▪ The DC-link voltage needs to increase to 6.67 kV to accommodate the 1.2 p.u. grid voltage with an acceptable PWM modulation saturation<br>▪ Power control coordination between the DC/DC stage and the DC/AC stage and between the PCS converter and other resources on the LV DC bus |
| Grid faults | ▪ Follow the voltage ride-through requirements if the overvoltage is lower than 1.2 p.u.<br>▪ If the fault causes overvoltage of more than 1.2 p.u., the converter can temporarily stop working, but when the grid voltage is recovered, the converter needs to restart within 3 s | ▪ Inrush current, up to 5 p.u.<br>▪ DC-link overvoltage, up to 9.3 kV<br>▪ Extra braking circuit, to reduce the DC-link overvoltage to 8 kV during the fault period, and to quickly discharge the DC-link after the fault is clear so that the converter can realize restart within 1 s |
| Frequency ride through | ▪ The continuous operation frequency range is [58.8 Hz, 61.2 Hz]<br>▪ Ride through the low-frequency range of [50 Hz, 58.8 Hz] and the high-frequency range of [61.2 Hz, 66 Hz] with a period of 299 s | ▪ No inrush and large DC-link overvoltage<br>▪ Need larger DC-link capacitance to limit the DC-link voltage ripple when operating at the lowest fundamental frequency |
| Grid voltage angle change | ▪ Ride through 20 electrical degrees of positive-sequence phase angle change within a sub-cycle-to-cycle time frame and up to 60 electrical degrees of individual phase angle change | ▪ Inrush current exists due to the voltage suddenly changes, but can be effectively limited by the PWM mask function<br>▪ DC-link voltage variation, but no need for hardware change |
| Lightning surge | ▪ Avoid damage or trip when a lightning surge occurs | ▪ Inrush current, up to 5 p.u.<br>▪ DC-link overvoltage, which is not too large because of the short period<br>▪ Converter internal component insulation needs to consider the potential of the neutral point during the lightning transient |

### 6.4.2 Impact on the DC-link Capacitor Design

The HVRT and the FRT requirements impact the DC-link capacitor design. Starting from the baseline design, the DC-link voltage changes from 6.3 kV to 6.67 kV after considering the HVRT. The capacitance, which is sized based on ±5% voltage ripple, changes from 114 μF to 99 μF after considering the HVRT, and then increases to 119 μF after considering the FRT, as shown in Fig. 6-22. However, the film capacitor products are not seamless in terms of voltage rating and capacitance value. The capacitor selected in the baseline design is still used after considering grid requirements, however, the voltage and capacitance margin are reduced.

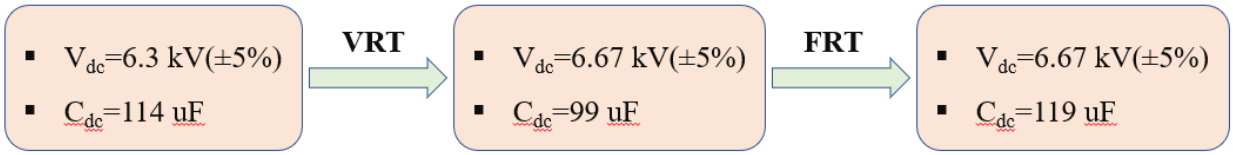



Fig.6-22. DC-link capacitor parameters.

### 6.4.3 Impact on the AC Filter Inductor Design

The inrush current needs to be considered in the inductor design to make sure it does not saturate. In cases of LVRT, HVRT, faults, grid voltage angle change, and lightning, a larger filter inductance leads to a smaller inrush current. Therefore, the inductor design has two choices:

- Same inductance with large inrush current capability.
- Larger inductance with small inrush current capability.

The design goal here is to get the inductor size as small as possible, so the two choices are compared. The AP value is commonly used in the inductor design and the core selection, and it can be calculated as

$$AP = L \cdot \frac{I_{rms} \cdot I_{inrush}}{K_u \cdot B_{max} \cdot J_{max}} \tag{6-14}$$

where $I_{rms}$ is the current RMS value, $I_{inrush}$ is the inductor inrush current, $K_u$ is the window area utilization factor, $B_{max}$ is the maximum flux density, and $J_{max}$ is the maximum wire current density. The inrush current in different grid conditions can all be estimated as

$$I_{inrush} = I_{ph} + \frac{\Delta v_{ph}}{L}\Delta t \tag{6-15}$$

where $I_{ph}$ is the phase current before the abnormal condition, $\Delta v_{ph}$ is the phase voltage change, which induced the inrush current, and $\Delta t$ is the rising period of the inrush current. Substituting (6-15) into (6-14) results in

$$AP = L \cdot \frac{I_{rms} \cdot \left(I_{ph} + \frac{\Delta v_{ph}}{L}\Delta t\right)}{K_u \cdot B_{max} \cdot J_{max}} = \frac{L \cdot I_{rms} \cdot I_{ph} + \Delta v_{ph}\Delta t}{K_u \cdot B_{max} \cdot J_{max}} \tag{6-16}$$

Since changing the inductance does not change the grid voltage variation and $\Delta t$, it can be concluded that a larger inductance leads to a larger core AP value, and thus the inductor size will be larger. Therefore, the inductance will not be changed, instead, the inrush current of the inductor will be designed up to the worst case, which is 5 p.u.

The inductor electrical design results are shown in Table 6-8. Compared to the baseline design, since the current peak is significantly increased, more cores are used, and the air gap is increased. Due to the longer wire length per turn, the copper loss is also increased. The same insulation design process as discussed in section 6.2.4 is followed to design the inductor. The thermal simulation is also conducted with Ansys/Icepak, and the temperature rise is around 68 ºC, which can meet the thermal requirement. The inductor's overall size and weight are around 16,410 $cm^3$ and 74.5 kg, respectively.

Table 6-8. Inductor electrical design results considering grid requirements.

| Parameters | Baseline | Considering grid requirements |
|---|---|---|
| Inductance | 4.4 mH | 4.4 mH |
| Current RMS value | 44 A | 44 A |
| Current peak | 66 A | 300 A |
| Core material | Amorphous | Amorphous |
| Core size | AMCC1000 × 2 | AMCC1000 × 8 |
| Winding turn number | 60 | 48 |
| Wire gauge | AWG #5 | AWG #5 |
| Air gap | 4.8 mm | 12 mm |
| Wire loss | 52 W | 90 W |
| Core loss | 48 W | 104 W |

### 6.4.4 Impact on the Device Design

The inrush current flows through both the inductor and the 10 kV SiC MOSFET, either the channel or the body diode. Although the thermal model in the simulation shows the estimated junction temperature does not exceed the maximum junction temperature too much, the device transient current rating is not only determined by the thermal requirements but also related to the package, wire bond, etc. Besides, the thermal model is an average model, and cannot accurately estimate the local temperature. There is little information about the transient current capability of the 10 kV SiC MOSFET or its body diode. However, since LV SiC devices are mature, this information can be easily found in their datasheets. The maximum current rating of these LV SiC MOSFETs within a short period ([100 us, 1ms]) is around 2 to 3 times their current ratings. Assume the 10 kV SiC MOSFET can also achieve 3 times of short period current capability through thermal and package design. Then, to withstand the 5 p.u. inrush current, the device current rating needs to be 1.67 p.u., i.e., 100 A, which means each device needs 5 dies in parallel. This increases the scaled half-bridge power module size and weight to 390 $cm^3$ and 0.4 kg, respectively.

### 6.4.5 Overall Converter Size and Weight Comparison

The converter component size and weight are compared with the baseline design. As shown in Fig. 6-23, compared to the baseline design. The device size and inductor size increase after the grid requirements are taken into consideration, as a result, the overall component size increases by around 26%. Compared to the baseline design, the overall component weight increases by 90%, as shown in Fig. 6-24. The DC-link capacitor design is also impacted by the grid requirements. However, due to the limitation of available products, the capacitor size and weight changes are not reflected in the figures.

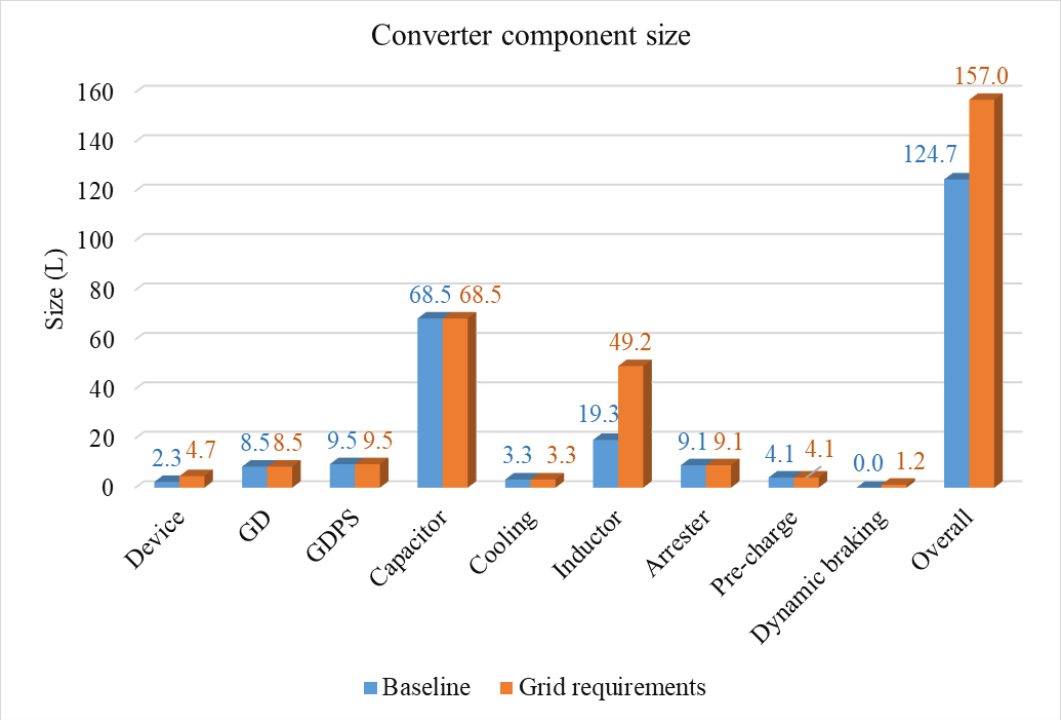



Fig. 6-23. Converter size comparison between the converter baseline design and the converter designed considering grid requirements.

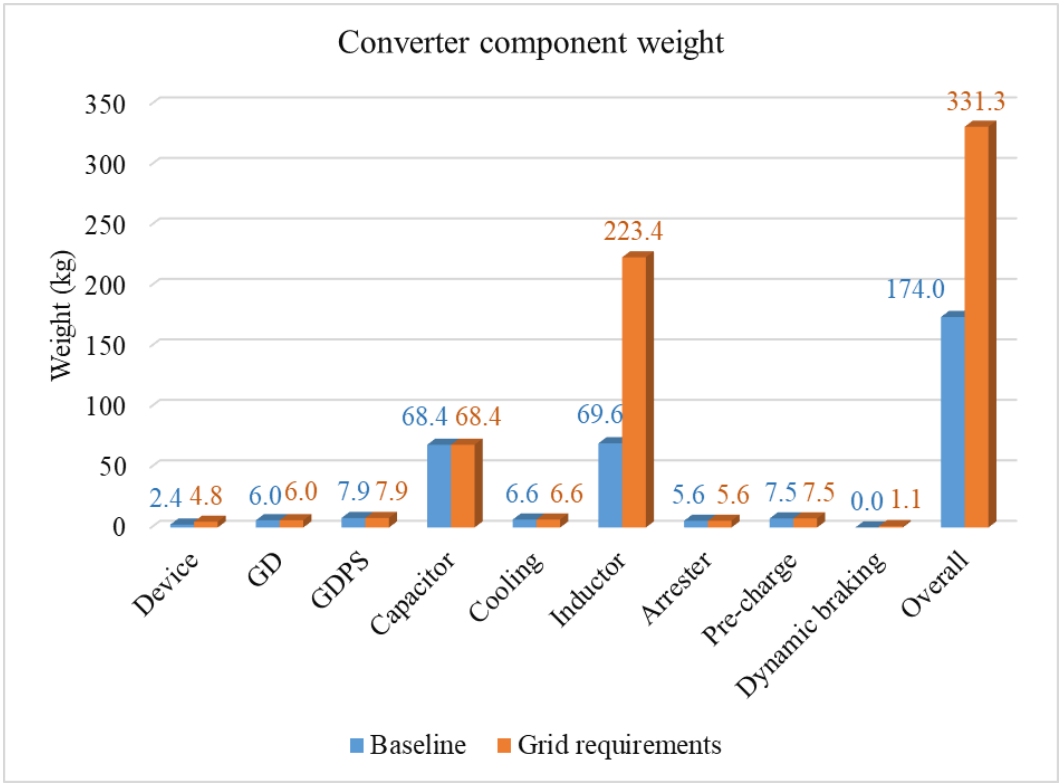



Fig. 6-24. Converter weight comparison between the converter baseline design and the converter designed considering grid requirements.

## 6.5 CONCLUSION

The impact of grid requirements on the MV SiC-based grid-connected converter is evaluated in this chapter. A baseline design is conducted first without considering most of grid requirements. Then, grid requirements are considered one by one, including the voltage ride through, grid faults, frequency ride through, voltage angle variation, and lightning surge. The impacts are mainly inrush current, DC-link voltage variation, and converter component insulation consideration. The inrush current impacts the inductor design and the device's transient current capability; the DC-link voltage needs to be selected based on the highest continuous grid voltage, and the DC-link capacitor needs to be sized based on the worst voltage variation condition. The insulation consideration is related to the converter and system grounding configuration and mainly needs to consider the lightning transient.

A PWM mask method has been introduced to limit the inrush current caused by grid voltage disturbances. However, when the grid voltage is higher than the overall DC-link voltage of each phase, the PWM mask method cannot effectively limit the inrush current, but can still reduce the current increasing rate, which reduces the inrush current to some extent. Simulation and experiment tests verify the control method. A dynamic braking circuit is introduced to limit the DC-link overvoltage when a fault happens and causes temporary overvoltage higher than 1.2 p.u. The braking circuit can quickly discharge the DC-link voltage to the normal range and let the converter restart within 1s after the fault is cleared. Then, based on the impact identification, the converter hardware has been redesigned. And the comparison between the new design and the baseline design is conducted. After considering the grid requirements, the overall component size and weight are increased by 26% and 90%, respectively, and most of them come from the filter inductor.

# 7. SUMMARY AND CONCLUSION

Through a survey and benchmark analysis, this report identified and documented potential high-impact applications in MV distribution grids that will significantly benefit from HV SiC devices. In particular, the report identified applications that can utilize the high switching speed and high control bandwidth enabled by SiC-based equipment.

Five main tasks were carried out:

1) Surveyed and summarized the latest HV SiC devices available from commercial vendors. The data were used in the analysis and benchmark study in comparison with Si devices;
2) Surveyed and summarized existing and emerging power electronics-based equipment for MV distribution grids, including current and future grids. The survey and analysis led to the selection of microgrids for further benchmark study;
3) Analyzed both the converter-level and system-level benefits of using HV SiC in the DER interface converters in conventional MV AC microgrids;
4) Analyzed both the converter-level and system-level benefits of using SiC in the PCS converters in MV asynchronous AC microgrids.
5) Evaluated the impact of grid requirements on the HV SiC-based grid-connected converter design.

The main findings in this report can be summarized as follows:

1) Compared with their Si-based solutions, most power electronics equipment using HV SiC can have simplified topology and smaller passive filters as a result of the higher voltage and faster switching capabilities of HV SiC devices. Fast switching of HV SiC devices will enable high control bandwidth, leading to enhanced functionalities and capabilities of some power electronics equipment, e.g., integrated filtering and system stabilizing functions for DER interface converters;

2) Microgrids, as an emerging application and an interface between the DERs and utility grid, involve many renewable energy sources, distributed generation, loads, and energy storage systems. Microgrids generally include multiple power electronic converters. HV SiC devices can help improve these converters and enhance their system capabilities and functionalities. Therefore, the MV microgrid can be a “killer application” for HV SiC devices;

3) HV SiC devices can benefit DER converters in a conventional AC microgrid at both the converter and system levels. At the converter level, the SiC-based DER converter will have a significant weight and size advantage compared with the Si counterpart, e.g. an 82.9% weight reduction and 73.2% size reduction can be achieved for a 1 MW, 13.8 kV PV interface converter using HV SiC devices. The SiC-based DER converters can work with a higher switching frequency (e.g. 3 times that of Si-based converters), and therefore have a higher control bandwidth. At the system level, the high control bandwidth results in power quality improvement (e.g. saving the need for a dedicated active power filter which can be 14% of the total converter rating in the example study), system stability enhancement (keeping stability even in weak grid conditions) and better LVRT dynamic performance;

4) HV SiC devices can also benefit PCS converters in asynchronous microgrids both at converter and system levels. At the converter level, the SiC-based PCS has significant benefits in weight and size (e.g., 83% weight reduction and 81% size reduction with SiC-based three-level 13.8 kV, 1 MW NPC, 60% weight reduction, and 67% size reduction with SiC-based MMC, compared with a Si three-level NPC, even without considering low-frequency transformers), and even in efficiency if the switching frequency is limited to 10 kHz (e.g., 46.6% loss reduction with SiC-based three-level

NPC and 31.8% reduction with SiC-based MMC). The HV SiC-based PCS converters can work with a higher switching frequency (around 10 to 20 times higher than Si-based PCS converters), and therefore have a higher control bandwidth. At the system level, the high control bandwidth of the PCS converters can result in enhanced performance of the microgrids on power quality, system stability, LVRT, transition between islanded mode and grid-connected mode, and black start capability. On power quality, SiC-based PCS can have integrated harmonic filtering capability and therefore eliminate the need for additional harmonic filters (e.g. saving an APF that can be 14% of the PCS converter or load rating). On stability, the SiC PCS can isolate the impact of the grid impedance and enhance the system stability in grid-connected mode, and operates as a stabilizer to enhance the stability in islanded mode. On LVRT, mode transition between grid-connected and islanded modes and black start, with the PCS, the load in the microgrid can be supplied normally even during the LVRT and mode transition periods and the black start can be easier.

5) Grid requirements have impact on the grid-connected converter design. The grid voltage disturbances, such as LVRT, HVRT, voltage angle change, temporary overvoltage, and transient overvoltage can lead to inrush current and DC-link overvoltage. A PWM mask method is used to limit the inrush current induced by the grid voltage sudden change by temporarily masking the PWMs so that the inrush current flow through the MOSFET body diode and is reduced by the DC-link voltage. However, when the grid voltage amplitude is higher than the DC-link voltage, the PWM mask method can only reduce the inrush current rising rate but cannot limit it. For temporary overvoltage higher than 1.2 p.u., which can be induced by grid faults, the converter is designed to temporarily stop operation, and restarts within 3 seconds when the grid voltage recovers to below 1.2 p.u. A dynamic braking circuit is introduced to suppress the DC-link overvoltage and ensure a quick restart. Although arresters are installed to protect the converter from lightning surge, the voltage clamped by the arrester is still much higher than the converter's normal operation voltage, and the high voltage leads to large inrush current, DC-link voltage variation, as well as insulation consideration. An online simulation consisting of the converter switching mode, the arrester mode, the coupling and decoupling network, as well as the combined wave generator is utilized to verify the lightning impact on the converter operation. A larger filter inductance helps to reduce the inrush current, but the converter size and cost will also be increased. A larger grounding impedance also helps to reduce the inrush current, but the converter components have a higher transient potential during the lightning surge, which results in a higher insulation requirement. Based on the converter design comparison, after considering the grid requirements, the converter size and weight increased by 26% and 90%, respectively.

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