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Additively Manufactured Photovoltaic Inverter (AMPVI)

Madhu Chinthavali Ph. D
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OAK RIDGE NATIONAL LABORATORY
MANAGED BY UT-BATTELLE FOR THE US DEPARTMENT OF ENERGY

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ADDITIVELY MANUFACTURED PHOTOVOLTAIC INVERTER (AMPVI)

Madhu Chinthavali Ph.D. (ORNL)

Steven Campbell (ORNL)

Jack Wang(ORNL)

Akanksha Singh (NREL)

Scott Sudhoff (Purdue University)

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EXECUTIVE SUMMARY

Successful integration of hundreds of gigawatts of solar photovoltaics (PV) into the electric power system requires transformative power conversion system design that optimizes various trade-offs among conflicting objectives, such as performance, reliability, functionality, and cost. To address this need, National Renewable Energy Laboratory, Oak Ridge National Laboratory, and Purdue University teamed up to develop a unique PV inverter design. The Additively Manufactured Photovoltaic Inverter (AMPVI) combines newer wide bandgap high-voltage silicon carbide (SiC) semiconductor devices with revolutionary concepts such as additive manufacturing and multi-objective magnetic design optimization. The AMPVI will not only provide superior technical capabilities in terms of energy conversion but also mitigate market barriers for SiC-based PV inverters. The benefits for this design will include better utilization of PV power due to higher DC voltage, lower operations and maintenance costs, better system efficiency, longer system lifetime, and advanced grid support functionalities for easier grid integration. All these advantages will lead to a significant reduction of the levelized cost of energy for PV systems.

Activities in Budget Period 1 (BP1) of this 3-year integrated project were focused on development and component-level validation of the foundational building blocks needed for the AMPVI. Multiple interrelated tasks were completed in parallel during work towards the initial development of the high-voltage SiC-based power block, gate driver, controller board, and control algorithms. Initial development of magnetic design tools and initial inverter thermal and mechanical design was also completed in this period. All these activities ensured that the initial prototype (called “alpha-prototype”) power block and controller would be ready after BP1 for integration into the first inverter prototype (i.e., the alpha-prototype inverter) in BP2.

The activities in BP2 focused on inverter system-level validation of the building blocks developed in the previous BP; development and validation of additional components such as new magnetics; and then optimization of the power block’s design, magnetics, and overall AMPVI based on system-level testing, cost, and reliability analysis results. The activities in BP3 focused on optimizing the inverter design based on the system-level testing results obtained in BP2. They included additively manufacturing the final building block and gate drive; refining the design codes for power magnetics devices; constructing a final set of additional components, such as a DC link inductor and an AC inverter-side inductor; testing the finalized PV inverter prototype; conducting system-level validation; demonstrating the inverter using power hardware-in-the-loop, and conducting a final cost and reliability analysis of the inverter.

This final report provides a detailed yet concise review of the technical results for the research activities conducted during the three BPs towards accomplishing the final project goals. This report also provides a comparison between the current state-of-the-art and the project design for each of the main components—the power block, the magnetics, the controller and the inverter—to highlight major technology advancements.

1. BACKGROUND

Based on the present industry outlook, it is certain that technical advancements and commercialization efforts for wide bandgap (WBG) power electronic devices such as silicon carbide (SiC) and gallium nitride (GaN) will drive the future of power electronics systems in terms of efficiency and power density. The potential for integration of WBG-based systems in commercial applications, including PV, has been discussed in previous literature. Studies have demonstrated that SiC-based PV power electronics could provide 6–8× reduction in switching losses and increase power density significantly with higher switching speeds. Still, such devices would be more expensive than their silicon (Si) counterparts (SiC devices are currently two to three times more expensive than Si devices with a similar rating). Moreover, the present-day design of SiC power electronics relies on discrete switching components (such as metal-oxide-semiconductor field-effect transistors [MOSFETs,] and Schottky diodes), discrete gate drivers and discrete interconnects packaged together in a nonstandard and unoptimized packaging, and magnetics and thermal design that are not optimized for SiC devices.

All of these make present-day SiC designs costlier than equivalent Si-based designs. As a result, the PV inverter industry is still hesitant to adopt SiC and thus trades higher inverter performance for lower cost. In an extremely competitive market, PV inverter manufacturers are reluctant to try new solutions that are not cost-optimized. Therefore, although various SiC inverters have been successfully demonstrated, a full SiC-based PV inverter is still not commonly available in the market; only a few commercial inverters use SiC partially (in the form of fast reverse-recovery diodes or in multi-level topologies with a mix of Si devices). Additionally, in present-day designs, the SiC-based power stage uses a simplified packaging approach with discrete components. This approach prohibits realizing theoretical SiC advantages such as high current density. Recent advancements in power stage packaging based on additive manufacturing have shown promises for addressing those challenges for electric vehicle applications. Furthermore, other inverter attributes, such as magnetics and thermal design, are often neglected in SiC-based designs. Only simplified assumptions based on prior Si-based systems are used in the design, and those do not hold true for fast-switching SiC-based systems.

Prior work in magnetics for electrical machines and power converters shows that a rigorous multi-objective, optimization-based magnetic design could significantly improve the efficiency and power density of the magnetics. Such a design approach could be used to develop optimized magnetics for SiC inverters. For the controller design, a flexible approach can be used in which controller application-specific input-output and communication requirements can be easily integrated with the core controller hardware. Such modularity in controller hardware is uncommon in present-day inverters, in which each manufacturer develops application-specific hardware for each of its products. There is an urgent need to develop transformative design approaches for PV inverters to reduce the cost of PV power electronics, while significantly improving performance and reliability, to achieve the SunShot goal of enabling the interconnection and integration of hundreds of gigawatts of solar generation into the electric power system.

2. PROJECT OBJECTIVES

The overall project objective is to develop a high-power density, high-efficiency, low-cost solar inverter with advanced grid support functionalities for easier grid integration. In order to realize the objective, specific metrics have been defined in terms of inverter power block, magnetics, and controllers, i.e., a final power block power density greater than 75 W/in^3; a final inverter with a California Energy Commission (CEC) efficiency > 98%; a final inverter design with an estimated inverter cost <$0.125/W and estimated inverter lifetime >25 years; and grid support through advanced functions defined by

Institute of Electrical and Electronics Engineers (IEEE) 1547-2018 revision and communication capability.

All technical milestones in budget period 1 (BP1) and BP2 were achieved according to the original project schedule. The technical milestones in BP3 were partly delayed and were fully achieved in December 2018. The key milestones achieved are summarized as follows:

BP1 (9/30/2016):

1. Obtained alpha-prototype power block power density six times greater than the state-of-the-art string PV inverter power density (5–12 W/in^3)

2. Obtained alpha-prototype power block peak power conversion efficiency greater than or equal to 99%

3. Delivered magnetic design codes with execution time of less than 48 hours and convergence of total inductor losses within 10%

4. Demonstrated the functionality of an alpha-prototype controller supporting current control, voltage and frequency regulation, ramping, ride-through, and anti-islanding by controller hardware-in-the-loop (CHIL) testing

5. Obtained inverter power density three times greater than the state-of-the-art string PV inverter power density (5–12 W/in^3).

BP2 (9/30/2017):

1. Achieved short circuit response time of less than 5 µs for the gate driver protection circuit

2. Achieved absolute output inductance error <10% and incremental common mode input inductance error <10%

3. Demonstrated functionality of beta-prototype controller supporting current control, voltage and frequency regulation, ramping, ride-through, anti-islanding, and communication-based advanced inverter functions by CHIL testing

4. Achieved alpha-prototype inverter peak conversion efficiency of 98% or higher

5. Demonstrated functionality of the alpha-prototype inverter in terms of voltage and frequency disconnection, voltage and frequency ride-through, reactive power injection, and anti-islanding

BP3 (12/30/2018):

1. Achieved final inverter with CEC efficiency >98%, grid support thorough advanced functions defined by IEEE 1547-2018 revision, communication capability

2. Achieved final inverter design with estimated inverter cost < $0.125/W and estimated inverter lifetime >25 years

3. Achieved final inverter power density >20 W/in^3

4. Delivered high–power density, high-efficiency power block and prototype inverter, additive manufacturing techniques for power block and heat sink, magnetic design optimization tool, versatile

controller, standard HIL inverter testing techniques, and cost and reliability analysis of SiC-based PV inverter.

3. PROJECT RESULTS AND DISCUSSION

3.1 ALPHA INVERTER PROTOTYPE AND KEY IMPROVEMENTS IN BETA VERSION

3.1.1 Task 1: Power Block

3.1.1.1 SiC Device Characterization

The solar inverter market traditionally uses 1200 V Si devices for string inverters with DC link voltages of less than 1 kV and a typical power rating of 20 kW or less. For higher-power string inverters, particularly those coupled with the movement to higher DC link voltages for better inverter utilization and cost reduction, higher-voltage SiC devices are preferable. In this work, the emerging 1700 V bare dies of SiC MOSFETs and SiC Schottky diodes were used. The current ratings of single SiC MOSFET and SiC Schottky diode are around 34 A and 50 A, respectively. Since the bare dies were engineering samples from the device manufacturer with limited performance data, their static and dynamic characteristics needed to be evaluated for comprehensive power module and thermal design.

The temperature-dependent output characteristic of a single SiC MOSFET bare die with a gate voltage of 20 V is shown in Figure 1. With this gate voltage, the on-resistance $R_{ds,on}$ is mainly dominated by the drift region resistance, and thus a positive temperature coefficient output characteristic is presented. The positive temperature coefficient of on-resistance contributes to the current balancing of the multi-chip air-cooled module. At a junction temperature of 125°C, the on-resistance value of a single SiC MOSFET bare die is around 175 mΩ.

Anti-parallel SiC Schottky diodes were also characterized. The output characteristic of a single diode bare die for a range of junction temperatures up to 175°C is shown in Figure 2. As junction temperature increases, the threshold voltage decreases while the on-resistance increases. At a current level higher than 5 A, a positive temperature coefficient of resistance was observed; therefore, the selected anti-parallel diodes were suitable for parallel operation within the module.

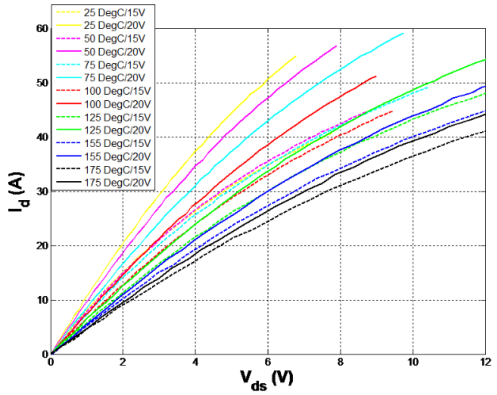


Figure 1. 1700 V SiC MOSFET output characteristics.

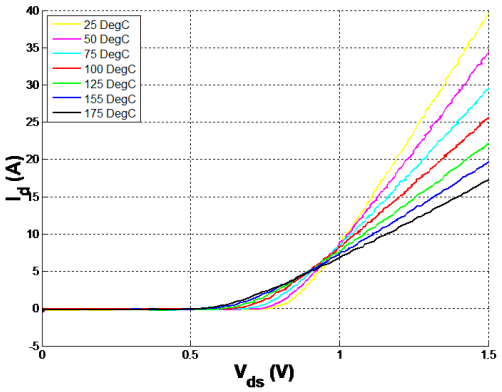


Figure 2. 1700 V SiC diode forward characteristics.

The switching behavior of the SiC MOSFET bare die was also characterized using the double-pulse test method. The temperature dependent turn-on and turn-off transient performance of the selected bare dies

were evaluated for switching loss estimation. The tests were performed under different drain currents and different operation temperatures, with a DC bus voltage of 600 V and gate resistance of 10 Ω. The same gate driver was used for the double-pulse test and the final inverter, with an output voltage from –5 to +20 V and a sinking/souring current capability of around 14 A. To keep the same switching speed for the inverter module, a gate resistance of 2 Ω was used for the five paralleled SiC MOSFETs. Within the plotted current and temperature range, turn-on energy decreased with temperature while turn-off energy increased with temperature, resulting in an almost constant total switching energy loss. The total switching energy loss under different temperature and current levels is shown in Figure 3. The temperature-insensitive feature would be beneficial for thermal stability under high-power and high-temperature operation.

3.1.1.2 Loss Calculation and Thermal Design

Based on the static and dynamic characteristics, the calculated total loss in one switch position is 123 W. This loss value was used as the heat source for the thermal design. The heat sinks were designed and optimized using a machine learning algorithm. Because of the high discontinuity of the solution space, non-convex objective function, and specific constraints of the problem, a population-based algorithm, i.e., a genetic algorithm (GA) (instead of gradient and Hessian-based algorithms) was used, which imitated the natural evolution process proposed in Darwinian evolutionary theory.

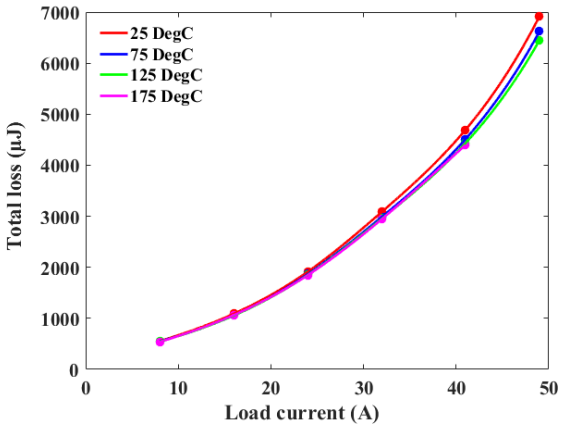


Figure 3. Total switching energy of single SiC MOSFET bare die.

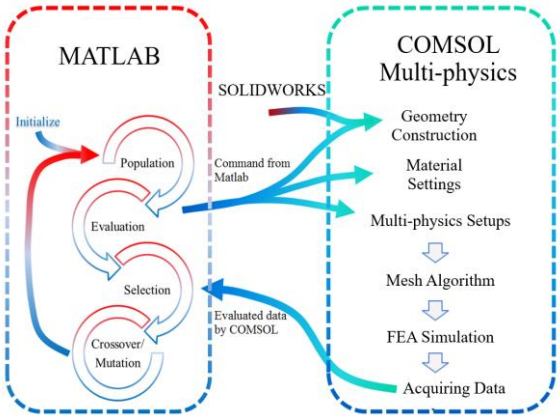


Figure 4. Automated co-simulation environment for heat sink optimization.

While a genetic algorithm, coded in MATLAB, was used to generate the design chromosomes of the heat sink, finite element analysis (FEA) simulations were used to evaluate the fitness value of each heat sink. For automation purposes, FEA simulation commands executed in COMSOL were directly invoked from the algorithms implemented in MATLAB. As shown in Figure 4, an automated interface between the optimization algorithm and the evaluation tool was created. All possible heat sink candidates were parameterized in MATLAB as a series of codes, like the DNA of a living creature. To decode the design, genetic expression was performed by sending construction commands to COMSOL based on the design instructions of chromosomes. In the meantime, other 3D mechanical models, such as semiconductor devices and substrate layouts, were directly imported from SOLIDWORKS automatically. The fitness evaluation was then carried out in COMSOL with the simulation setting command delivered from MATLAB. Upon completion of the FEA, the target performance—for example, the junction temperature of the module—was obtained and automatically sent back to the genetic algorithm in MATLAB. Then, a fitness value was assigned to the individual. After evaluation of the whole population, individuals with higher fitness values were provided better chances to pass their chromosomes to their offspring. The population of the next iteration was then generated by crossover, mutation, and recombination of the

selected chromosomes; and the genetic algorithm repeated a similar process until it converged to the final optimized result. The genetic algorithm–based heat sink optimization consisted mainly of five major steps.

1. Initialization: This step created random 2D extruded heat sink candidates with different combinations of cell patterns as the first-generation population in GA. The first generation, considering nine types of possible cell patterns (coded from 1 to 9), is shown in Figure 5. The numbers of the 4 × 9 matrix in Figure 5 represent all cell pattern combinations and form the cell distribution chromosome in the GA. 3 × 9 matrix was used to control the presence and absence of walls between any two vertically adjacent cells, which forms the wall-layout chromosome. The two chromosomes determine the DNA of one individual, i.e. the cross-section pattern of one heat sink candidate.

2. Evaluation and Selection: The temperature distribution for all individuals in the population was evaluated based on FEA thermal simulation in COMSOL. For a population of 21 individuals in this work, 16 individuals were picked as survivors for the next step based on the ranking of junction temperatures.

3. Crossover and Mutation: The 16 survivors in step (2) were then divided into eight independent couples for crossover and mutation. Specifically, each couple would produce two offspring to be used in the next step. The crossover was conducted by exchanging the matrix elements, and mutations were created by randomly changing a matrix element in the two chromosomes.

4. Recombination: In this step, five individuals were added to the population from the previous step (with 16 survivors). Specifically, an elitism operator was utilized to pick the best individual from the previous generation, so that it would be merged into the next generation. In addition, a migration operator was used to introduce four new individuals for the next generation.

5. Second-stage Perturbation: This step aimed to make a minor modification (e.g., a randomly change in a cell pattern) for the surviving heat sink candidates to further improve their thermal performance. The candidates with higher junction temperatures were replaced by better ones, and the design iteration was repeated until it converged to the best result.

   Following this optimization method, the finalized heat sink model for this inverter was selected (Figure 6). Because of the complexity of the heat sink design generated, traditional manufacturing methods could not be used, and 3D printing manufacturing technology was chosen to produce this design.

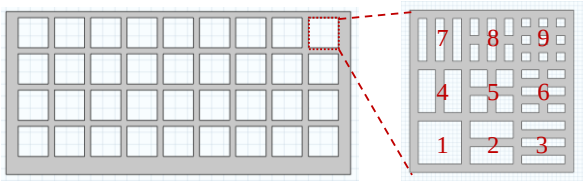


Figure 5. Initialization based on nine possible cell patterns.

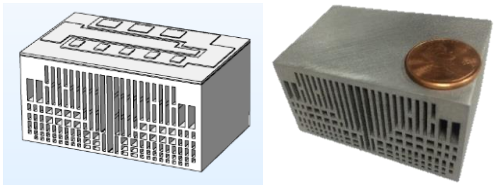


Figure 6. Genetic algorithm optimized heat sink.

A thermal simulation comparison of the heat sink optimized using GA (57×36×27 mm) with a customized solution (60.5× 36 ×32 mm) from a heat sink manufacturer (60.5×36×32 mm) is shown in Figures 7 and 8. The key simulation parameters remain the same. As can be observed, the junction temperature decreased from 108.3°C to 102.1°C when heat sink optimized by GA was used, and that design had a 27% smaller volume.

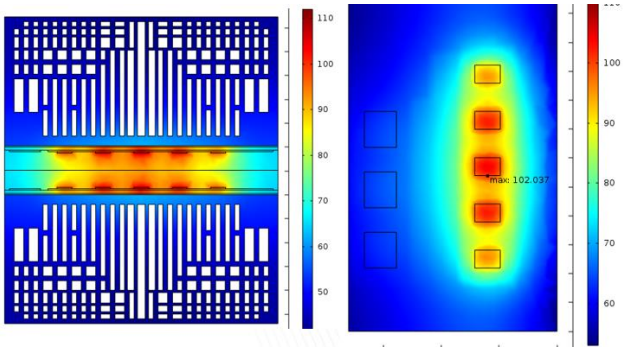


Figure 7. Thermal simulation result for GA optimized heat sink.

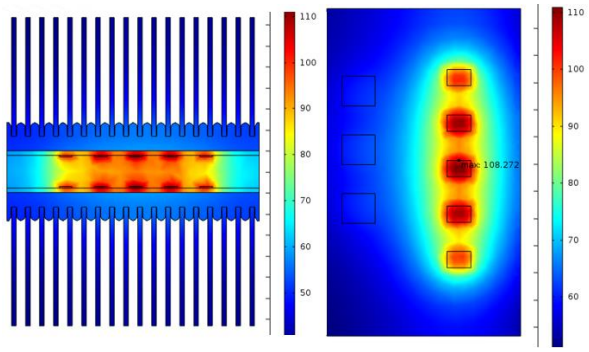
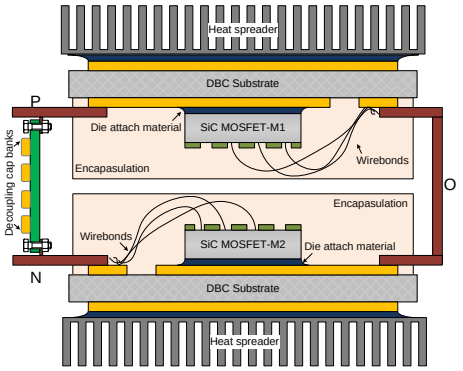


Figure 8. Thermal simulation result for customized heat sink.

3.1.1.3 Power Module Development and Evaluation

The proposed air-cooled module with a novel 3D packaging structure is shown in Figure 9, in which P, N, and O denote the positive, negative, and output terminals of the phase leg module configuration, respectively. The main objective of this structure is to increase the effective heat dissipation area through thermal decoupling for multiple chips. Because the phase leg module is split into two submodules—i.e., a high-side switch module and a low-side switch module attached to two separate heat sinks—the horizontal distance and associated heat dissipation area for each chip is enlarged, and thus the thermal coupling effect among the chips is well mitigated. This module design is an improvement on the previous design of a 3D-printed air-cooled module at Oak Ridge National Laboratory (ORNL). Each submodule consists of a direct bond copper (DBC) substrate attached to the flow channel via a thermal interface material. The aluminum flow channel is electrically insulated from the positive and negative DC bus by the aluminum nitride substrate. The high-voltage DC bus interconnects the power module from the left side of the air flow channel, and the gate driver and control interface on the right side. In addition, a decoupling circuit board, adjacent to the DC buses, is designed to minimize the power loop parasitic inductances and improve switching performance.

The fabrication procedures include several key steps: die attachment and pin attachment (gate/source pins), die interconnection using 5-mil aluminum wire bonds, power terminal attachment and strain relief, and encapsulation to protect the die and wire bonds from mechanical and chemical damage. The fabricated phase leg module used for single-phase continuous operation tests is shown in Figure 10, in which only the low-side switch of the phase leg module is shown. The high-side switch has exactly the same structure, which is stacked in reverse order on top of the low-side switch.



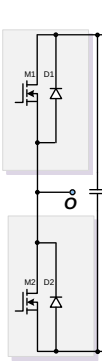


Figure 9. Proposed 3D packaging structure.

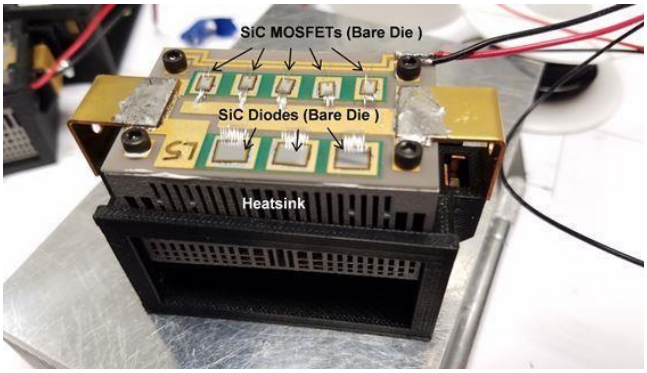


Figure 10. Fabricated phase-leg power module (low-side switch).

Before the 3-phase power stage was built, a buck converter setup was built to evaluate performance in continuous operation. The single-phase power block assembly with fan is shown in Figure 11. The volume of this single-phase power block without incorporating the fan and air duct is ~20 in^3. The phase leg power module is mounted within a 3D printed plastic housing with two air ducts (one for the high-side switch, one for the low-side switch) for even air flow sharing and reduced air pressure loss. The gate driver boards are mounted on the frontside of the housing, with pulse width modulation (PWM) signal input from the left side. The overcurrent protection component, i.e., solid-state circuit breaker, and DC link capacitors are mounted on the backside of the housing. A separate fan is also used to prevent the potential thermal runaway of the circuit breaker induced by its conduction power loss. In addition, two thermocouples are used to monitor the heat sink inlet and outlet temperatures.

For this test, the low-side SiC MOSFETs were reverse biased to serve as free-wheeling diodes. The LC filter was composed of an inductor of 0.2 mH and a capacitor of 100 μF, and a resistive load of around 10 Ω was used. The buck converter was operated with 1 kV input DC bus voltage and 40% duty-cycle, at a power level of ~11 kW. Figure 12 illustrates the continuous operating waveforms and measurement results with 1 kV DC bus voltage and 20 kHz switching frequency. As can be observed, for a 40% duty cycle, the inductor current is around 40 A and the ripple current is fairly high (~20 A) because of the relatively low switching frequency and reduced filtering inductance at high DC current bias. The continuous power test lasted for 10 minutes to reach the thermal steady state, and then the inlet and outlet air temperatures were measured. With an inlet air temperature of 28.8°C, the high-side and low-side outlet air temperatures were measured to be 74.8°C and 40.2°C, respectively.

The thermal performance of the designed power module was evaluated through FEA-based thermal simulation and then compared with the continuous experimental results. The switching and conduction losses of the high-side MOSFETs were calculated to be 220 W and 12.8 W, respectively, and the losses of the low-side free-wheeling diodes were calculated to have a loss of 22.8 W. The total calculated loss of the buck converter was 255.6 W, close to the power loss measured from the experiment (258 W).

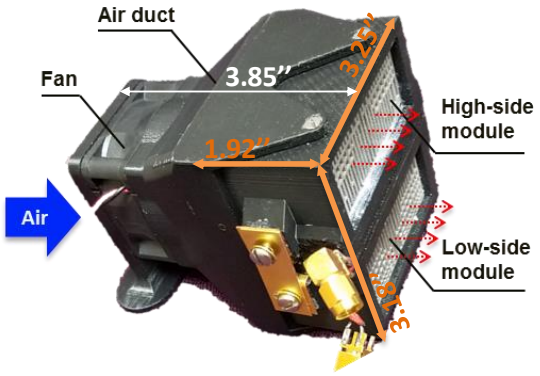


Figure 11. Single-phase power block assembly.

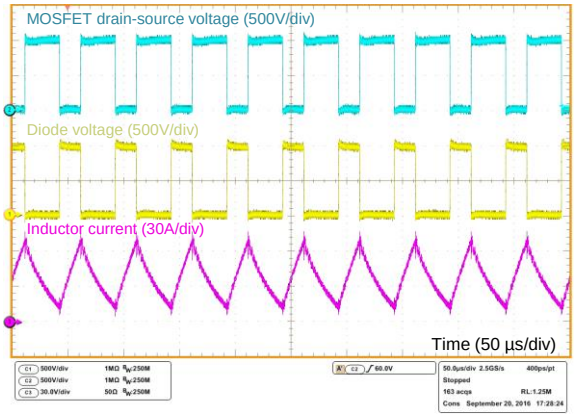


Figure 12. Experimental waveforms under 1 kV, 20 kHz buck operation.

Since the junction temperature of bare dies from the actual tests cannot be measured because of the special power module package structure (i.e., there is a lack of physical/visual access to the semiconductor devices), validation of other FEA thermal simulation results became critical to predict the operating junction temperature in the buck test. With the previously mentioned loss information and the fan curve, the temperature distribution of the module was simulated in COMSOL. Figure 13 shows the temperature of the outlet air and the heat sink outlet surface temperature. The air temperatures of the testing points (the locations of the thermocouple in the experiment) in the simulation were around 75°C at the high-side outlet and 38°C at the low-side outlet, which match well with the measured results (74.8°C and 40.2°C). Based on the validity of the thermal simulation, the operating junction temperatures could be estimated from the simulation results. In the simulation, a 100 µm thermal grease with a thermal conductivity of 0.8 W (m·K) was also assumed to emulate the real case more accurately. The temperature map of junction positions indicates that the maximum MOSFET junction temperature was about 131.5°C and the maximum diode junction temperature was around 70.5°C.

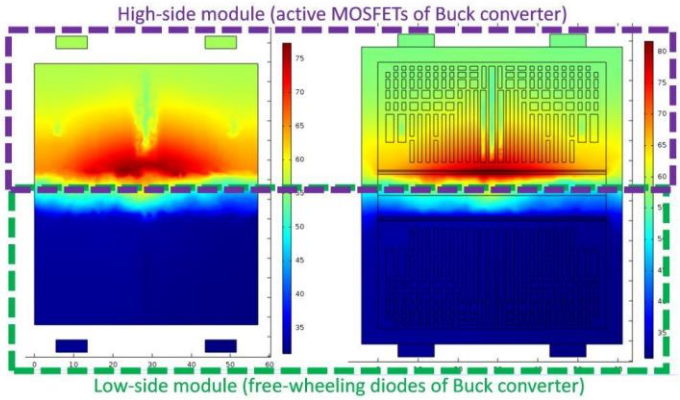


Figure 13. Thermal simulation results: outlet air temperature (left) and surface temperature of heat sink outlet (right).

3.1.1.4 Power Block Development and Evaluation

The actual hardware prototype of the 3-phase inverter is shown in Figure 14, with an overall volume of ~671 in^3. The power density for 50 kW operation is 75 W/in^3.

The inverter was tested in an open-loop configuration, with input power provided by a DC power supply. The performance of the inverter was evaluated at three input voltage levels: 800, 900, and 1000 V. In order to emulate a 480 V grid voltage, the inverter line-to-line output fundamental voltage was maintained at 480 V RMS by adjusting the modulation index at different DC bus voltage levels. The inverter was tested with an inductive load, consisting of an inductor of 0.9 mH and a step-change resistive load for different output active powers up to 48 kW.

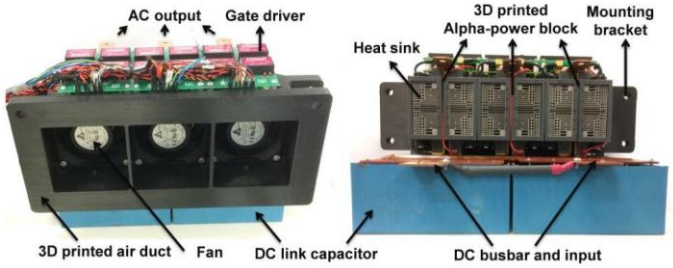


Figure 14. Hardware prototype of power block–based 50 kW 3-phase inverter: front view (left) and back view (right).

Figure 15 illustrates the 3-phase AC current at 1 kV DC bus voltage and 48 kW output power. The inverter AC output current is close to a pure sinusoidal wave, with some switching ripples and minor distortion at the zero-crossing point. The switching ripple can be better suppressed with higher filtering inductance and/or higher-order harmonic filters in future grid-tied operation. Based on the power analyzer measurement results, the inverter output AC current (I_{rms2}) was around 60 A RMS with a total harmonic distortion of ~2.5%. The inverter line-to-line fundamental RMS voltage was around 460 V (U_{rms4}). However, the overall inverter line-to-line RMS voltage (U_{rms2}) was much higher than the fundamental value because of the high switching ripple and its side-band harmonics. Therefore, the inverter output apparent power (SΣA) was much higher than its active power (PΣA). The inverter input and output active power were 48.15 kW and 47. 28 kW respectively, resulting in an efficiency of ~98.2%.

The CEC defined efficiency was also obtained for the purpose of rating and comparing efficiencies with those of other inverters. According to the CEC inverter test protocol, inverter efficiency numbers were measured at six power levels (10, 20, 30, 50, 75, and 100% of rated output AC power) and at three predefined DC voltage levels (V_{min} = 800 V, V_{nom} = 900 V, and V_{max} = 1000 V), as shown in Figure 16. Then, the CEC efficiency was calculated as a weighted average efficiency of these 18 values, with the following DC voltage independent weighting factors for the six power levels: 10% ~ 0.04, 20% ~ 0.05, 30% ~ 0.12, 50% ~ 0.21, 75% ~ 0.53, 100% ~ 0.05. The calculated CEC efficiency was 98.42% for the developed inverter.

An FEA simulation model was built in COMSOL to validate the thermal results obtained and to estimate the junction temperatures of the power semiconductors. The simulation was performed to obtain the estimated junction temperature. Based on the experimental loss data, the simulated temperature profile of the power module under rated operation is shown in Figure 17. The maximum junction temperature of the bare semiconductor die (MOSFET) was 103°C, and the temperature variation among the MOSFETs was within 10%. The junction temperature of the SiC diodes was ~ 65°C because of low conduction losses. While the junction temperature can be further promoted with higher output power and higher power density, the SiC device reliability and lifetime would be compromised.

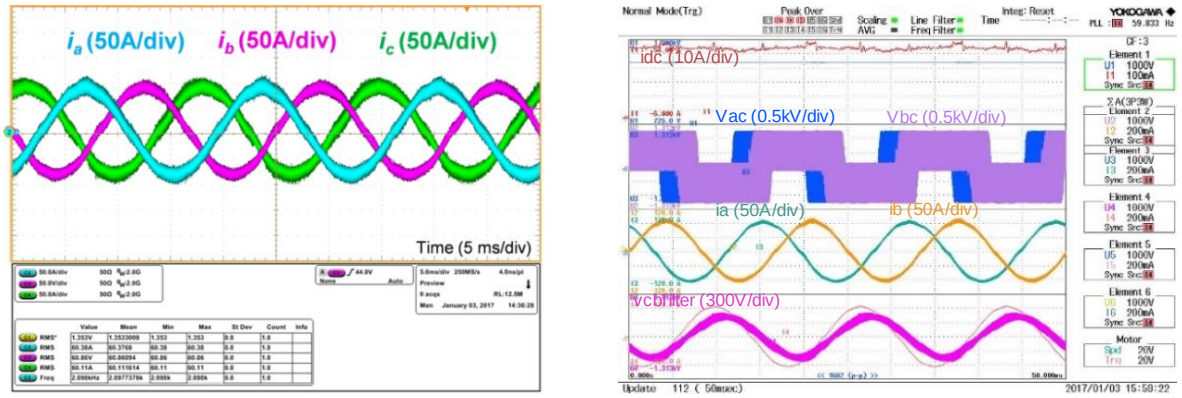


Figure 15. Three-phase AC current (top), power analyzer waveforms (middle) of the 3-phase inverter operating at 1 kV DC bus voltage and ~48 kW output power.

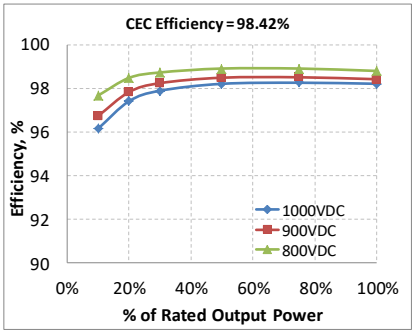


Figure 16. CEC efficiency of the inverter.

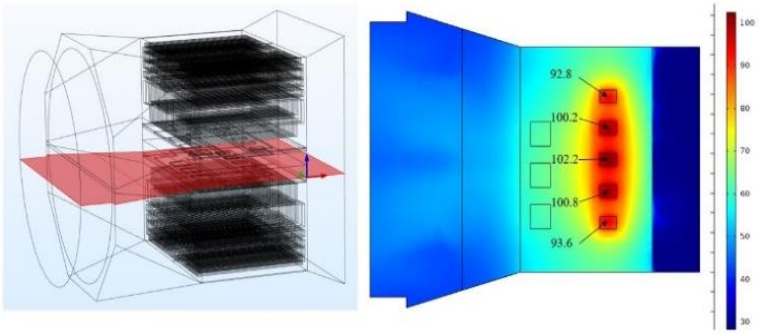


Figure 17. Thermal profile plots.

3.1.2 Task 2: Magnetics

Within the larger Sunlamp AMPVI system, specific consideration was given to the magnetic components found within the power electronic circuit. Optimizing the design of the AMPVI inductors yields reductions in overall packaging volume and total system weight. The Sunlamp AMPVI uses three inductors, as illustrated in Figure 18. These include two AC side inductors configured in an LCL filter (r_{fi}, L_{fi}, M_{fi}) and (r_{fl}, L_{fl}, M_{fl}), as well as a DC-side common mode inductor (r_{dc}, L_{dc}, M_{dc}). Over the course of the project, multi-objective optimization-based design codes for both the AC inductors and DC inductors have been developed. The design code for the common mode inductor continued development under a Small Business Innovation Research Project Phase II with the US Navy. This effort may result in licensing of the code. The code for the AC-side inductor will be documented in the second edition of the book *Power Magnetic Devices: A Multi-Objective Design Approach* by S. D. Sudhoff. Based on the results from these design codes, inductor designs were developed, constructed, and tested. Discussions in this report are a summary of the work performed.

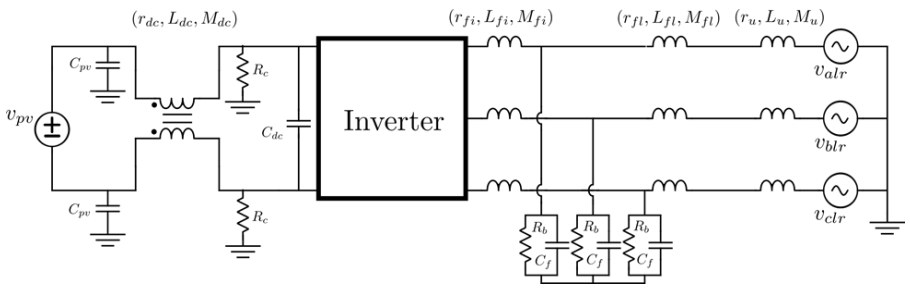


Figure 18. AMPVI circuit topology.

3.1.2.1 AC Filter Inductor Design Methodology

The output side of the inverter was connected directly to a 3-phase utility. To minimize inverter switching ripple being injected into the grid, an inductor-capacitor-inductor (LCL) filter was used. This LCL filter consisted of an inverter-side inductor (r_{fi}, L_{fi}, M_{fi}), a line-side inductor (r_{fl}, L_{fl}, M_{fl}), and three line-to-neutral connected capacitors (C_f).

The first task was to determine appropriate values for L_{fi}, L_{fl}, *and* C_f. To that end, metamodels of these components were constructed to predict volume as a function of component value. The capacitor metamodel was derived from commercially available capacitors, whereas the inductor metamodel was generated based upon a detailed design model prediction. With metamodels for the capacitors and inductors, an optimization could be run to select preliminary values for an effective yet compact AC filter. Ultimately, this optimization process determined target values of inductance of 188 µH for the inverter-side inductor and 35 µH for the line-side inductor.

To generate the inductor design model for the filter sizing optimization, decisions regarding the inductor topology first had to be made. When specifying a 3-phase inductor, the designer generally has two options to select from: independent phase inductors such as the U-I core inductors shown in Figure 19 or coupled phase inductors such as the E-I core inductors shown in Figure 20. For the 3-phase system, a single E-I core inductor could be used, whereas three U-I inductors would be required.

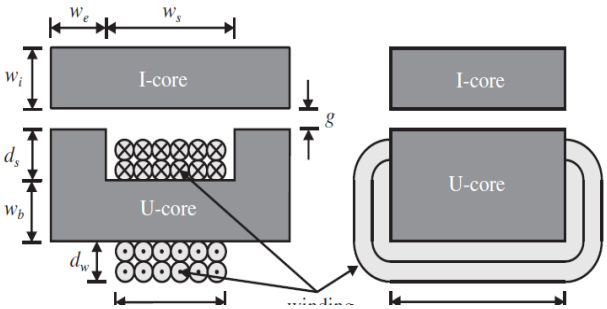


Figure 19. U-I Core inductor cross section and side view.

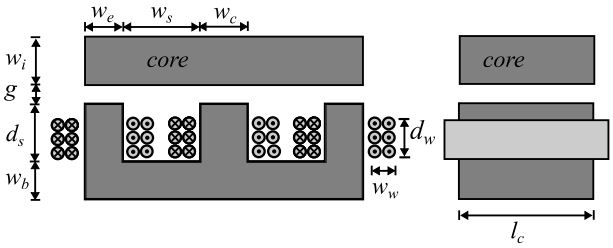


Figure 20. E-I core inductor cross section.

As Purdue has design models for the U-I core and E-I core inductors readily available, a comparison between the two approaches was generated for a 0.3 mH, 100 A_{rms} inductor. The comparison was run as a two-objective optimization concerned with minimizing both mass and volume. The results in Figure 21 show a clear advantage for the E-I core over using three discrete U-I core inductors in that, for any desired power loss limit, the mass of the E-I will be significantly less. However, the E-I core geometry

magnetic asymmetry causes variations in inductance over the excitation phase angle. Constraining the inductance variation to 5% resulted in the green curve of Figure 21, showing an increased mass design.

Because a uniform inductance was desired, a symmetric inductor topology was investigated. This investigation gave rise to the design of the Y core inductor of Figure 22. When the inductor was designed with a 3D Y core element, the flux paths of the inductor became inherently symmetric. A preliminary design model for the Y core was then generated and evaluated for the same operating conditions, resulting in the black curve of Figure 21 showing the Y core inductor to be superior for mass and loss. In light of the knowledge that the Y core inductor had this advantage, it was the topology selected for the Sunlamp AMPVI project.

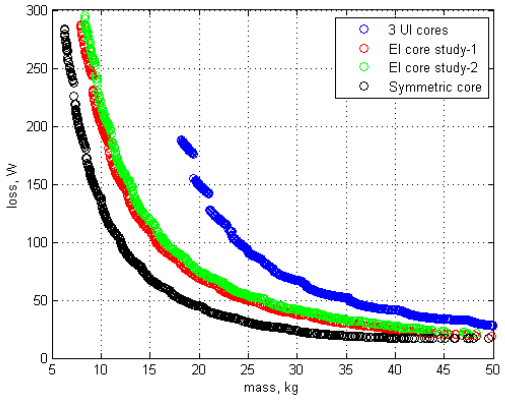


Figure 21. U-I, E-I, and Y core topology comparison.

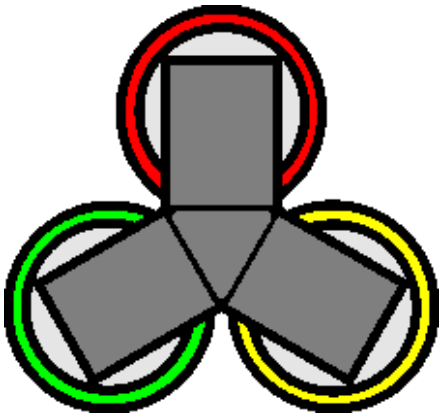


Figure 22. Y core profile view (phase windings in color).

The detailed design model for the Y core inductor had inputs including the desired inductance, the fundamental electrical frequency, and a time domain phase current waveform. A system-level reduced-complexity differential mode simulation of the inverter and LCL filter was used to generate this time domain current waveform. To reduce computational effort, the time domain current waveform was represented in terms of its main spectral features.

The available design space for the model contained components such as the core and coil geometry, number of turns in a coil, conductor size, and materials used in the core, coil, bobbin, and potting. These parameters are also subject to numerous geometrical constraints, such as ensuring positive dimensions, not exceeding a wire's minimum bending radius, and aspect ratio. Nongeometrical constraints on the model included maximum permissible mass, inductance tolerance, maximum permissible temperature limits, and electrical constraints such as the RMS current density. When the execution of the design model was completed, the resulting design's mass and loss were used as the metric to determine the design performance.

To evaluate the inductor design, four stages of modeling were evaluated: inductor geometry, magnetics, losses, and thermal performance. The geometrical calculations took a subset of independent geometrical values and generated all remaining design feature dimensions while ensuring that the mechanical constraints were satisfied.

The magnetic analysis used a technique known as magnetic equivalent circuits (MEC) to represent the magnetic flux paths in a circuit format. The inductor geometry was broken down into multiple paths that flux can potentially follow, as shown in Figure 23. These flux paths were then connected to one another to create flux paths throughout the inductor design, including primary paths and leakage or fringing paths.

The MEC was evaluated with respect to position in the stationary reference frame to find the inductance. Within the model, these inductances are subject to design constraints and tolerances.

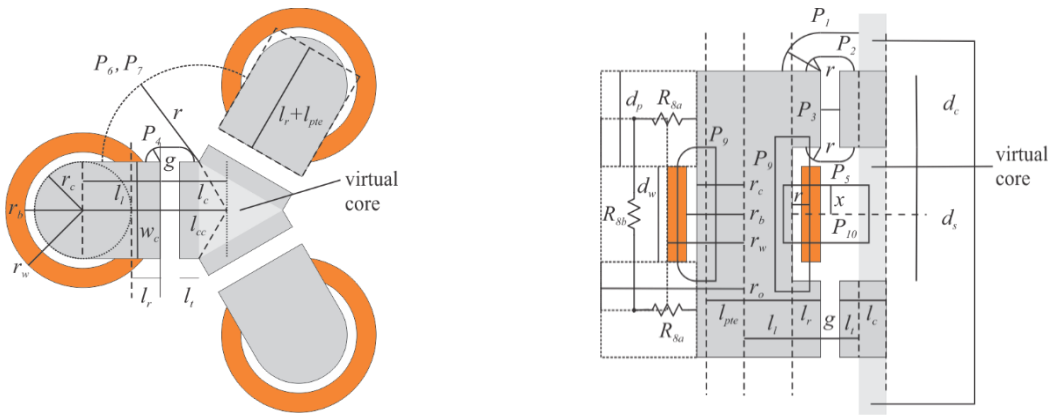


Figure 23. Y core AC inductor MEC flux paths.

In the first version of the code, core loss was computed using the fundamental component of the input current waveform evaluated with known characterized values of the material with a modified Steinmetz equation method. In later versions of the code, the impact of high-frequency eddy currents in the core was included. Based on the spectrum of the current waveform, an evaluation of the skin and proximity effect losses was computed. Including the winding conduction loss, all loss components could then be tallied to determine the total design loss. This loss was then used as the second metric in the multi-objective optimization process.

The thermal model consisted of a nodal thermal equivalent circuit (TEC)-based evaluation. The TEC takes in the prior computed dissipated power losses for various locations of the design and calculates the steady state temperature of the inductor features. The TEC was based on the symmetry-simplified mechanical representation of Figure 24 and then represented by the cuboidal or cylindrical elements shown in Figure 25. Each element was mapped to a material's thermal properties, with connections to one another or with ambient work to predict a steady state operating temperature. Some losses, such as wire conduction losses, were modified by temperature; therefore, the loss evaluation and TEC evaluation were repeated until convergence was reached and constraints could be checked.

During the Sunlamp AMPVI project, a genetic algorithm was used to run the inductor design code and generate optimized designs. From the desired input values and constraints, the Purdue optimizer GOSET progresses through multiple generations of designs; the process ultimately results in a Pareto-optimal front of designs, with each point on the curve representing a complete unique inductor design. A single point can be selected, and a full set of design details and results are produced. Upon completion of a design optimization run, the designer then can review the designs and ultimately select the design deemed most desirable for the project. In the case of the Sunlamp AMPVI project, once the team selected a specific design, further evaluation of the design was done using FEA to verify that the performance predicted by the inductor design model was accurate and that the correct inductance value was produced.

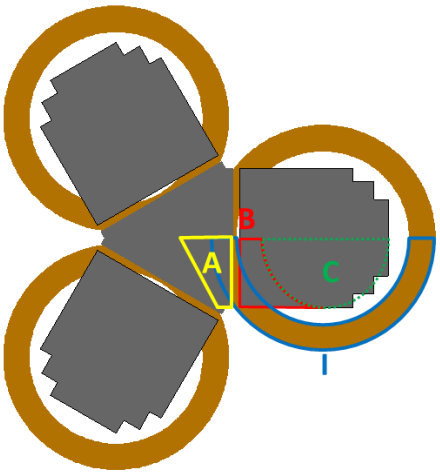


Figure 24. AC inductor TEC design.

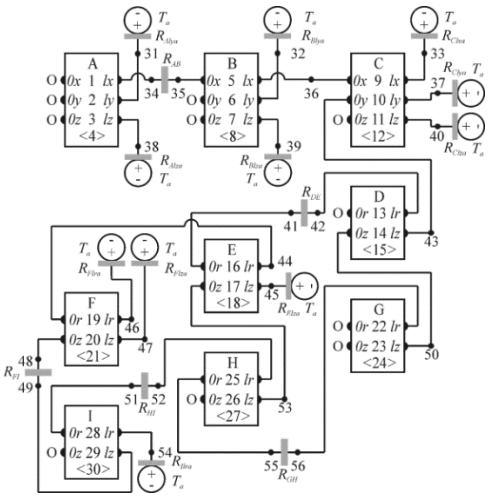


Figure 25. AC phase leg TEC model.

3.1.2.2 Alpha Prototype - AC Inductor

The LCL filter sizing optimization resulted in an alpha prototype inverter-side AC inductor sized at 188 µH. After running the design model and a team review of the resulting loss vs. mass performance, specific design 68 was selected to be built. The design's parameters were then transferred into an FEA simulation. The FEA results were compared with the analytical model in Figure 26, and the results demonstrated good agreement within the required 10% specification.

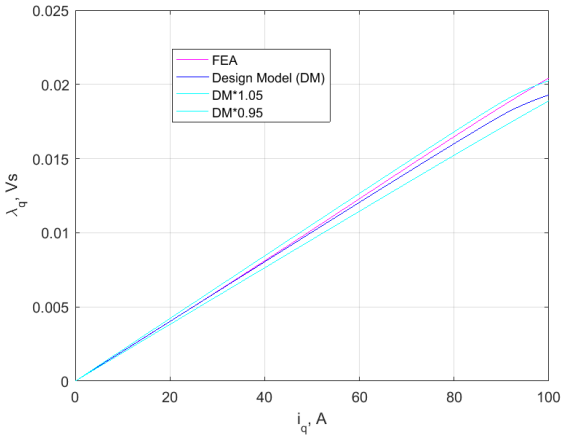


Figure 26. Inverter-side AC inductor magnetic performance comparison.

The same design methodology was followed for the line-side AC filter inductor, sized at 35 µH. Discussion of the line-side inductor is omitted for brevity. Both the inverter-side and line-side inductors were fabricated within the Purdue laboratories and tested for design model and project compliance. The completed alpha prototype AC inductors are depicted in Figure 27.

Figure 27. Alpha prototype AC inductors: line side (left), inverter side (right).

Testing began with electrical safety tests to ensure that the inductors were fit for use in high-power, high-voltage systems. Both inductors passed the electrical safety tests and were then subjected to functional tests to validate the core parameters of the as-built inductors against the design model predictions. The primary validation test evaluated the *q*-axis and *d*-axis flux-linkage versus current characteristics through the full range of operation and into magnetic saturation. Thermal testing was also performed to determine if the inductors would be safe to operate under loaded conditions and to validate the thermal model. Test results largely validated the model predictions. Where minor discrepancies arose, consideration was given to model revisions to improve accuracy further.

Modifications were made to the design model and the improvements were applied to the beta prototype. The main design model modification was with respect to the method utilized to predict core loss. During testing, power dissipation exceeding the model prediction was noted. Core loss prediction in the design model was complicated by the fact that, strictly speaking, superposition/spectral decomposition cannot be applied. Models capable of loss prediction for complex flux density waveforms, such as the Jiles-Atherton and Praisach models, are computationally intense and do not account for eddy currents, and so are not applicable. Thus, in the original version of the design code, the core loss calculation was based on the Modified Steinmetz equation applied to the low-frequency component of the flux density. This approach was found to be inadequate with high-silicon-content steel for conditions of high flux-density ripple, so a revised loss model had to be developed. This was done by assuming that hysteresis loss was driven by the low-frequency portion of the waveform, and eddy current loss was dominated by the switching-frequency components of the waveform. Since eddy currents are a linear phenomenon, superposition should apply. Such an approach may miscalculate the hysteresis component of the loss, but that component was small for the class of materials being considered. To test the new loss model, lab testing was performed by driving the inductor *d*-axis configuration in series with a resistive load, with an H-bridge operating at 20 kHz. The new model prediction compared with lab tests found a total loss error of only 4%, which was deemed satisfactory.

This new core loss evaluation was also important in the conversation of switching frequency. After evaluating the performance of the alpha prototype inverter, the team agreed that boosting the switching frequency to 50 kHz was feasible and could better utilize the SiC switches. For the magnetics, shifting to a 50 kHz switching frequency offered the opportunity for significantly smaller volume while also dissipating less loss, as demonstrated in Figure 28. However, the high-silicon-content steel laminations used in the alpha prototype would no longer be suitable for use. To better accommodate the 20 kHz switching and to be capable of supporting 50 kHz switching, the move to a nanocrystalline core material

was made. While it is a more expensive material, the lower losses in the range of tens of kHz made it an excellent candidate for the beta prototype.

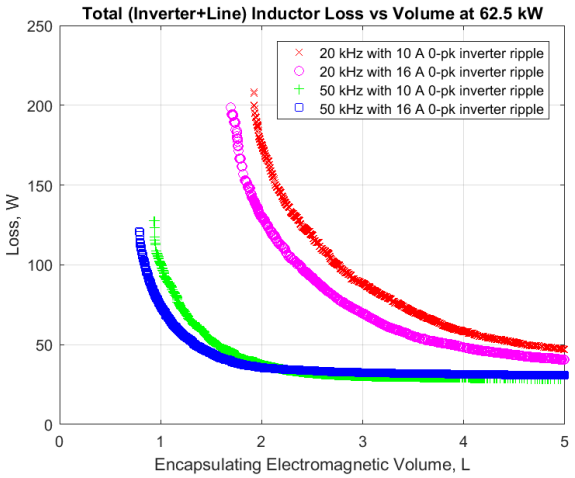


Figure 28. The 20 kHz versus 50 kHz switching frequency impact on AC filter inductor pareto-optimal fronts.

With the transition to nanocrystalline cores, the previously used core mounting points were no longer available, requiring a redesign of the packaging. With the packaging redesign shown in Figure 29 in place, assembly of the inductor was also simplified, and air gap consistency was improved.

The core shape change and revision in packaging also required a revision of the TEC. This included a restructuring of the segmented sections of the core to better reflect the new C core geometry. TEC modifications were also made as illustrated in Figure 30 to represent the bobbin with additional fidelity, including reevaluation of surfaces that can be best modeled as adiabatic heat flows.

Figure 29. Cutaway view of beta prototype mechanical structure.

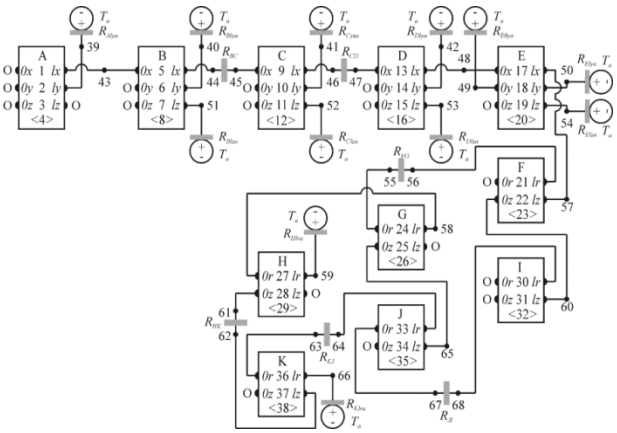


Figure 30. Revised beta prototype TEC.

3.1.2.3 DC Common Mode Choke Inductor Design Methodology

On the dc side of the inverter system shown in Figure 18, the primary magnetic component is the dc link common mode inductor (CMI). This inductor serves to reduce the magnitude of common mode (CM)

currents. The first step in the design of the inductor is to translate the circuit diagram of Figure 18 into the CM equivalent circuit shown in Figure 31. The overall CM equivalent circuit can also be taken as a worst-case evaluation when the utility-side neutral is grounded. An additional factor to consider in the worst-case analysis is an infinite PV-side capacitance and no CM inductance present in the AC-side filter inductors. With these assumptions, the CM equivalent circuit of Figure 31 can be reduced to the worst-case scenario of Figure 32. In the worst-case condition, the principle circuit element serving to impede CM current flow is the DC-side CM inductance. Because of the RLC (resistor-inductor-capacitor) nature of this reduced order circuit, it also becomes imperative that the capacitive impedance be much less than the inductive impedance to avoid resonances.

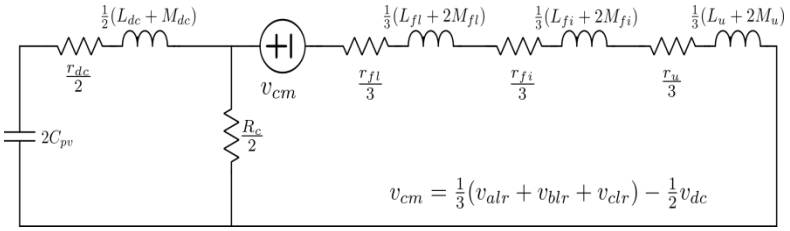


Figure 31. AMPVI CM equivalent circuit.

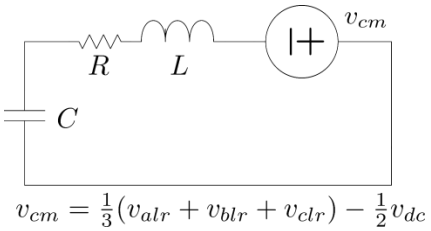


Figure 32. Worst-case reduced CM equivalent circuit.

To evaluate the magnitude of the CM voltage source, the inverter modulation strategy must be considered. Two common types of modulation, space vector PWM and sine-triangle PWM were considered. The CM flux linkage can be calculated by taking the integral of the time domain simulation of the CM voltage generated by a switching strategy. Comparing the resulting flux linkage waveforms in Figure 33 demonstrates a clear difference in magnitude. Space vector modulation exhibits a third harmonic CM voltage of 180 Hz. This large-magnitude third harmonic component of the space vector-based flux linkage is not generated when using the sine-triangle modulation strategy. Comparing the mass versus loss characteristics of the CMI with required third harmonic filtering, with that of a CMI without required third harmonic filtering, showed an order-of-magnitude of loss and mass advantage in favor of not having a third harmonic. This base analysis helped to drive decisions for the selected AMPVI modulation strategy, as well as to determine what magnetic materials were appropriate for the required frequencies.

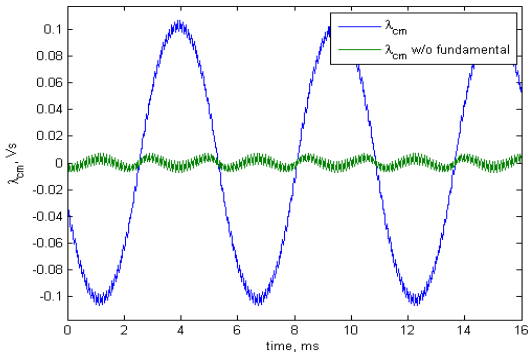


Figure 33. Flux linkage: space vector (blue) and sine-triangle PWM (green).

When analyzing the time domain CM currents, it became apparent that some challenges were present. The CM currents were a-periodic, varying in both amplitude and shape over time. As this a-periodic wave-shape analysis would not be computationally efficient for optimization-based design, a proxy

current waveform was developed. To maintain validity in analysis, this proxy waveform was constrained to have the same peak value as the original waveform, the same RMS value as the original waveform, and the same RMS value of the flux linkage time derivative. These constraints ensured that the proxy waveform will have the same impact on magnetic saturation, resistive losses, and proximity effect losses.

With the proxy CM waveforms serving as the base input, a design code was constructed. A design space was created to include the core and coil geometries, number of coil turns, coil conductor sizing, and provisions for core material selection. Constraints were put into place to limit items such as mass, aspect ratio, current density, peak common mode current, and RMS CM current. Upon completion of an iteration of the design code, the mass and loss were metrics to determine a design's performance.

To evaluate the inductor design, four stages of modeling were evaluated: inductor geometry, magnetics, losses, and thermal performance. The geometrical calculations took the specified geometrical values and generated all remaining design feature dimensions while ensuring that the mechanical constraints were satisfied.

The magnetic analysis used a nonlinear MEC technique to represent the magnetic flux paths in a circuit format. The MEC element representation of the CMI, coupled with the proxy flux density waveforms, calculated a CM current waveform and the core losses. The CM current waveform was then used to evaluate additional losses of the design, such as DC resistive loss, AC resistive loss, and proximity effect loss. These losses were summed to yield the total loss.

The thermal model consisted of a nodal TEC-based evaluation. The TEC took the computed dissipated power for various locations of the design and calculated the steady state temperature of the inductor features. The TEC was based on a symmetry-simplified mechanical view and then represented by cuboidal or cylindrical elements. Elements were mapped to a material's thermal properties, and connections to one another or ambient air predicted a steady state operating temperature. Some losses, such as wire conduction loss, were modified by temperature; therefore, the loss evaluation and TEC evaluation were repeated until convergence was reached and constraints could be checked.

With a complete design model, a given set of desired inductor performance parameters and constraints permitted the full design and analysis of a CMI. The design model generated all details that pertained to a complete inductor design and made them available for review. Using this model, an optimization engine could use the model to generate optimized designs. From the desired input values and constraints, Purdue's GOSET optimizer was used to generate Pareto-optimal front of designs. All points on this curve represented unique, complete inductor designs. Upon completion of a design optimization run, the designer then had the opportunity to review the designs and ultimately selected the design deemed most desirable for the project. In the case of the Sunlamp project, once the team chose a specific design, further evaluation of the design was done using FEA to verify that the performance predicted by the inductor design model was accurate and that the correct inductance value was produced.

3.1.2.4 Alpha Prototype – DC Common Mode Inductor

With a completed CMI design code in place, a design optimization was run. In all studies, the goal was to achieve an RMS common mode current of less than 83.3 mA. The CMI design code was then run to generate a Pareto-optimal front of designs for review. Multiple runs were made to better understand differences such as core materials, with ferrite having much lower losses than steel.

Note that the CMI performs best with a continuous core (no air gap). However, the design used two UR shaped cores that were connected together to facilitate a bobbin-based winding. Inherently, two mating surfaces will never have a truly zero air gap; even perfectly machined parts retain some surface roughness

that results in some level of air gap, which reduces the resulting CMI inductance. This characteristic was tested experimentally and in FEA to determine how much of an air gap may be present in the final design. By fabricating a test inductor with commercially available UR cores, a flux linkage versus current profile was generated. When these results were plotted against the FEA results for zero air gap as in Figure 34, a large discrepancy became apparent. The measured results showed a significantly gentler knee in the flux linkage versus current waveform than the FEA predicted. However, acknowledging the inevitable presence of an air gap between the two cores, the FEA could be run with a small effective air gap. When the FEA was executed with an air gap equal to 27 µm, the resulting magenta trace in Figure 34 showed very strong correlation with the tested sample. This test case shows that care must be taken to account for the small air gaps of an assembled design in the design model.

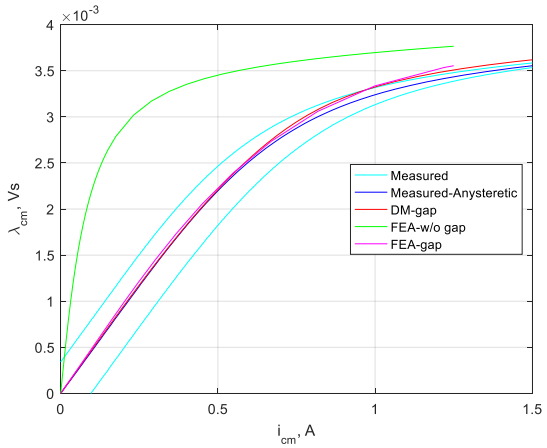


Figure 34. CMI flux linkage versus current.

Design number 193 was selected for the alpha prototype CMI, and its parameters were transferred to an FEA simulation. The FEA compared with the analytical model in Fig 35 demonstrates good agreement, within the specification of 10% dictated by project goals. The CMI was fabricated in Purdue laboratories and thoroughly tested for design model and project compliance. The completed alpha prototype CMI is depicted in Figure 36.

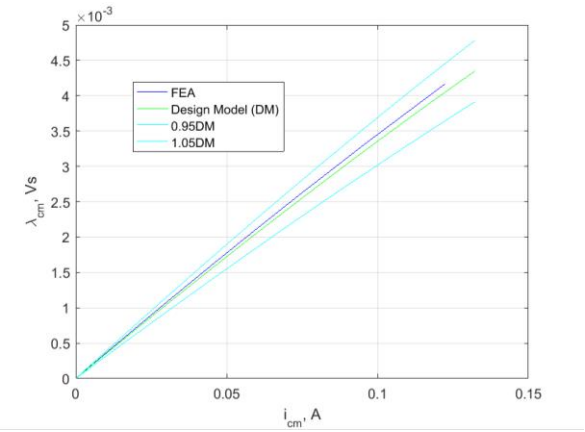


Figure 35. CMI magnetic performance: analytical versus FEA.

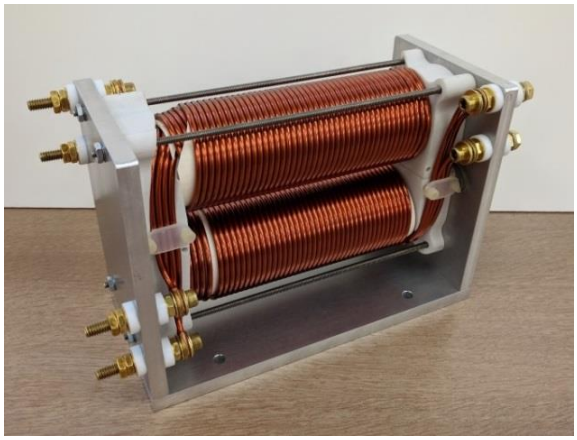


Figure 36. As-built common mode inductor design 193.

During testing, an immediate concern was noted with respect to the inductor's resonance point, as the resulting parasitic capacitance was out of specification. An initial capacitance model of the CMI estimated that the inductor would exhibit a shunt CM capacitance of 280 pF; it was later measured at 260 pF. Unfortunately, this value placed the first resonance of the CM impedance at 50 kHz, which was lower than desired, as there is some third harmonic content of the common mode voltage at 60 kHz. It was calculated that adding Nomex paper between the coil layers would reduce the CM capacitance to 45 pF. However, when the inductor was rewound in this configuration, a capacitance of 97 pF was measured. Although that was a large discrepancy, the change pushed the resonance frequency to 84 kHz, which is acceptable for the application. The differential mode showed a minimal impedance of approximately 2 µH as desired.

Additional testing included electrical safety tests and functional tests. To validate the inductance of the CMI, flux linkage versus current measurements were taken. These flux linkage versus current data were then processed to show incremental inductance versus current, as in Figure 37. The unknown air gap due to surface roughness had to be considered to compare the model-predicted to measured inductance. In the case of Figure 37, the model was set with an air gap of 8 µm, yielding a strong correlation of the model and as-built tests. This 8 µm was plausible for the surface roughness-based air gap.

Finally, thermal testing was performed and revealed no concerns regarding operation. The test results largely validated expectations for the inductor based on model predictions. Where minor discrepancies arose, consideration was given to model revisions to improve accuracy.

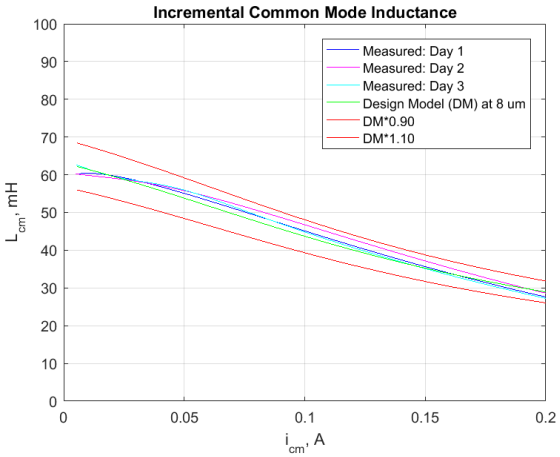


Figure 37. CMI incremental common mode inductance.

3.1.2.5 Design Model Modifications and Improvements Applied to Beta Prototype

The primary refinement was made to the prediction of CM capacitance. With the proposed move to 50 kHz switching, the resonance of the CMI needed to be pushed higher. As switching frequency increased, the required inductance decreased, making the resulting LC resonance point much more sensitive to accurate prediction of the parasitic capacitance. A highly detailed capacitance model was included in the design code, including the layer-to-layer capacitance, the capacitance that results from the electric fields between the core posts, and the capacitance that results from the electric field between the innermost layer of the winding and the core. These capacitances are strong functions of the details of the winding, the connections, the layer-to-layer insulation, and the potting and bobbin materials.

In testing, it was found that the large-signal inductance was appreciably higher than the small-signal inductance. This difference was attributed to magnetic hysteresis, and a time domain hysteresis model was implemented in the design code. This additional model yielded an appropriate reduction in average slope that represented a much better prediction of the RMS common mode current.

Finally, the original TEC was updated to include the plastic structure of the bobbin, which assisted in incorporating the thermal penalty of the support structure, as well as a provision for a heat sink to provide cooling for the cores. The TEC was also updated to reflect variable amounts of insulating paper between successive coil layers used in capacitance manipulation. The beta prototype CMI TEC revision updates to the thermal model mechanical segmenting and TEC layout are depicted in Figure 38 and Figure 39, respectively.

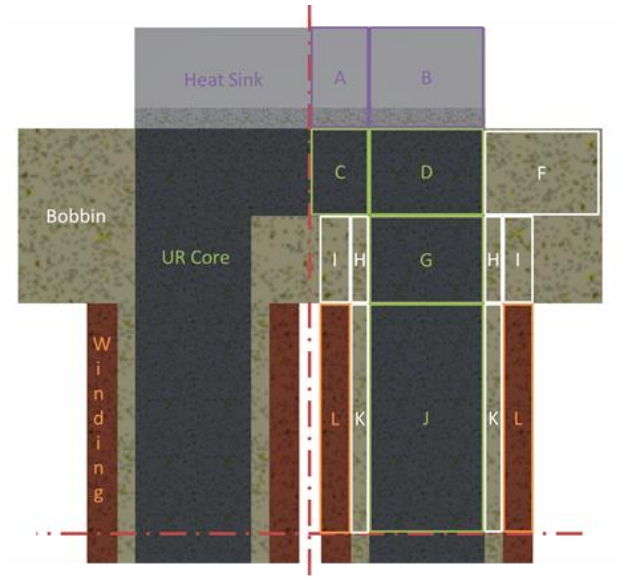


Figure 38. CMI TEC segmenting revision.

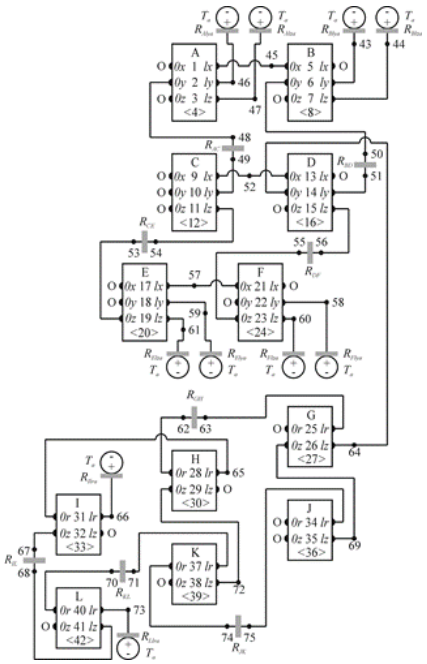


Figure 39. CMI TEC model revision.

The final modification to the CMI design was a redesign of the mechanical packaging structure. In the alpha design, the inductor was contained within an aluminum chassis for strength and robustness; and a thermal transfer pad was installed to connect the cores to the chassis, using the chassis as a heat sink to increase thermal performance. However, in application, the chassis would be grounded and thus the cores would also be electrically grounded. This grounding of the cores had the unintended consequence of creating additional penalty capacitance in the inductor. For the beta prototypes, the cores were intentionally left electrically isolated to prevent extra capacitance of a grounded surface in close proximity to the winding. This new requirement necessitated a full redesign of the mechanical structure, so the opportunity was taken to also modify the design for ease of assembly. A cutaway view of the new mechanical structure is illustrated in Figure 40.

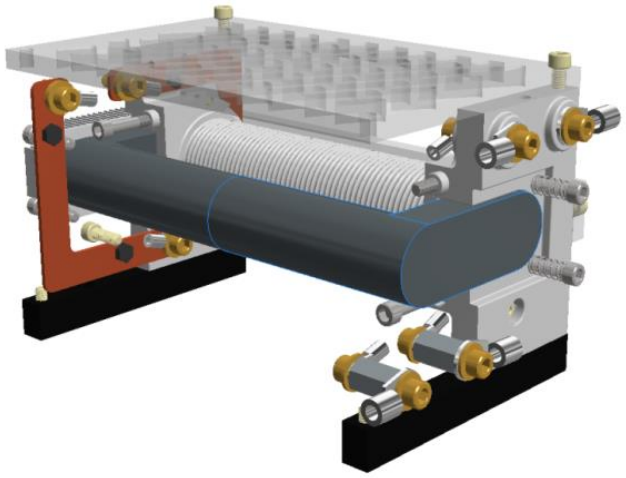


Figure 40. Cutaway rendering of beta CMI.

3.1.3 Task 3: Controller Board and Control Algorithms

The objective of this task was to develop a flexible inverter controller using a motherboard-daughterboard concept that can satisfy functional requirements for the PV inverter. Control algorithms were developed and implemented in the new controller board to provide advanced grid support functions such as voltage regulation, frequency regulation, ramping, ride-through, and anti-islanding. These controls were then implemented and validated using a developed CHIL setup for fast switching converters. Furthermore, DNP3 communication capability was developed for the inverter controller to enable interoperability. The inverter interoperability was also validated through the CHIL setup. The developed controller was interfaced with both the alpha inverter prototype and the gamma inverter prototype. The control algorithms were validated through experimental results in single-inverter grid-connected mode as well as power-hardware-in-the loop (PHIL) mode. This section presents various developments, evaluations, and validations to demonstrate the accomplishments in this task.

3.1.3.1 Prototype Controller

Controller Hardware—The first effort under this task was to select a control board architecture that can provide computing power for advanced inverter control algorithms, PWM outputs with high resolution for SiC MOSFET switching, fast analog-to-digital conversions for sensor inputs, and various analog-digital inputs-outputs (IOs) for auxiliary functions such as relays. Several commercially available controller boards with digital signal processors (DSPs) and/or FPGAs were compared. Current state-of-the-art embedded inverter controller design is based on a three-chip solution including an FPGA for fast low-level protection and custom PWM algorithms; a DSP for 3-phase transformations, feedback loops, and power computations; and a microprocessor for data logging and networking.

The design using the General-Purpose Inverter Controller (GPIC) and single-board RIO (sbRIO) leverages years of National Instruments (NI) embedded expertise [1]. The sbRIO is based on the Xilinx Zynq 7000 reconfigurable system-on-a-chip (RSOC). The RSOC integrates the capabilities of an FGPA and a DSP in one chip. NI has integrated this chip along with a dual-core 667 MHz ARM Cortex-A9 processor onto the sbRIO 9607. The FPGA, DSP, and microprocessor functionalities can all be programmed using the intuitive LabVIEW graphical programming language. The GPIC was designed by NI in collaboration with NREL to meet the needs of current and future inverters. The additional hardware

design required integration of the various inverter power supplies and, optionally, integration of gate drive circuitry to exploit the native FPGA TTL (transistor-transistor logic) outputs (vs. existing GPIC half-bridge DO outputs). The platform allows high-speed communication between the FPGA and DSP algorithms and can facilitate loop rates in the MHz range. This facilitates not only the development of higher-switching-frequency converters, but also the incorporation of complex advanced control algorithms such as model predictive control, which requires a complete model of the physical device to be executed on the controller in real-time.

The sbRIO (NI 9607) is composed of a Xilinx Zynq-7000, 667 MHz dual-core ARM Cortex-A9 processor, an Artix-7 FPGA, and a mezzanine card connector that is used to connect with GPIC (NI 9683). The NI 9683 provides various IOs for inverter control, such as 16 simultaneous analog input channels, 8 scanned analog input channels, 8 analog output channels, 28 sourcing digital input channels, 14 half-bridge digital output channels, 24 sinking digital output channels, 4 relay control digital output channels, and 32 digital I/O channels to the FPGA. The motherboard sbRIO (NI 9607) and daughterboard GPIC (NI 9683) configuration of the controller provides an economic advantage in that the sbRIO is commercially used in various other applications, thus making it available for high-volume pricing.

Interface Design—Even though commercially available, off-the-shelf primary controller boards were selected for the alpha-prototype controller, one of the tasks was focused on developing the interface board that could connect the controller board signals to the power block gate drivers. The interface board was also designed to host various low-power DC supplies to provide suitable DC voltages to the gate driver circuits, to the controller board, and to the sensors. In collaboration with ORNL, pin layout, power requirements, impedance, and voltage matching requirements were analyzed for the interface board. Two interface boards for the prototype controller designed were developed and validated.

These two interface boards were built to stack on top of the NI GPIC and sbRIO. The first board was a breakout board. The purpose of the breakout board was twofold: (1) to provide convenient, noise-immune, and space-optimized connections to all the GPIC IO signals, and (2) to incorporate noise-immune high-speed signaling circuitry for the gate drive outputs, allowing direct use of the sbRIO FPGA 40 MHz LVTTL outputs. For the high-speed gate drive functionality, RS422 differential signaling was selected to maximize noise immunity. The breakout board included LVTTL-RS422 transmitter chips. Matching receiver chips will need to be incorporated on the power block gate driver boards. The second board was a power supply board that provides power at various voltage levels required by external devices, including the power block and transducers. The power supply board includes signal conditioning for the 24 Vdc input and outputs +12 Vdc, + 5 Vdc, and +3.3 Vdc required by the power block gate driver, and ± 15 Vdc for the current and voltage transducers. A picture of the complete alpha-controller assembly, including NI sbRIO, NI GPIC, breakout board, and power supply board is shown in **Error! R eference source not found.**.

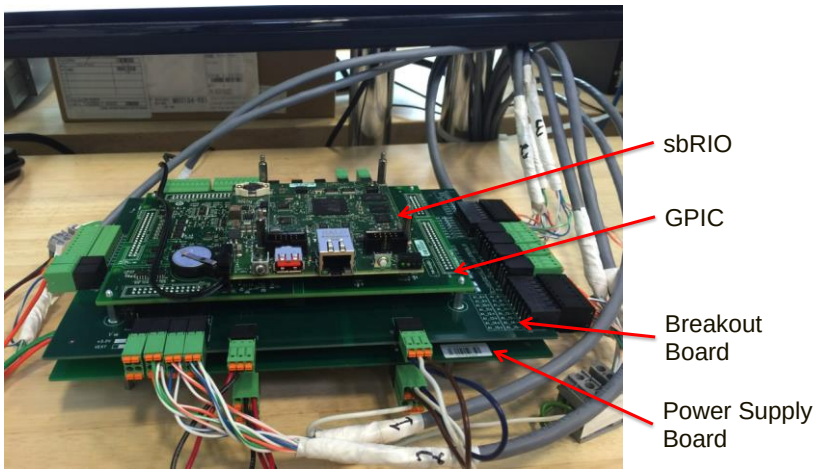


Figure 41. Picture of the complete alpha-controller assembly.

3.1.3.2 Control Algorithms

Inverter Model Description—A detailed transient-domain, switching model of the 50 kW, 3-phase, transformer-less inverter was built initially in PLECS software. It was then converted to Simulink SimPowerSystems for implementing advanced control functions. The model also included leakage capacitances that emulate the leakage capacitance of a PV panel to the ground. Ideal switch and diode models were used in the simulation. Space-vector PWM (SVPWM) was used in these initial simulations. The general objective of SVPWM is to control six switches so that the inverter output currents follow the reference currents. The switching frequency used in the simulation was 20 kHz. A *dq0* axis-based current control was employed for the SVPWM. A large number of simulations were completed to validate inverter current controls and four-quadrant operations with respect to various PV leakage impedances and grid impedances. The higher harmonics seen in the current were due to the presence of PV leakage capacitance, which required the design of the dc-link inductor (as discussed earlier) to reduce the leakage current. Then the SVPWM was replaced with sine PWM (SPWM) in the current controller in order to mitigate third harmonic components in the common mode flux linkage for the dc-link inductor.

Advanced Grid-Support Functions—Based on the transient-domain inverter model and the current control, advanced inverter control functions including volt-VAR (VVAR), volt-watt (VW), and frequency-watt (FW) were developed. The signals measured for the advanced inverter functions were the 3-phase RMS voltage from the grid side and the frequency of the grid. Depending on these signals, the real and reactive power references were generated by the VW, FW, and VVAR functions. The real and reactive power references were checked to make sure they stayed within the apparent power limit. Then, using these two references, the RMS current reference and the phase angle of the current reference were generated and sent to the lower-level PWM signal generator.

The VVAR, VW, and FW implementation in SimPowerSystems platform is shown in Figure 42. This representation has three parts to it: the inputs used to obtain the reference points, the controllers used, and the outputs that drive the lower-level inverter current control. This architecture uses 3-phase sinusoidal grid waveforms (at point-of-common-coupling, or PCC), frequency measurement (at PCC), and finally the apparent power limit on the inverter. For voltage regulation, VVAR and VW controllers generate real and reactive power references respectively to control the voltage. The curves used for these controls are shown in Figure 43.

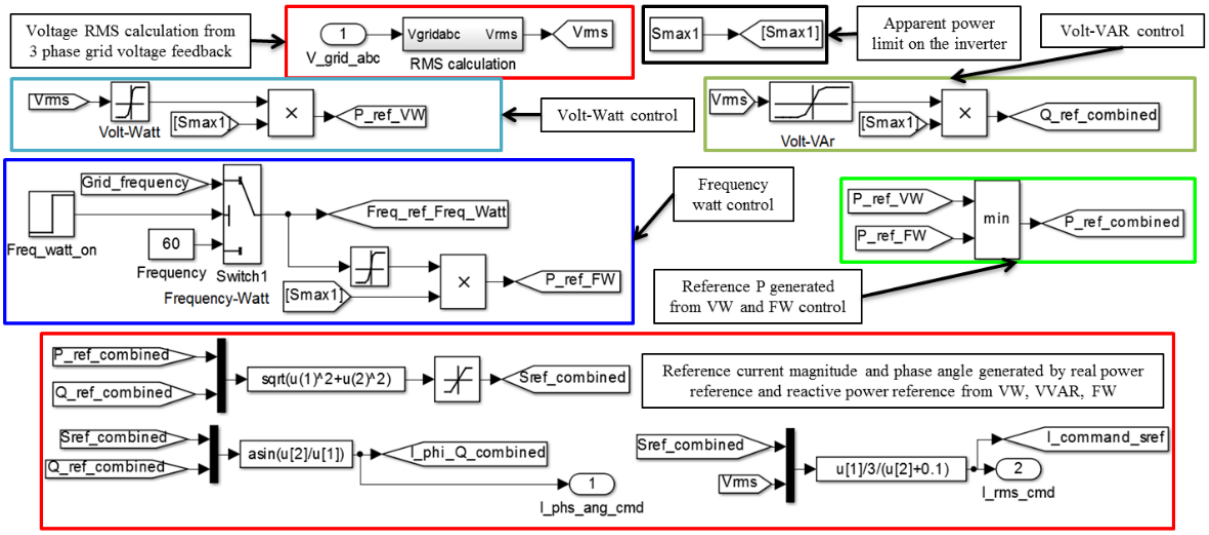


Figure 42. VVAR, VW, and FW control implementations.

The curve used for VVAR was designed for testing purposes, but it closely resembles the curve from IEEE 1547-2018. The VVAR-enabled inverter injects or absorbs reactive power autonomously to the grid in order to mitigate grid voltage fluctuations. Both the VW and the FW curves generate the real power references. The VW parameters were selected so that after the VVAR control reached its reactive power absorption limit, the VW curve would start curtailing real power generation. The goal of FW is to work along with the VW to generate the real power reference. The curve used for FW was also designed to make testing of the controllers easier. After two real power references are generated, priority is given to the controller that curtails more heavily. Finally, a check is made to ensure that the apparent power calculated from the real power and the reactive power references does not exceed the apparent power limit of the inverter. After this check, the current magnitude and the phase angle references are generated for the current control. Many simulation test cases were run to validate these advanced functions. Results from a sample case study are shown in Figures 43–46. The VVAR, VW, and FW curves for this case study are shown in Figure 43.

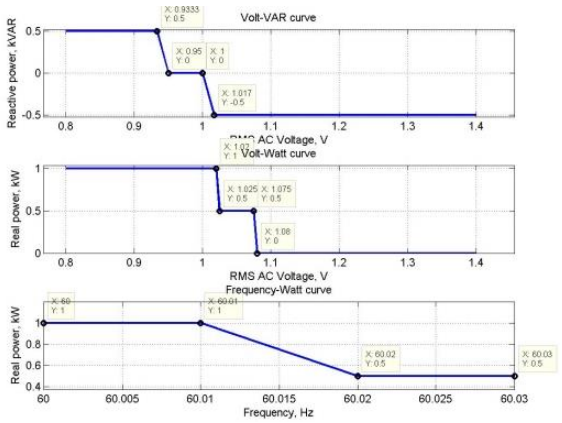


Figure 43. Curves used in testing.

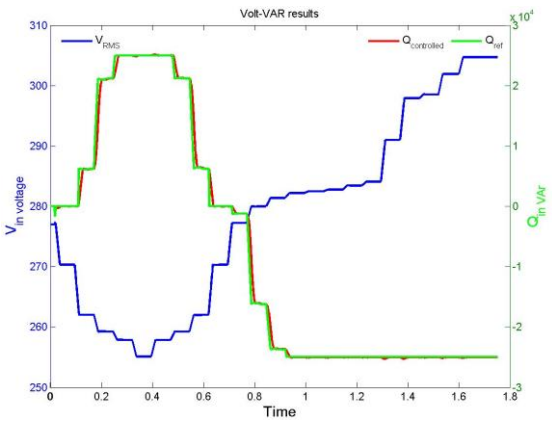


Figure 44. VRMS, Qreference by VVAR, and Qcontrolled.

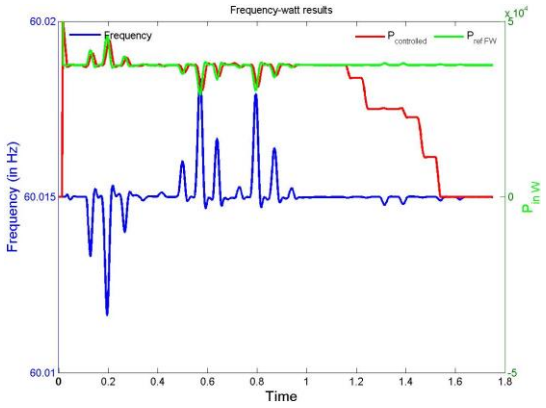


Figure 45. Grid frequency, Preference by FW, and Pcontrolled.

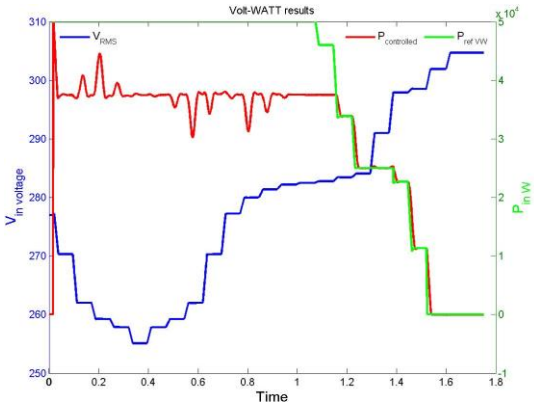


Figure 46. VRMS, Preference by VW and Pcontrolled.

The key characteristics in the VVAR and VW curves include the saturation point for VVAR and the starting point for VW. The saturation point in VVAR indicates that the inverter has reached its maximum acceptable range of reactive power absorption. In this test case, the frequency of the grid was kept at 60.015 Hz. This starting frequency helped in varying the real power reference from 1 per unit (pu). The corresponding reference active power for 60.015 Hz is 0.75 pu, which translates to 37.5 kW. This can be verified in Figure 46. The grid phase voltage RMS was reduced from 1 pu (277 V) at the start of the simulation to 0.92 PU (254 V) and then back to 1 pu. It was then increased until it reached 1.1 pu (304 V). This variation provided the capability to trace the references in the VVAR curve and VW curve. Figure 44 indicates that when V_{RMS} is high, reactive power (Q) is absorbed; and when V_{RMS} is low, Q is injected; and at V dead band, Q is set at 0. In Figures 44, 45, and 46, a green line indicates the reference point set by the corresponding controllers ($P_{reference}$ and $Q_{reference}$) and a red line indicates the controlled parameters ($P_{controlled}$ and $Q_{controlled}$). Other advanced grid-support functions such as voltage ride-through, frequency ride-through, and ramp-rate control were also developed and verified using simulations. The verification through HIL and hardware is presented later in this report. There are multiple anti-islanding schemes available in the literature [2]–[4]. Islanding operation of PV inverters occurs when the main grid is interrupted, and the general inverter protection schemes fail to identify this interruption. Because of this failure to identify the grid outage, the inverter keeps supplying power into the distribution network. For the PV inverter controller, a positive feedback–based inverter resident active anti-islanding scheme was used and verified by simulation.

A simplified block diagram of the anti-islanding scheme is shown in Figure 47 and Figure 48 [5]. This scheme uses the grid frequency as the feedback and is passed through a band pass filter, a gain, and a limiter. The resulting value is a current variation that is added to the q-axis current reference in the PWM signal generator. At the optimal gain value, if the grid is available, the change in Q-component of the current (ΔI_Q) generated is small to ensure the system is stable. At the optimal gain value, if the grid is not available, the ΔI_Q creates a perturbation in the frequency, thus pushing it to unstable. This rate of change of frequency is set so that the frequency will reach a high value very quickly and trigger the frequency trip settings. The developed scheme was tested in simulation, HIL, and a hardware setup. The results from the HIL and hardware setups are provided later in the report.

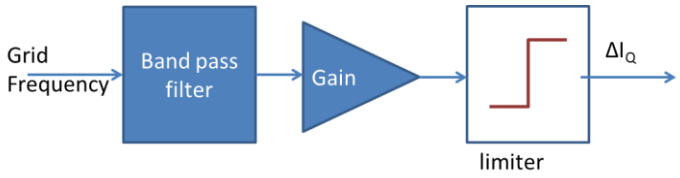


Figure 47. Frequency perturbation-based active anti-islanding scheme.

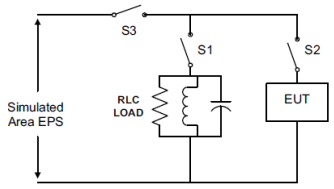


Figure 48. IEEE Std.1547.1 test setup used in the simulation to test the anti-islanding scheme.

3.1.3.3 Firmware Development and CHIL Setup

The firmware implementation of the control algorithms was carried out in the NI sbRIO (NI 9607). The control algorithms were implemented in both real-time (RT) processors and in FPGAs. Advanced inverter control functions VVAR, VW, FW, voltage ride-through (VRT), and frequency ride-through (FRT) were programmed in the real-time layer. The FPGA controller was coded in LabVIEW FPGA; it implemented all the high-speed inverter control functions, including AC current and DC voltage feedback control loops, phase-lock loop, and unintentional island detection algorithms. The code allowed inverter operation in AC current control or DC bus voltage control modes. The 3-phase inverter control was performed in the rotating synchronous frame, i.e. the dq-frame. Sinusoidal PWM at 20 kHz switching frequency was implemented that included a user-adjustable dead time. The AMPVI controller hardware (including both RT and FPGA control algorithms) was tested using CHIL. For the testing, a switching-level model of the 3-phase inverter was implemented on the Opal-RT OP5607 FPGA expansion chassis. The OP5607 includes a Xilinx Virtex V FPGA that can be programmed using the Opal-RT eHS Gen3 real-time power electronics simulation toolbox. This toolbox allows creating switching-level models of power electronics using Matlab/Simulink SimPowerSystems blocks, which will then run on the FPGA at much higher rates than would be possible on the Opal real-time processor. For this testing, the inverter, as well as the DC input and AC grid connection, were simulated on the OP5607 at a 500 ns time step, or 1% of the 20 kHz switching period. The modeled inverter voltage and current waveforms were connected to the sbRIO analog input channels via the OP5607 analog output channels. Similarly, the sbRIO PWM and trip outputs were connected to the modeled inverter inputs via the OP5607 digital input channels.

3.1.3.4 CHIL Validation of Control Algorithms

Three test cases are presented here for validating the developed control algorithms and the firmware implementation. The firmware implementation of the control algorithms was done in the NI sbRIO (NI 9607). The control algorithms were implemented in both RT processors and in FPGAs, as shown in Figure 49.

Frequency-Watt—In this test case, voltage and frequency were controlled in the Opal machine to compare the CHIL performance of advanced inverter functions VW, FW, and VVAR with the simulation results. Table 1 summarizes grid voltage and frequency set points for a simulation-only test scenario. The voltage was set at a constant 0.975 pu throughout the simulation. The VAR reference for this voltage was 0. The frequency was changed from 60 Hz to 60.1 Hz and then back to 60 Hz. At 60.1 Hz, the active power set point was 0.5 pu (25 kW). The simulation result and CHIL result are shown in Figures 50 and 51. It can be observed that the steady-state results match the frequency-watt curve programmed in the controller. In Figure 51, results for the same voltage and frequency set points are shown.

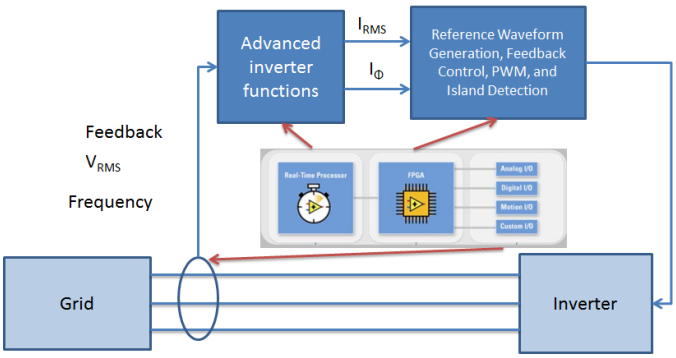


Figure 49. Simplified block diagram showing implementation of inverter control functions.

Table 1. Test case used in the simulation-only scenario

Time (s)	V (pu)	F step (Hz)	Watt reference
0.08	0.975	Steps from 60 to 60.1	Sets 1.0 pu at 60.0 HZ and 0.5 pu at 60.02 HZ
0.3	0.975	Steps from 60.1 to 60	Sets 0.5 pu at 60.02 HZ and 1.0 pu at 60 HZ

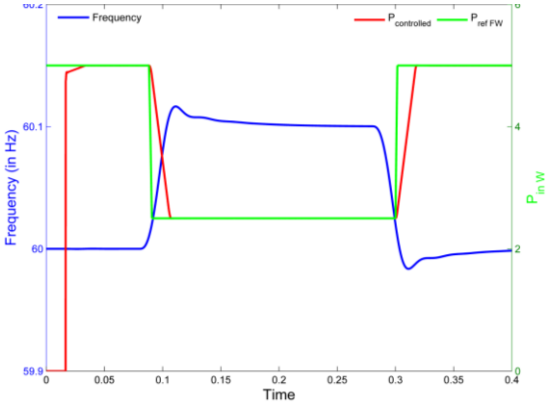


Figure 50. Comparison of FW test case (pure simulation).

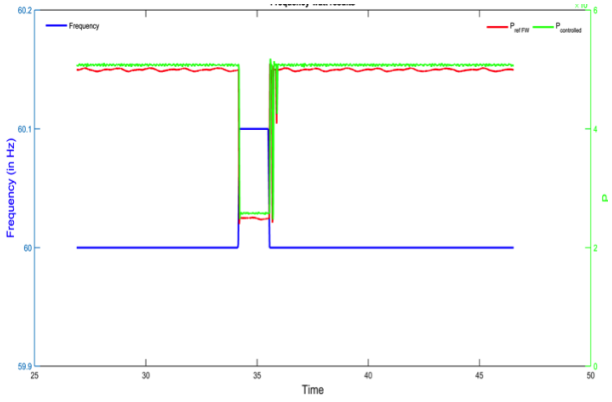


Figure 51. Comparison of FW test case, (CHIL results).

Over-voltage ride through (OVR)—This case tests the ride-through controls programmed in the simulation model and the CHIL setup. The ride-through feature of OVR1 was tested. For this OVR1 case, when grid voltage exceeded 1.1 pu, a timer was started; and if the voltage remained at this level for more than 0.92 seconds, a trip signal was enabled. At the start of the experiment, the voltage was programmed to exceed OVR1 for less than 0.92 seconds and then it was brought back to a nominal value; no trip was enabled, as expected. Again, the voltage value was programmed to exceed OVR1 (but under OVR2), and it stayed at that level for more than 0.92 seconds. Once the timer exceeded 0.92 seconds, a trip signal was generated and sent to the circuit breaker. This process is shown in Figures 52 and 53, for both the pure simulation and the CHIL case. The current waveform in Figure 53 is scaled up by a factor of 10 for better viewing.

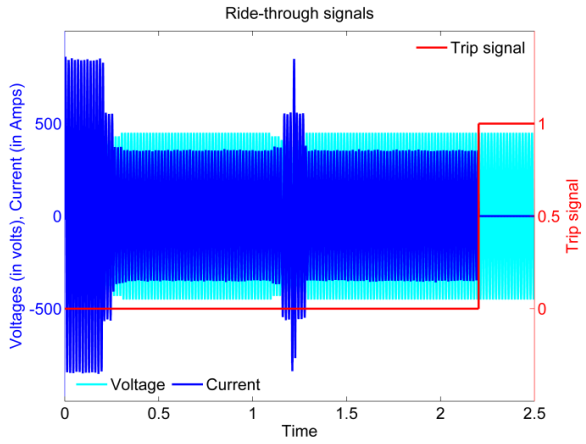


Figure 52. Comparison of voltage ride-through functions, pure simulation (current is scaled by 10).

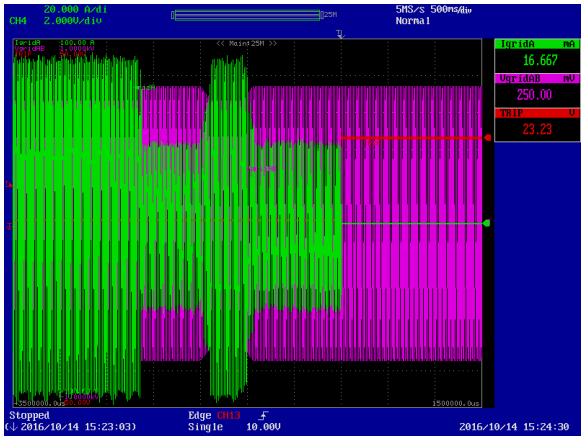


Figure 53. Comparison of voltage ride-through functions, CHIL results (time scale = 500 ms/div; green = Ia (20 A/div), pink = Vab (100 V/div), red = trip signal).

3.1.3.5 Development and Validation of Communication Functionalities

Communication protocols are necessary for interoperability of inverters with other smart devices. Also, it is necessary to modify settings of advanced inverter functions like volt-var, ride-through, and ramp-rate when needed. The next development for the inverter controller was focused on making the developed controller interoperable. This was achieved by enabling Distributed Network Protocol (DNP3) communications for the inverter controller, in alignment with the IEEE 1815-2012 standard. These communications algorithms were coded and implemented on the controller using LabVIEW. Then the validation of DNP3 communications protocols on the prototype controller board was done using the CHIL setup (Figure 54).

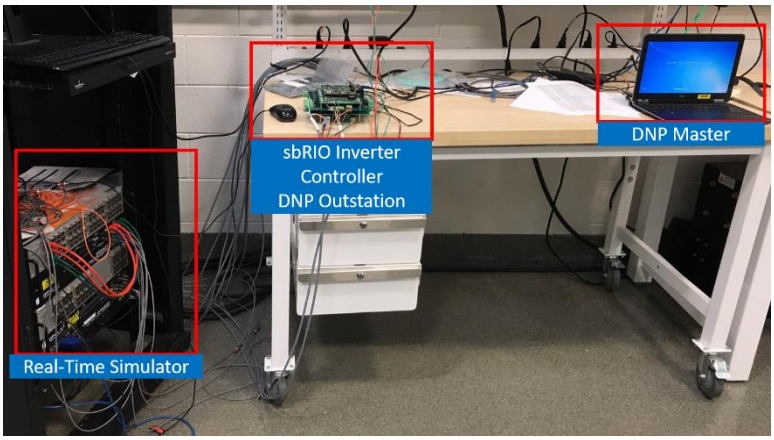


Figure 54. Controller hardware-in-the-loop setup to test DNP3 communication.

DNP3 is used in the power industry for communication between different intelligent electronic devices used in the power industry. Generally, master DNP3 station sends requests to a DNP3 outstation and the outstation respond to these requests. Outstations are generally remote computers used in the field. Outstation devices gather data and transmit it to the master. This data could be binary and/or analog.

DNP3 has an application note (AN2013-001 – DNP3 profile for advanced photovoltaic generation and storage). This application describes the standard data point configuration, set of protocol services and profiles for communicating with photovoltaic (PV) generation and storage systems using DNP3. This profile makes it easier to interconnect the DNP3 masters and outstations that control these systems. This application is designed based on the data models of the IEC 61850 protocol.

The PV inverter is typically programmed as an outstation. The master (DMS emulation) which sends the information to the inverter using DNP3 protocol is emulated using Triangle Microworks–based Distributed Test Manager. Figure 54 shows the CHIL setup with the master, outstation, and OPAL-RT hardware. The registers for the advanced inverter function were borrowed from the application note (AN2013-001–DNP3 profile for advanced photovoltaic generation and storage). A CHIL-based experiment was performed to validate the capability of the control board to update curve points through DNP. Figure 55 shows the data transfer between different layers of the CHIL setup. The DNP master sends the VVAR and VW curve settings to the sbRIO (DNP outstation). These data are stored in the real time layer of the sbRIO.

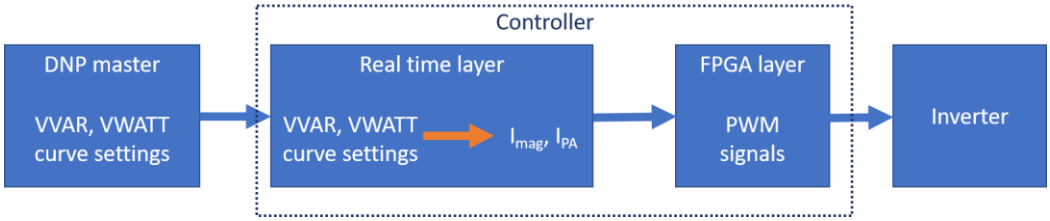


Figure 55. Data transfer between different layers of the CHIL setup.

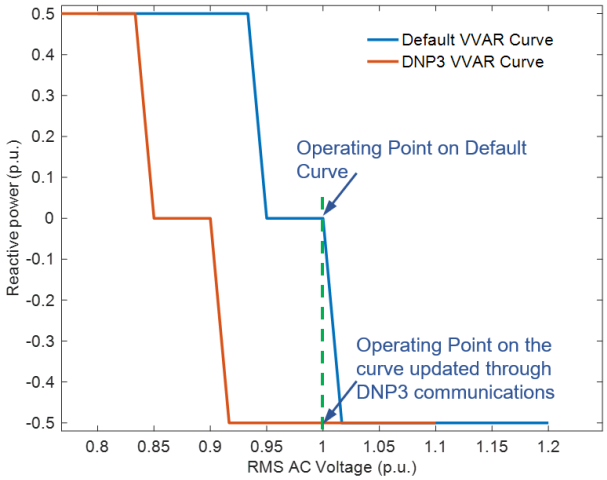


Figure 56. The inverter default and DNP3 updated VVAR curves used for CHIL verification.

The verification test case was to change the inverter operating VVAR curve through DNP3 communications and verify the inverter operation. The default curve that was stored in the outstation (sbRIO) and the VVAR curve sent from the master are shown in Figure 56. During this test, the grid-side voltage was not changed and was kept close to nominal at about 1.001 pu. As can be seen from Figure 56, for a grid voltage of 1.001 pu, the inverter should absorb about 0.5 pu reactive power, as per the DNP curve, while the reactive power absorbed is almost zero. The results for a change in inverter operation

from a default operating curve to a curve sent by the master are shown in Figures 57 and 58. Initially the inverter was operating based on default curve settings (see Figure 56), i.e., absorbing almost zero reactive power. DNP3 communication was enabled at t = 479 seconds, and the inverter received the new VVAR operating curve. The new reference operating point (see Figure 56) for the inverter therefore changed and the inverter actual reactive power followed the new reference point, as can be seen in Figure 57. Note that the ramp on the reference points is due to implemented ramp rate control.

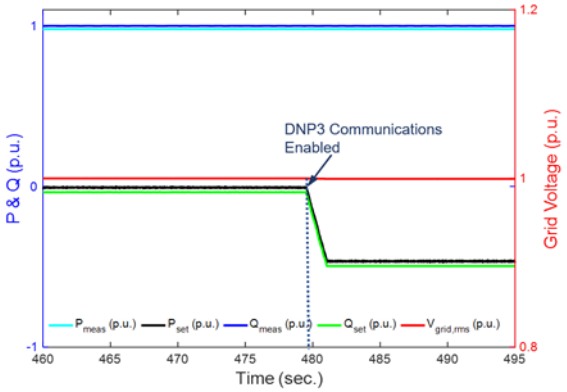


Figure 57. Change in inverter operating point when DNP3 communication with the master is enabled.

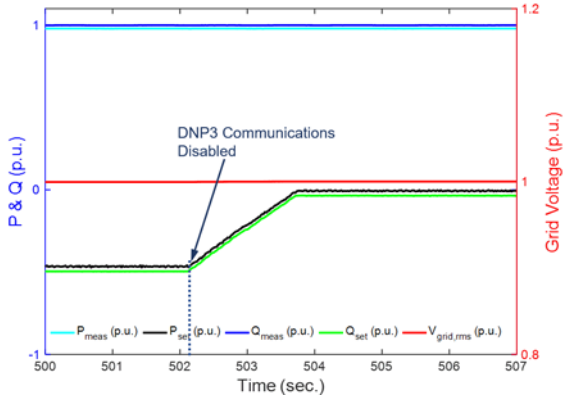


Figure 58. Change in inverter operating point when DNP3 communication with the master is disabled.

Additionally, the active power set point and measured active power remained unchanged, as only the VVAR curve was updated through communication from the master while keeping the VW curve the same. Figure 58 shows that the inverter started following the default curves when the DNP3 communication was disabled. This is important, as the inverter should be capable of operating and providing grid services even in the event of a loss of communications. In the developed algorithms, the inverter reverted to default operating curves in case of a loss of communication, but this can easily be modified to keep the inverter operating at the last curve sent by the master in case of a loss of communication.

3.1.4 Task 4: Inverter Development and Validation

The objective of this task was to develop methodologies for inverter thermal and enclosure design. Two inverters were designed and developed in this project—the alpha prototype and the gamma prototype. This section presents the design, development, and evaluation first of the alpha prototype inverter and then of the gamma prototype inverter.

3.1.4.1 Electrical Design

The electrical design for the alpha prototype inverter was completed and various design requirements were finalized—such as inverter topology, DC and AC filters, sensing requirements, and protection—based on the transient-domain, switching-level simulations of the inverter. Electrical systems including controls were completed in SimPowerSystems to compare the results with various DC voltages, AC filter types, filter sizes, leakage capacitances, and grid impedances. Based on the simulation results, the LCL AC output filter topology was selected and initial values for the LCL filter were provided to the magnetics design task for the optimization algorithm. In addition, the common mode voltage information was acquired from the simulations and was used for the DC-link inductor design under the magnetics design task. The design consisted of two parts, the inverter and the disconnect box. The inverter itself was a single-stage, two-level, 3-phase 50 kW, DC-to-AC converter.

The disconnect box design for this project consisted of connections to the PV and the grid. This design also included the common-mode filter needed for this transformer-less, single-stage inverter.

3.1.4.2 Alpha Prototype Inverter Design and Validation

The objective of this task was to construct and test the alpha prototype inverter and then revise the design to develop the final gamma inverter prototype. The alpha-prototype of the inverter along with its DC-disconnect box was built based on the design presented. The electrical schematic of the inverter box and the picture of the alpha-prototype inverter are shown in Figures 59 and 60, respectively.

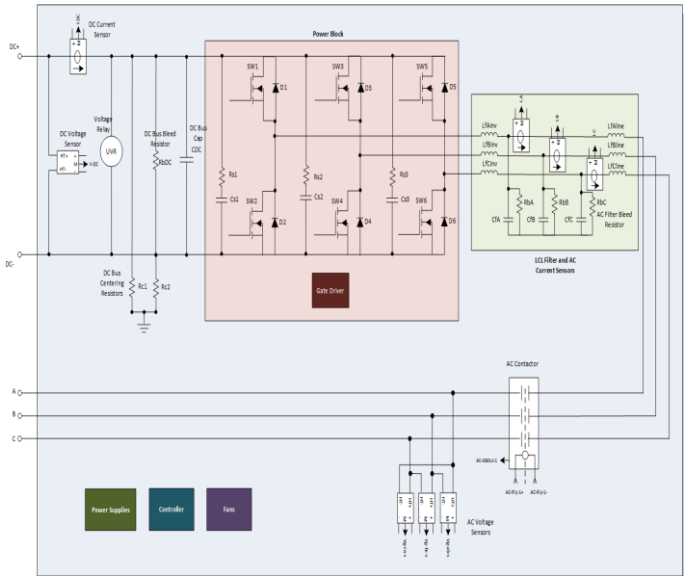


Figure 59. Electrical schematic.

Figure 60. Developed alpha-prototype inverter.

Alpha Prototype Evaluation—The testing of the inverter was done sequentially, and the results are presented next. The inverter was tested in stand-alone, open loop voltage-control mode, followed by testing in grid-tied, closed loop current-control mode.

- Voltage-Control Mode

To limit failure scenarios and for ease of troubleshooting, the inverter was first tested in open loop voltage-control mode, in which the inverter was connected to a variable resistive load. The dc-bus voltage was maintained at ~900 V and the output line-to-line voltage was commanded to be at 480 V_{rms}. The inverter output voltage and current waveforms were monitored for different loads to quantify the waveform total harmonic distortion (THD) and inverter efficiency. The output line-to-line voltages and line currents had a THD of less than 5% for all the loads. The waveforms of the three line-to-line voltages and line currents when the output power from the inverter is 40 kW and 50 kW are presented in Figure 61 and 62, respectively. The THD of the line-to-line voltages for 40 kW and 50 kW output power was measured to be about 1.12% and 1.24%, respectively. The THD of the load currents for 40 kW and 50 kW power being supplied by the inverter was measured to be about 2.35% and 2.14%, respectively. The efficiency of the inverter was also measured at different loads. The peak efficiency of the inverter was measured to be 98.20% with a load of about 45 kW, which corresponds to 90% of the rated output. The CEC efficiency of the alpha-prototype was computed to be about 97.72%.

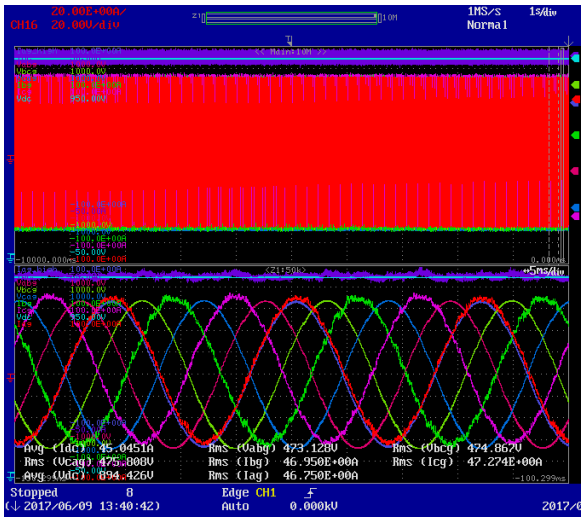


Figure 61. Measured 3-phase waveforms of line-to-line voltages and line currents for different output power and output line-to-line voltage of 480 V (output power = 40 kW.

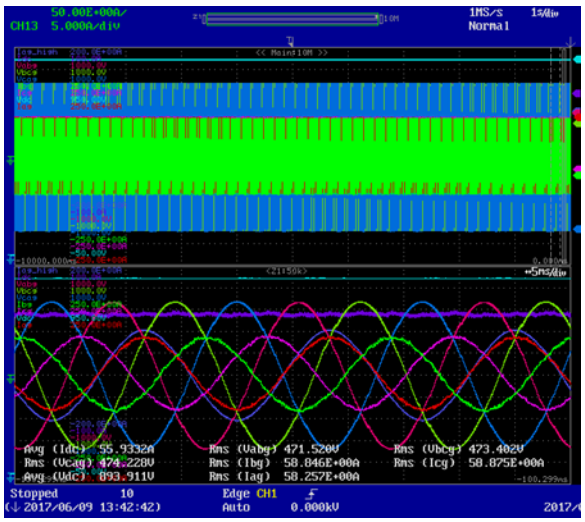


Figure 62. Measured 3-phase waveforms of line-to-line voltages and line currents for different output power and output line-to-line voltage of 480 V (output power = 50 kW.

- Current-Control Mode

The first test performed in verifying the grid-connected operation of the alpha prototype inverter was to operate it under constant current command. This test was done with a DC bus voltage of 897 V and grid-side RMS line-to-line voltage of 480 V. Figures 63 and 64 show the waveforms of the 3-phase inverter output currents and 3-phase line-to-line voltages at the point of common coupling when the inverter was injecting 50 A and 60 A current into the grid, respectively. The current waveforms shown in Figures 63 and 64 are measured on the inverter side (before the filter). The THD of the grid current was measured to be between 3.62 and 5.0% for the cases shown in the figures. The efficiency of the inverter at full load was measured to be about 98.18%, while the peak efficiency was measured to be 98.2% ± 1.48%. Note that the power dissipation in the controller and the fans was measured to be about 98 W and is also included in computing the efficiency of the alpha prototype inverter.

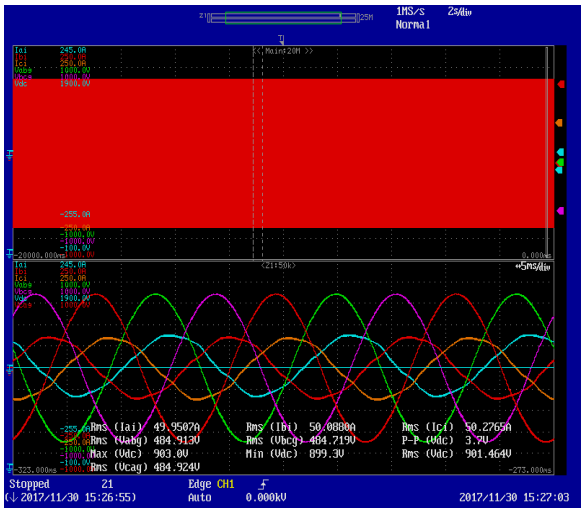


Figure 63. Measured 3-phase waveforms of line-to-line voltages and line currents for different output power in current control mode of operation (output power = 41.5 kW).

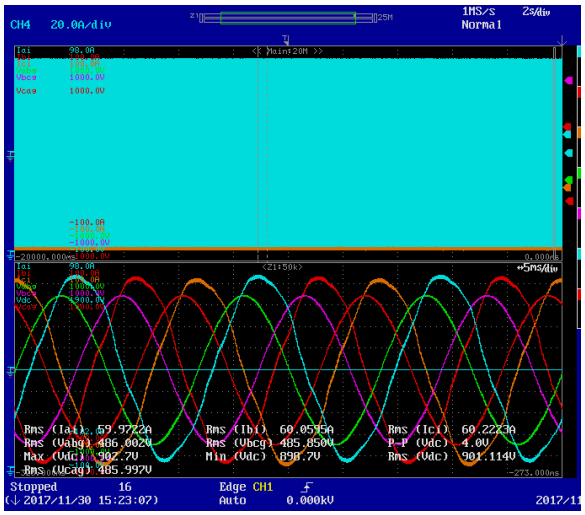


Figure 64. Measured 3-phase waveforms of line-to-line voltages and line currents for different output power in current control mode of operation (output power = 50 kW).

- Advanced Inverter Functions Verification

The next set of tests were done to verify the developed advanced inverter controls. A large number of test cases were run to validate these advanced functions. The results presented here are for verification of (1) VVAR control, (2) VW control, (3) VRT controls, and (4) anti-islanding function.

The first test case is VVAR verification. Figure 65 shows the VVAR curve used for the verification. The grid-simulator (Ametek RS-90) used for the tests was coded to provide voltage steps at different time intervals, as shown in Figure 66. The inverter was capable of changing the reactive power injected into the grid through these voltage changes. Furthermore, it can be seen from Figure 66 that the measured reactive power injected into the grid followed the volt-VAR curve presented in Figure 65.

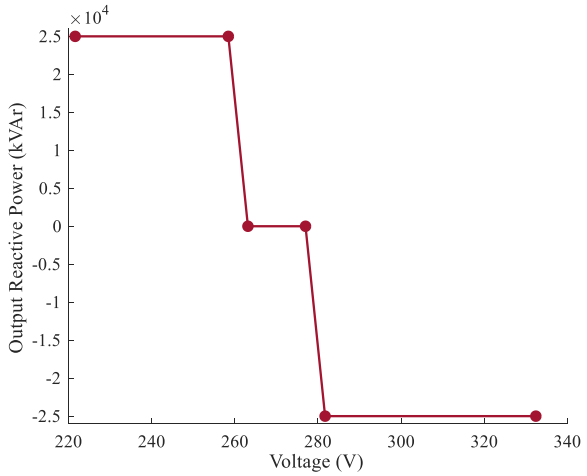


Figure 65. VVAR curve used in verification.

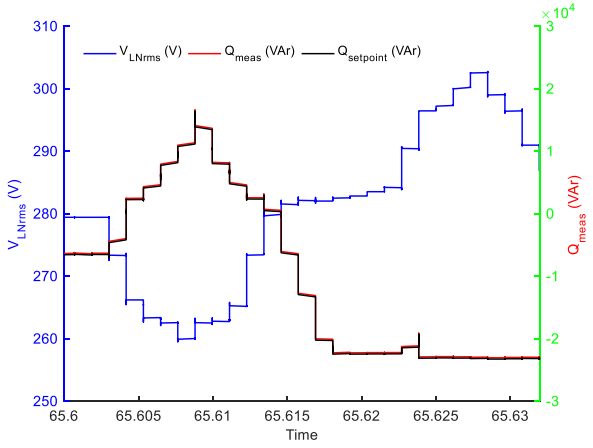


Figure 66. Test results showing voltage steps and measured reactive power injected into the grid.

In addition to the regulation functions, both the VRT and FRT were implemented in the controller. When the voltage or frequency exceeded the limit, an elapsed timer was triggered. The voltage and FRT settings that closely matched Hawaii's ride-through requirements were used for testing purposes[6], but these values can easily be modified for other regional or IEEE 1547-2018 settings. In this verification, the OVR1 setting was tested. This particular OVR1 setting gets activated when the grid voltage is over 110% but less than 120% of the nominal voltage. For that operating region, the inverter is required to ride-through for 0.92 seconds. If the voltage does not return to the normal range in that time, the inverter should trip. In the test results, it can be observed that the voltage exceeded 1.1 pu (431 $V_{ph,peak}$) at about 0.45 seconds. At 0.75 seconds, the voltage dropped to normal range and thus did not trigger the trip signal. At 1.35 seconds, the voltage increased to 1.1 pu and stayed at that voltage level.

The trip signal was triggered after 0.92 seconds as expected and required. Note that the trip signal shown in Figure 67 is the actual 24 V signal being sent to the 3-phase AC contactor by the sbRIO. It can be seen from Figure 67 that during normal operation and ride-through periods, the trip signal is at 24 V; i.e., the contactor is ON. When the ride-though limit is reached at about 2.25 seconds, the controller sends 0 V to the contactor coil to trip it.

The next advanced grid-support function verified for the developed alpha prototype inverter was the anti-islanding function. The inverter was operated at a current command of 55 A and phase angle of 0° and with a 45 kW resonant load with a Q-factor of 1 connected to the inverter terminals. The grid was then disconnected from the inverter output and the waveforms were captured. The plots in Figures 68 and 69 include inverter line-line output voltage (between phases A and B), the status of the grid circuit breaker, and the status of the inverter circuit breaker. Figure 68 shows the case when the island detection algorithms were disabled. The test results show that when the grid outage was performed, the inverter failed to disconnect from the grid beyond the 2 second limit as specified by IEEE 1547-2018. All advanced functions were disabled for these tests; instead, the sbRIO was configured to trip the inverter off-line immediately if the frequency reached ±5 Hz. Figure 69 shows the case when the anti-islanding algorithms were enabled. For this case, the trip happened within 2 seconds after the grid breaker was opened. The test started with normal operation, and the grid was disconnected from the inverter and the load at 2.15 seconds. After that simulated grid outage, the ΔI_Q value increased, thus perturbing the frequency. The frequency started increasing and reached 64 Hz at around 3.7 seconds when the FRT control block detected the over-frequency and opened the inverter circuit breaker. The effective time for this gain value to trip the circuit breaker was around 1.55 seconds from the beginning of the grid outage.

Note that even with the FRT settings enabled, at such a large frequency deviation, the inverter will trip immediately; hence, no additional delay in tripping will be noticed.

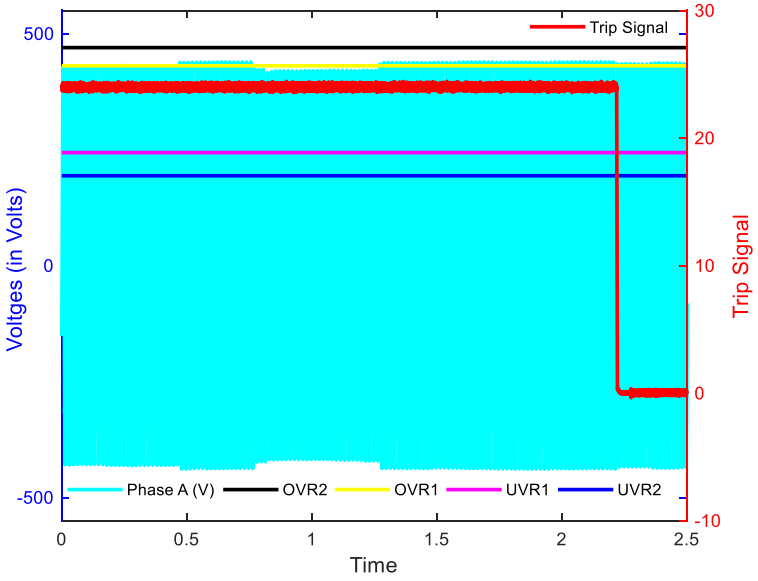


Figure 67- Experimental results for VRT showing two over-voltage events

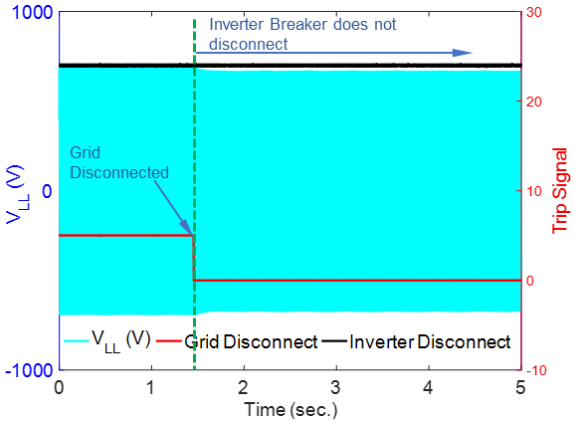


Figure 68. Experimental results for validation of anti-islanding algorithm with algorithm disabled.

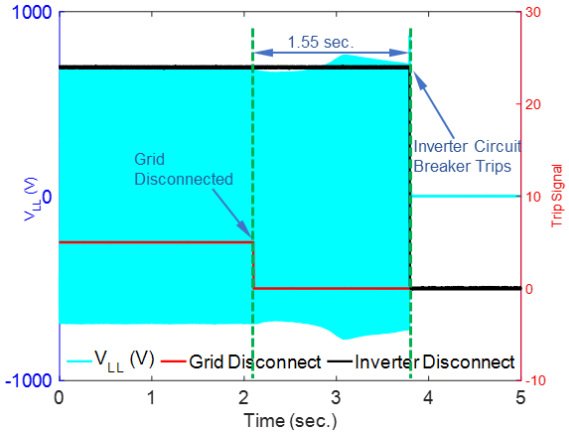


Figure 69. Experimental results for validation of anti-islanding algorithm with algorithm enabled.

- Inverter testing in Hardware-in-the-loop (HIL) setup

In addition to the experimental validation of the alpha prototype inverter for stand-alone operation, closed loop grid-connected operation, and grid-support functionality, the developed inverter and its controls were evaluated in a PHIL setup. Figure 70 shows the block diagram of the hardware setup for the PHIL system-level validation of AMPVI. A representative reduced-order feeder model was selected to develop the PHIL test setup. A transformer was used to connect the 13.2 kV distribution feeder to the 3-phase 480 V output of the alpha-prototype inverter. In this verification, a high-voltage grid event was created to verify overall system operation and to check the inverter response to the grid event. The result for this test is shown in Figure 71. The grid voltage increased to about 1.08 pu in 0.3 seconds. The experimentally measured 3-phase grid voltage, 3-phase inverter current, and reactive power injected by the inverter into the grid are presented in Figure 71. It can be seen from the results that the inverter current decreased and

the reactive power was being drawn from the grid following the programmed VVAR curve. The alpha prototype inverter and the developed controls performed as required during grid event when tested in a PHIL setup.

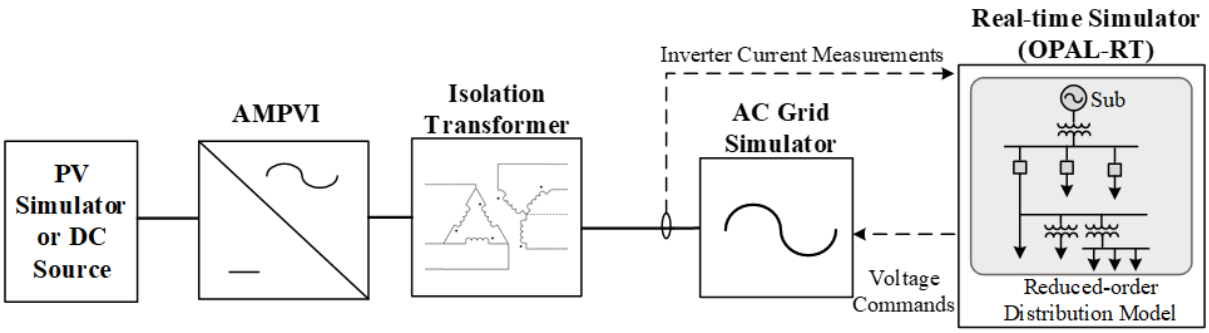


Figure 70. System-level testing of the AMPVI with simulated grid models using PHIL.

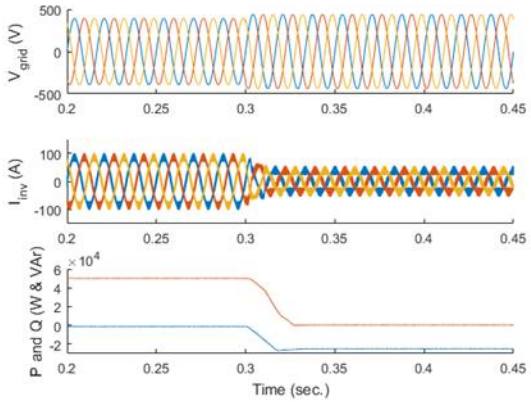


Figure 71. Plot of experimental results for inverter testing in PHIL setup when a high-voltage event occurs at the grid.

As noted previously, the alpha prototype inverter was evaluated for stand-alone voltage-control mode, closed loop grid-tied mode, all grid-support functions, and grid variations in a PHIL setup. Additionally, the performance of the inverter was also quantified in terms of inverter efficiency at different loads, peak efficiency, CEC efficiency, THD of output voltage (for stand-alone mode), and THD of output current (for both stand-alone and grid-tied mode).

3.1.4.3 Alpha Prototype Inverter Cost and Reliability Analysis

To estimate the lifetime of an inverter in the early stage of design, a preliminary reliability analysis based on the failure rate of different constituent components was performed using the guidelines provided in MIL-HDBK-217F [7]. The failure rates were computed based on different factors affecting the component, considered at their extreme points, such as peak possible electrical stress factors, highest operating temperature, and worst-case environmental stress factors. A reliability analysis of the constructed alpha-prototype inverter was done to compute the mean time between failures (MTBF) for the alpha-prototype inverter. In this analysis, the failure rate of constituent components was computed by using the electrical, thermal, and environmental stress factors from data obtained in the analysis of the alpha-prototype inverter. The failure rate thus obtained was $\lambda_c = 0.0464$. Similarly, computation of the

failure rate for all the other components led to a total failure rate of λ_{tot} = 4.2188 failures/106 hours. This translates to an estimate of system lifetime for an alpha-prototype inverter or MTBF of about 27 years.

3.1.4.4 Inventions, Patents, Publications, and Other Results

1. K. Prabakar, M. Shirazi, A. Singh and S. Chakraborty, "Advanced photovoltaic inverter control development and validation in a controller-hardware-in-the-loop test bed," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 1673–1679.

2. A. Singh et al., "Development and validation of a SiC based 50 kW grid-connected PV inverter," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 6165–6172.

3. A. Singh and K. Prabakar, "Controller-hardware-in-the-loop testbed for fast-switching SiC-based 50-kW PV inverter," *IECON 2018—44th Annual Conference of the IEEE Industrial Electronics Society*, Washington DC, 2018, pp. 1109–1115.

4. K. Prabakar, A. Singh, and M. Shirazi, "Enabling DNP3 communication for sbRIO boards controlling PV inverter," Software Record SWR-18-09.

5. C. Tombari, K. Prabakar, and A. Singh, "Configuration of advanced inverter functions using IEC 61850," Software Record: SWR-19-01.

6. K. Prabakar, A. Singh, and C. Tombari, "IEEE 1547-2018 based interoperable PV inverter with advanced grid-support functions," *submitted to Photovoltaic Specialist Conference (PVSC) 2019*.

7. A. Singh, S. Reese, and S. Akar, "Performance and techno-economic evaluation of a three-phase, 50-kW SiC-based PV inverter," *submitted to Photovoltaic Specialist Conference (PVSC) 201*9.

3.2 GAMMA INVERTER PROTOTYPE

3.2.1 Task 1: Power Block

The objective of this task was to develop a high-power density power block based on improvement of the alpha prototype.

3.2.1.1 SiC Device Characterization and Loss Calculation

Power semiconductor bare dies, including SiC MOSFETs and Schottky diodes, were selected based on the desired voltage and current rating. Corresponding characteristics of phase leg module were evaluated through both static and dynamic characterization. Based on the peak current of the gamma-prototype power block, one high-side/low-side switch position comprising one Cree SiC MOSFET and one Rohm Schottky diode in parallel was sufficient to handle the rated current. However, to further improve the reliability and thermal performance of the gamma prototype, each high-side/low-side switch consisted of two Cree SiC MOSFETs and one Rohm Schottky diode. Leveraging the measured device characteristic data presented before, a detailed comparison of power losses in a phase-leg module is summarized in Table 2 regarding these two different switch configurations to justify the merits of adopting the two parallel SiC MOSFET bare dies.

Table 2. The comparison of the total loss in one switch position with different switch configurations and operating frequencies (20 kHz and 50 kHz)

	Total loss (W)	Switching loss (W)	Conduction loss (W)	Loss per bare die (W)
Single die (20 k)	75.4	9.3	66.1	75.4
Double dies (20 k)	46.4	13.5	32.9	23.2
Single die (50 k)	89.5	23.4	66.1	89.5
Double dies (50 k)	66.6	33.7	32.9	33.3

As illustrated in Table. 2, the parallel configuration can dramatically cut down the conduction loss by 33.2 W at a cost of increasing the switching loss by only 4.2 W, with a switching frequency of 20 kHz and 10.3 W at 50 kHz. In addition to the total loss savings, another merit of adopting a parallel configuration is that it shares the power loss equally among multiple devices to improve the thermal performance of the gamma prototype. Consequently, the energy dissipation on each SiC MOSFET bare die in the parallel configuration was 23.2 W, compared with 75.4 W for the single SiC MOSFET configuration; the lower dissipation significantly relieved the thermal stress for individual bare dies.

3.2.1.2 Thermal Design

Based on the loss estimation and the consideration of reliability issues, two parallel SiC MOSFETs and one free-wheeling SiC diode were designed for one switching position. To satisfy the need for higher power density and lower parasitic inductance for fast switching, both switches, i.e,. the upper switch and the lower switch, were placed on one DBC substrate. Compared with the alpha version consisting of two power blocks in a phase leg module, the gamma prototype design is much more compact. The comparision between these two power module designs is demonstrated in Figure 72. The total volume of the power module has been significantly reduced from 191652 mm^3 for the alpha prototype to 99725 mm^3 for the gamma prototype—a 48% volume reduction. In addition, to further decrease the parasitic inductance of the communication loop, a P-cell/N-cell layout is proposed in the current run of design to enable a higher switching frequency without creating any overvoltage concerns during the switching transient.

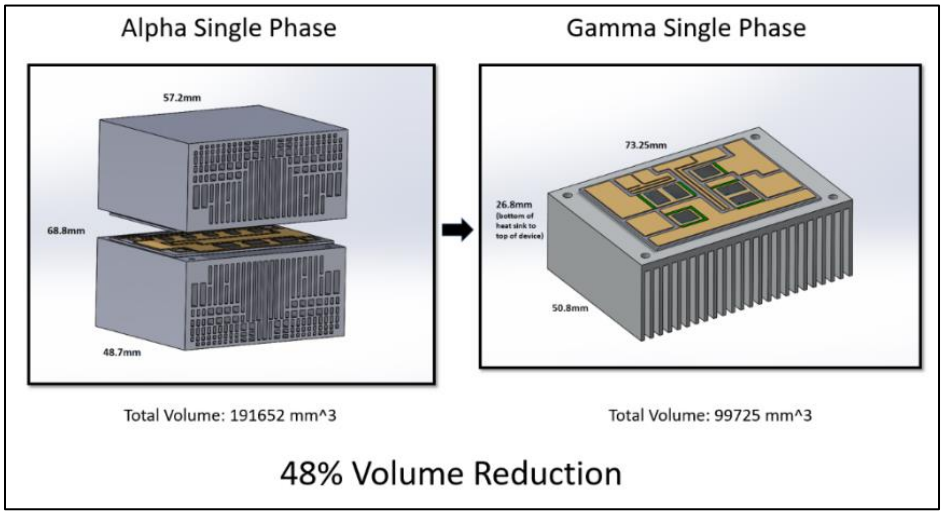


Figure 72. Power module volume comparison between alpha and gamma prototype.

Gamma-prototype Power Block Thermal Management System Design. Because of the more compact design compared with the first two versions, the thermal management system is critical for dissipating heat from the power module. In the gamma version of the design, a commercially available heat sink manufactured by Aavid was obtained, based on the footprint area of the designed DBC substrate and the required maximum thermal resistance.

To further improve thermal performance, a thermal interface material was substituted for the Tgon 800 interface pad. The thermal conductivity of Tgon 800 is 5 W/m·K compared with the thermal grease with a thermal conductivity of 0.8 W/m·K. FEA simulation was used to estimate the thermal performance of the designed module at the inlet flow speed of 4 m/s. Loss data of 20 kHz were used in the simulation for the case using two parallel MOSFETs. As shown in Figure 73, the temperature profile of the module indicates that the maximum junction temperature was below 125°C. The fan operating point has not been decided yet; however, the previous alpha design operated at 6 m/s, so a reduced flow rate of 4 m/s should be a reasonable starting point and should be achievable.

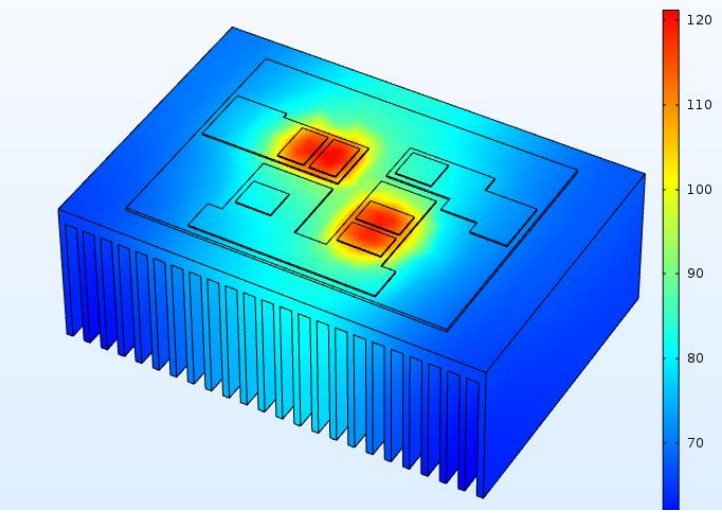


Figure 73. Temperature profile.

3.2.1.3 Power Module Development and Evaluation

Key features within the mechanical structure of the power module include a graphite thermal interface and optimized DBC to heat sink attachment. A thermal grease was used in the alpha power module, which was difficult to apply and remove. The graphite thermal interface mater (TIM) used on the solar gamma power module was an easy to apply one-sided adhesive sheet with more than five times the thermal conductivity of the thermal grease. Instead of soldering the DBC to a base plate or screwing the DBC to the heat sink directly, a multifunctional 3D printed clamp was used to evenly distribute force on open areas of the DBC shown in Figure 74. The clamp itself screwed directly to the heat sink, reducing the risk of prematurely cracking the DBC.

Once the DBC was soldered, the wire bonds were attached before the power module was placed into the lead frame/clamp assembly and encapsulated as shown in Figure 75.

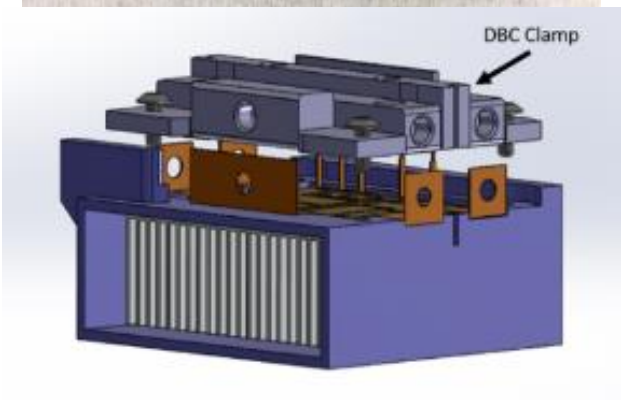


Figure 74. The assembly of the multifunctional 3D printed DBC clamp.

Figure 75. The soldered DBC with wire bonds.

The fully encapsulated and assembled gamma prototype phase-leg module with the multifunctional 3D printed DBC clamp is illustrated in Figure 76. The fabricated gamma prototype power module can be directly used for single-phase power testing, as it integrates the commercial heat sink, TIM, phase-leg module, decoupling capacitor board, and DC link capacitors. The verified multifunctional gate drive is stacked on top of the power module, as shown in Figure 77.

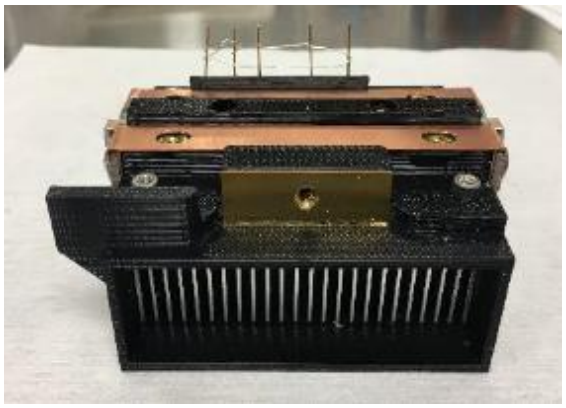


Figure 76. Front view of gamma-prototype phase-leg module.

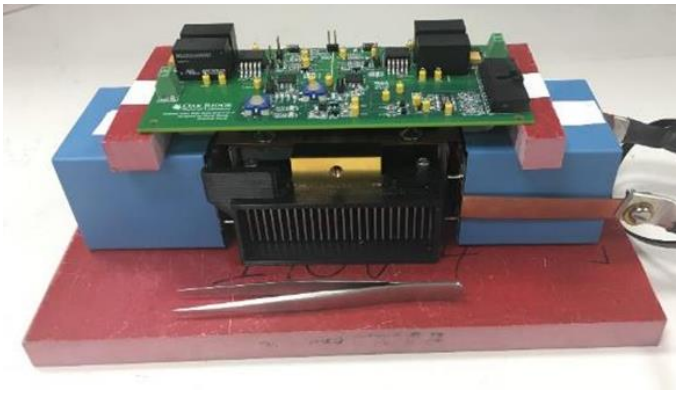


Figure 77. The assembled single-phase power module for power testing.

A single-phase power testing circuit in buck topology was built based on the fabricated gamma prototype power module. The LC filter was composed of an inductor of 0.23 mH and a capacitor of 100 μF. The maximum equivalent resistive load was around 10 Ω. The buck converter was operated at a 1 kV input DC bus voltage, 0.35 duty-cycle. The power level achieved by the buck converter was around 12 kW. The gamma prototype power module was mounted to a 3D printed plastic house with one air duct and one fan (for both the high-side switch and low-side switch) for even air flow sharing and reduced air pressure losses. Two thermocouples were used to monitor the heat sink inlet and outlet temperature values.

Figure 78 illustrates the operating waveforms and measurement results under 1 kV DC bus voltage and a 50 kHz switching frequency. As can be observed, for a 35% duty cycle, the RMS value of the inductor current was around 34 A, and the ripple current was relatively low (~15 A) thanks to the increased switching frequency compared with the alpha prototype. According to the measurement results from a power analyzer, shown in Figure 79, the input power was 11.73 kW, and the output power was 11.54 kW. The overall efficiency of the buck converter at 50 kHz was 98.38%.

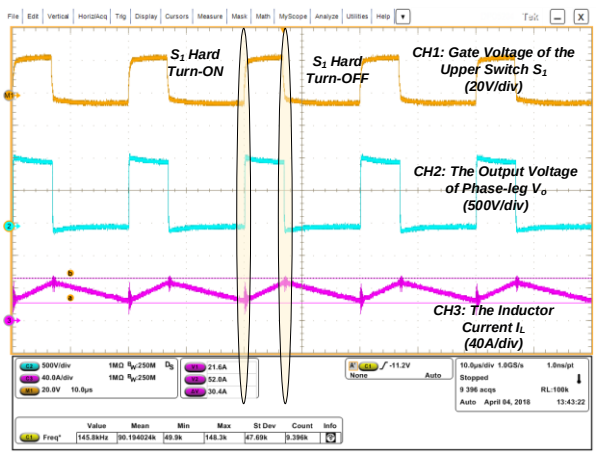


Figure 78. The experimental waveforms in buck topology at 11.73kW and 50 kHz.

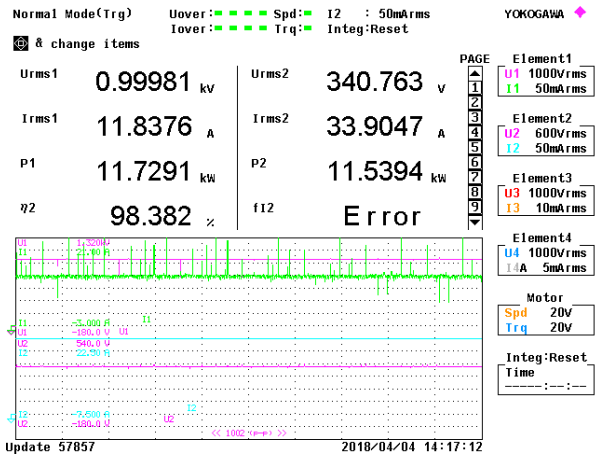


Figure 79. The phase-leg power testing results.

3.2.1.4 Power Block Development and Evaluation

The gamma inverter CAD model shown in Figure 80 and Figure 81 has been revised to the final version with the addition of the full enclosure cooling scheme, separate inverter cooling assembly, LCL filter placement, DC-DC converter board, voltage measurement board, and disconnect box. It was previously stated that the disconnect enclosure for the gamma inverter would be the same size as the enclosure for the alpha inverter. However, a new disconnect enclosure was selected, yielding a 36% volume reduction.

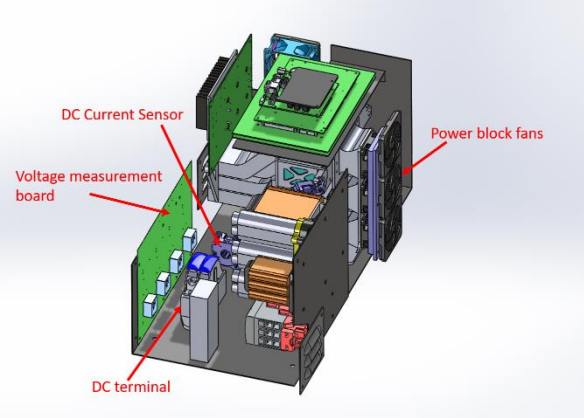


Figure 80. Gamma inverter - front view.

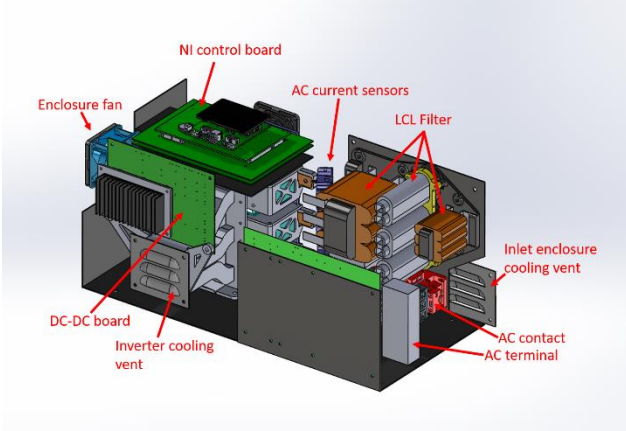


Figure 81. Gamma inverter - side view.

Power Block Development. The power block of the 3-phase inverter assembly includes the gamma power modules, each housing the DC-link capacitors, DC busbars, AC busbar, and gate driver board. The three fans are mounted to a shroud that also attaches the power modules in their respective 3-phase configuration. Figure 82 shows the full 3-phase assembly of the gamma power block CAD model and actual prototype.

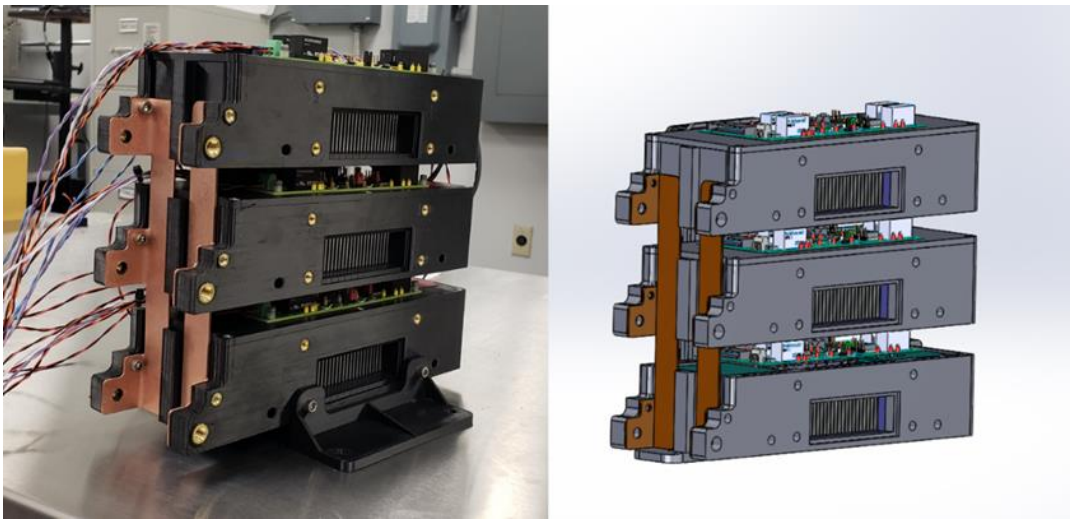


Figure 82. Full gamma power block.

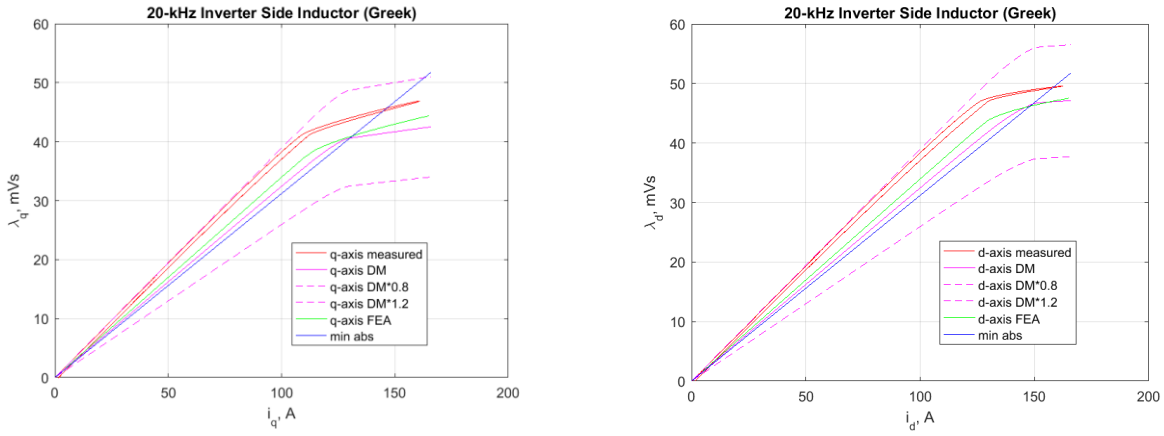
3.2.2 Task 2: Magnetics

3.2.2.1 AC Inductor

With the revisions made to the Y core AC inductor design code, the final prototype optimization was under way. For the final prototype phase, two inverter side inductors were built: one designed specifically for 20 kHz and the second for 50 kHz. To compensate for the added effort, the line-side inductors were removed from the research workload. The 20 kHz inductor was specified at 312 µH and the 50 kHz inductor at 121.3 µH. Both inductors were increased in nominal power rating from 50 kVA to 62.5 kVA to further increase the AMPVI capability. The as-built inductors are depicted in Figure 83.

Figure 83. Final prototype AC inductors: 20 kHz (left) and 50 kHz (right).

The final prototype AC inductors underwent the same progression of testing as the alpha prototypes. The first stage of electrical safety testing passed in all cases, ensuring the inductors were fit for use in in the final AMPVI system. The frequency response was also measured to evaluate self-resonance locations, with the resonance of both designs proving acceptable in excess of 600 kHz. The *q*-axis and *d*-axis flux-linkage versus current characteristic through the full range of operation and into magnetic saturation is captured in Figure 84. The difference between the model and as-built units is most likely due to differences in the parameters of the magnetic materials used compared with the parameters that are modeled. While this accuracy between modeled designs and built designs is less than ideal, the higher than anticipated inductance serves to reduce current ripple below the required value. Thermal testing completed the final prototype testing sequence with resulting temperatures consistent with the intent that the inductors could be operated under rated load indefinitely. Overall, the test results verified model predictions and the inductors were installed into the AMPVI system.



(a) *Q*-Axis **(b) *D*-Axis**

Figure 84. 20 kHz AC inductor Lambda-I versus current characteristics.

3.2.2.2 DC Common Mode Inductor

The final prototype phase was different from the alpha prototype phase in that both 20 kHz and 50 kHz rated inductors were built. Both inductors leveraged the same design code; the only difference was the designed switching frequency. A full run of the design code was performed for both desired switching frequencies, and unique designs were selected and built. The as-built inductors are depicted in Figure 85.

The final prototype common mode inductors underwent the same progression of testing as the alpha prototypes. Electrical safety tests were passed, certifying the inductors safe for use. The frequency response was measured to evaluate self-resonance locations. The frequency response depicted in Figure 86 shows resonances in excess of 100 kHz for the 20 kHz inductor and 200 kHz for the 50 kHz inductor, both sufficiently far away from the intended operating frequency.

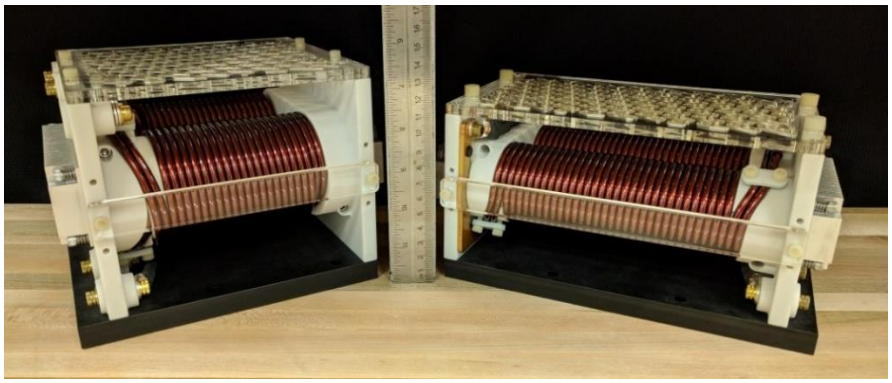
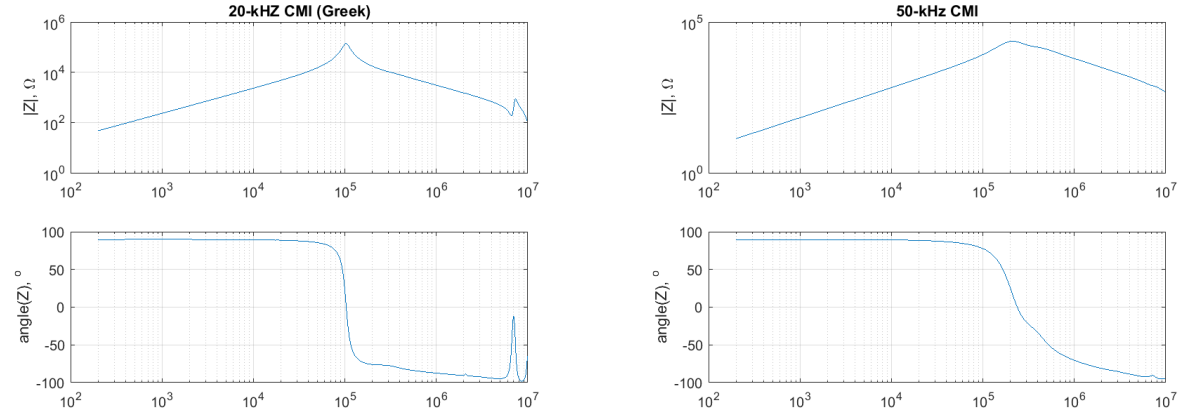


Figure 85. As-built final prototype common mode inductors: 20 kHz (left) and 50 kHz (right).

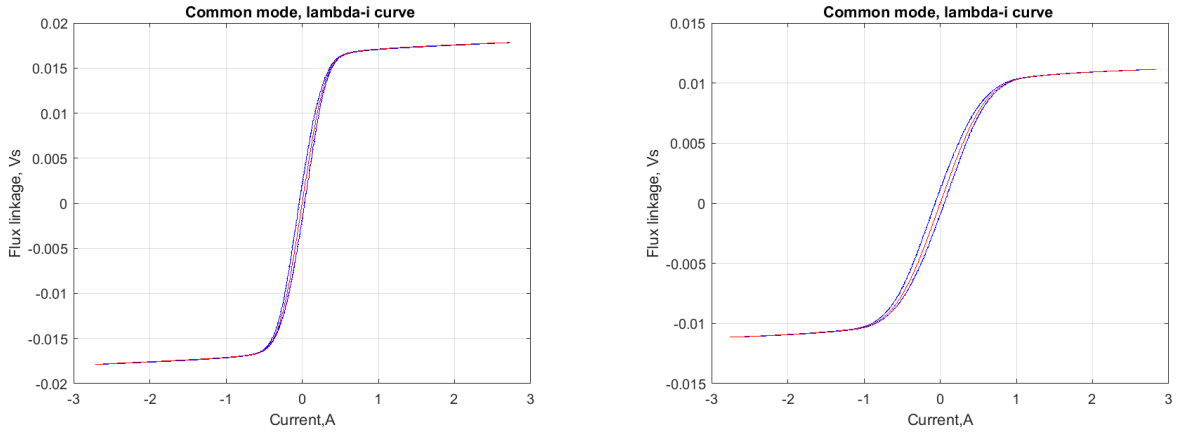


(a) 20 kHz CMI **(b) 50 kHz CMI**

Figure 86. Final prototype CMI impedance frequency sweeps.

The flux-linkage versus current characteristic through the full range of operation and into magnetic saturation was also captured and is reported in Figure 87. Inductance performance differences between the as-built units and the as-designed models did show some minor discrepancy. The variance here was expected, as the model used a conservative estimate for the effective air gap due to surface roughness of the mating core surfaces.

Thermal testing completed the final prototype testing sequence. The resulting temperatures were consistent with the intent that the inductors could be operated under rated load indefinitely. Overall, the test results served to verify model predictions; the inductors were deemed ready for installation into the final AMPVI system and were shipped to ORNL for system-level testing.



(a) 20 kHz CMI **(b) 50 kHz CMI**

Figure 87. Flux-linkage versus current characteristics.

3.2.3 Task 3: Final PV Inverter Prototype

This final task was to construct, test, and demonstrate the final PV inverter prototype for compliance with the revised interconnection standards. System-level validation and demonstration of the inverter using PHIL was conducted via testing of the final inverter prototype in open-loop voltage-control mode and closed-loop current control mode.

The full gamma inverter is shown in Figure 88, including the full enclosure cooling scheme, separate inverter cooling assembly, LCL filter placement, DC-DC converter board, voltage measurement board, NREL control platform, and disconnect box. It was previously stated that the disconnect enclosure for the gamma inverter would be the same size as of that for the alpha inverter. However, a new disconnect enclosure was selected, yielding a 36% volume reduction.

Figure 88. Full gamma version 3-phase inverter.

Test Setup and Results

The inverter was tested in an open-loop configuration, i.e., PWM signal was generated from a digital signal processor (DSP) with a preset modulation index. The input power was provided by a DC power supply. The performance of the inverter was evaluated at three input voltage levels: 800, 900, and 1000 V. To emulate a 480 V grid voltage, the inverter line-to-line output fundamental voltage was maintained at 480 V RMS by adjusting the modulation index at different DC bus voltage levels. The inverter was tested with an inductive load consisting of an inductor of 0.9 mH and a step-change resistive load for different output active powers of up to 50 kW.

Figure 89 illustrates 3-phase AC current and power analyzer results when the 3-phase inverter operates at 1 kV dc bus voltage and ~ 50 kW output power, with a switching frequency of 20 kHz. A further test with the switching frequency of 50 kHz is shown in Figure 90. The inverter AC output current is close to a pure sinusoidal wave, with some switching ripples and minor distortion at the zero-crossing point. The switching ripple can be better suppressed with higher filtering inductance and/or higher-order harmonic filters. The zero-crossing distortion is primarily caused by the dead time effect, which can be improved using various dead-time compensation techniques.

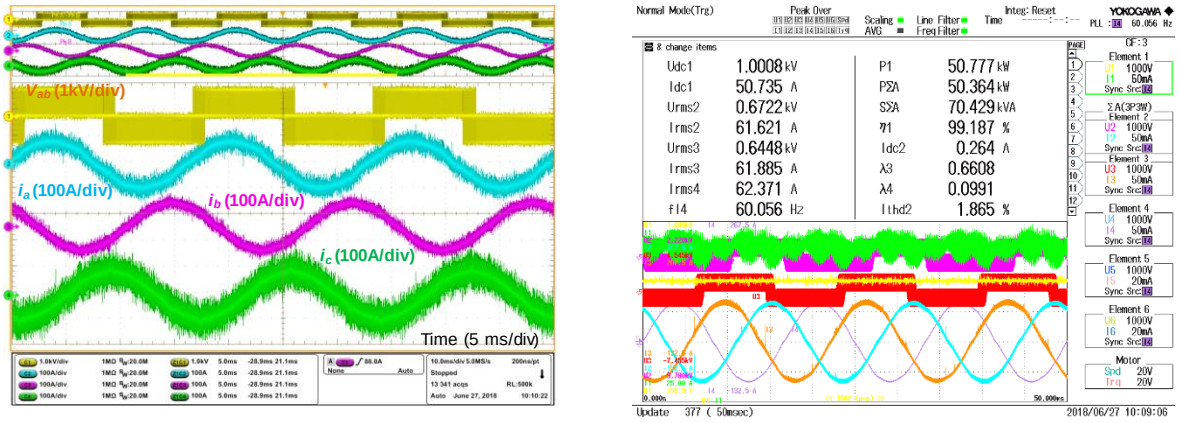


Figure 89. Three-phase AC current (left) and power analyzer waveforms (right) of the 3-phase inverter operating at 1 kV dc bus voltage and ~50 kW output power.

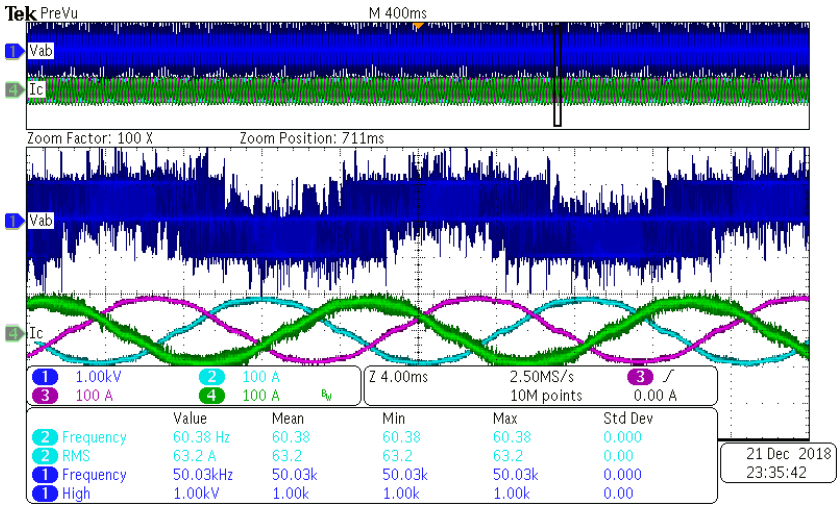


Figure 90. Three-phase AC current of the 3-phase inverter operating at 1 kV dc bus voltage and ~50 kW output power, with 50 kHz switching frequency.

4. REFERENCES

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